Lab 7: Implementation of Digital Stop Watch on Altera DE1 Board

Objective:

* To implement Digital Stop Watch design on Altera DE1 board

Open Stop Watch Project - *stopwatch*

1. Open *counter0to9* circuit and include a *clr* pin as shown in Figure 7.1.



Figure 7.1 counterOto9 circuit with clr pin

Input pin name: clk and clr

Output pins names: q3, q2, q1 and q0

2.	Create a new	symbol for	counter0to9	as shown in	Figure 7.2.	Overwrite the	e old symbol.

Symbol Libraries:	
Libraries:	
Counter0o5 Counter0o9 Jocumento Jocumento	
	1.

Figure 7.2 *counter0to9* symbol with *clr*

3. Open *counter0to5* circuit and include a *clr* pin as shown in Figure 7.3.



Figure 7.3 counter0to5 circuit with clr pin

Input pin name: clk and clr

Output pins names: q2, q1 and q0

4. Create a new symbol for *counter0to5* as shown in Figure 7.4. Overwrite the old symbol.



Figure 7.4 counter0to5 symbol with clr

5. Select and delete the $lpm_counter$ symbol (modulus count = 50,000,000) on the *stopwatch* circuit.



Figure 7.5 Delete *lpm_counter* symbol with modulus count = 50,000,000

6. Recreate the *lpm_counter* symbol with modulus count = 5,000,000.

Double-click on the blank space in the Graphic Editor window, or Click on the Symbol Tool icon D in the toolbar. A pop-up box in Figure 7.6 will appear. Type lpm_counter in the search bar to locate the symbol and Click *OK*.



Figure 7.6 Choose *lpm_counter* from the library

MegaWizard Plug-In Ma	inager[page 2c]	×			
Selected <u>M</u> egafunctions:	Which type of output file do you want to create?				
LPM_COUNTER	⊙ AHDL ⊙ YHDL				
ć	O Verilog <u>H</u> DL				
i i i i i i i i i i i i i i i i i i i	What name do you want for the <u>o</u> utput file? Bro <u>w</u> se				
4	/DIPLOMA/Year2/EG2163/g8_1/digital/stopwatch/lpm_counter0				
	Note: To compile a project successfully in the Quartus II software, your design files must be in the project directory, in the global user libraries specified in the Options dialog box (Tools menu), or a user library specifie in the User Libraries page of the Settings dialog box (Assignments menu).	d			
	Your current user library directories are:				
. 2					
t					
E Don't ask me for an out	put file name or the output file format again.				
(Note: You can turn the Block Editor's auto naming and auto format selection on and off with the Options command in the Tools menu.)					
	Cancel < <u>B</u> ack <u>N</u> ext > <u>F</u> inish				

Figure 7.7 Change output file name from *lpm_counter1* to *lpm_counter0*

MegaWizard Plug-In Ma	nager[page 2c]	×				
Selected <u>M</u> egafunctions:	Which type of output file do you want to create?					
LPM_COUNTER	AHDL					
ć	O ⊻HDL O Verilog <u>H</u> DL					
ć	What name do you want for the <u>o</u> utput file?	Bro <u>w</u> se				
i de	/DIPLOMA/Year2/EG2163/g8_1/digital/stopw	atch/lpm_counter0				
	Note: To compile a project successfully in the Qu design files must be in the project directory, in the securified in the Options divide her (Tools more)	uartus II software, your e global user libraries				
MegaWizard Plug-In Manager Image:						
E Don't ask me for an out In future, name output I	put file name or the output file format again. iles automatically and use the current output file fo	rmat.				
(Note: You can turn the Block Editor's auto naming and auto format selection on and off with the Options command in the Tools menu.)						
	Cancel < Back	<u>N</u> ext > <u>F</u> inish				

Figure 7.8 Click OK to overwrite

MegaWizard Plug-In Manager - LPM_COUNTER [page 3 of 7]							
- COLLER	<u>About</u> <u>D</u> ocumentation						
1 Parameter 2 EDA 3 Summa Settings	ary						
General > General2 > Optional Input:	s /						
Ipm_counter0	Currently selected device family:						
	How wide should the 'q' output bus be? 🛛 🔽 💽 bits						
	What should the counter direction be?						
	 Up only 						
	Down only						
e	 Create an 'updown' input port to allow me to do both 						
	(1 counts up; 0 counts down)						
1							
Resource Usage							
27 lut + 27 reg							
	Cancel < Back Next > Einish						

Figure 7.9 2^26 = 67,108,864 => Wide of 'q' output bus: 27 bits Click *Next*

MegaWizard Plug-In Manager - LPN	_COUNTER [page 4 of 7]				
- Water		<u>A</u> bout	<u>D</u> ocumentation			
1 Parameter 2 EDA 3 Sum Settings	mary					
General > General2 > Optional Inp	uts >					
lpm_counter0 up counter1 Clock modulus 5000000 Clk_en q[260] → cout →	Ipm_counter0 up counter1 up counter1 up counter1 clock modulus 6000000 Plain binary clk_en q[260] cout Modulus, with a count modulus of 500000					
	Clock Epoble	additional ports :	in.			
	Count Enable	Carry Carry	-ui			
4 6 11						
Resource Usage	Cancel	< <u>B</u> ack	Next > <u>F</u> inish			

Figure 7.10 Modulus with count 5,000,000 with Clock Enable and Carry-out ports Click Next

MegaWizard Plug-In Manager - LPM_(COUNTER [page 5 of 7]		- 🗆 ×
	TER	About Docume	ntation
Parameter 2 EDA 3 Summa Settings Ceneral Ortional Inputs			
lpm_counter0 yp_counter clock modulus 5000000 clk_en q[260] cout	Do you want any optional in Synchronous inputs Clear Load Set Set all 1's Set to all 1's	Puts? Asynchronous input: Clear Load Set Set to all 1's Set to 0	8
Resource Usage 27 lut + 27 reg	Cancel	< Back Next >	Einish

Figure 7.11 Click Next

MegaWizard Plug-In Manager - LPM_COUNTER (page 6 of 7) EDA					
	JNTER				
1 Parameter 2 EDA 3 Su Settings	mmary				
Ipm_counter0 wp counter1 clock modulus 5000000 clk_en q[26.0] cout	Simulation Libraries To properly simulate the generated design files, the following simulation model file(s) are needed F Description Ipm LPM megafunction simulation library				
Timing and resource estimation Generates a netlist for timing and resource estimation for this megafunction. If you are synthesizing your design with a third-party synthesis tool, using a timing and resource estimation netlist can allow for better design optimization. Not all third-party synthesis tools support this feature - check with the tool vendor for complete support information. Note: Netlist generation can be a time-intensive process. The size of the design and the speed of your system affect the time it takes for netlist					
Resource Usage 27 lut + 27 reg	generation to complete. Generate netlist Cancel < Back Next > Finish				

Figure 7.12 Click Next

MegaWizard Plug-In Manager - Lf	PM_COUNTER [page 7 of 7]	Summary
	JNTER	About Documentation
1 Parameter 2 EDA 3 Su Settings	mmary	
lpm_counter0 up counter clock modulus 500000 clk_en clk_en cout →	Turn on the files you wish to genera automatically generated, and a red Finish to generate the selected files subsequent MegaWizard Plug-In Ma The MegaWizard Plug-In Manager of directory: DIPLOMA/Year2/EG2163/g8_1/digit	ate. A gray checkmark indicates a file that is checkmark indicates an optional file. Click . The state of each checkbox is maintained in nager sessions. reates the selected files in the following al/stopwatch/
	File	Description
	V Ipp, counter() tdf	Variation file
	V lpm_counter0.inc	AHDL Include file
-	pm_counter0.cmp	VHDL component declaration file
	☑ lpm_counter0.bsf	Quartus II symbol file
	Ipm_counter0_inst.tdf	Instantiation template file
	☑ Ipm_counter0_waveforms.html	Sample waveforms in summary
	: lpm_counter0_wave*.jpg	Sample waveform file(s)
1		
-		
-		
-		
Resource Usage		
27 lut + 27 reg		Cancel < <u>B</u> ack Next > Einish

Figure 7.13 Click *Finish*

 Mega₩i	zard Plug-In Manager
	The MegaWizard Plug-In Manager will overwrite the following existing file(s): /DIPLOMA/Year2/EG2163/g8_1/digital/stopwatch/lpm_counter0.inc /DIPLOMA/Year2/EG2163/g8_1/digital/stopwatch/lpm_counter0.bsf

Figure 7.14 Click OK

7. Complete the *stopwatch* circuit as shown in Figure 7.15. Click *File > Save*.



Figure 7.15 Complete stopwatch circuit

Input pin name: clk clk_en and clr

Output pins names: tenmina, tenminb, tenminc, tenmind, tenmine, tenminf and tenming mina, minb, minc, mind, mine, minf and ming tenseca, tensecb, tensecc, tensecd, tensece, tensecf and tensecg seca, secb, secc, secd, sece, secf and secg

8. Pin Assignment

You can import pin assignments by choosing *Assignments > Import Assignments*. This opens the dialogue in Figure 7.16 to select the file to import.

\$\$\$\$	
K Quartus II - /DIPLOMA/Year2/EG2163/g8_1/digital/stopwatch/	stopwatch - stopwa
File Edit View Project Assignments Processing Tools Window	<u>H</u> elp
🗋 🖻 🖨 🗿 🎒 🐰 🏆 Device	- 3
Project Navigator Image: Section	
Tasks Import Assignments Flow: Early Timing Estime Task ⊑' Signment (Time) Groups ? Analysis & Design Partition B Flow: Partition Signment (Time) Groups Partition Signment (Time) Groups Partition Sign Closure Floorplan B LogicLock Regions Window Alt+L P Fitter (Place & Route) ? Fitter (Place & Route) ? Classic Timing Analysis	
X Type Message	

Figure 7.16 Importing the pin assignments

Browse to select the desired file *stopwatch.csv*. Click *Open*.

::::: inst6 clk q3 clk q3 clk q2 clk qq q q2 clk q2	Sel	lect File	OUTPUT seca		×
Import Assignments Specify the source and categories of assignments to import		ook in: 🔄 stopwa	tch 💽	1 🗟 凿	
File name:	ories	incremental_db stopwatch.csv			
Copy existing assignments into stopwatch.qsf.bak before importing	nced	ij stopwatch.qsf			
OKCar					
	File	e <u>n</u> ame: stopwa	atch		<u>O</u> pen
pwatch -c stopwatchtiming_analysis_only	File	es of type: Import	Files (*.qsf;*.esf;*.acf;*.csv;*.txt	;*.sdc) 💌 🔤	Cancel

Figure 7.17 Select stopwatch.csv

Click **OK** to confirm pins assignments file *stopwatch.csv*.



Figure 7.18 Confirm pin assignments file stopwatch.csv

9. Compile the circuit with pin assignments as shown in Figure 7.19 and ensure no error (Ignore warning/s).



Figure 7.19 Compile the complete stopwatch circuit with pin assignments

10. Programming and Configuring the FPGA Device

Select *Tools > Programmer* as shown in Figure 7.20.

0 C								
♥ Quartus II - /DIPLOMA/Year2/EG2163/g8_1/dig ♥ Quartus II - /DIPLOMA/Year2/EG2163/g8_1/dig ♥ Elle Elle Edit View Project Assignments Processing ● ● ※ ● ● sto Project Navigator ●	gital/stopwatch/stopwatch - stopwatch - [s Tools Window Help Run EDA Simulation Tool Run EDA Timing Analysis Tool Launch EDA Simulation Library Compiler Launch Design Space Explorer ImmeQuest Timing Analyzer Advisors Planner (Floorplan and Chip Editor)							
Ipm_counter0.qip Stopwatch.cs∨ Hierarchy Files	Q Design Partition Planner Netlist ⊻iewers SignalTap II Logic Analyzer In-System Memory Content Editor Logic Analyzer Interface Editor In-System Sources and Probes Editor SignalProbe Pins Programmer							
Task ☑ ✓ ► Analysis & Synthesis ● Partition Merge ● Early Timing Estimate with Syr ✓ ● Fitter (Place & Route) ✓ ● Classic Timing Analysis	MegaWizard Plug-In Manager SOPC Builder Tol Scripts Customize Options License Setup							
Image: A state of the state	Customize Block Editor Options for Block Editor							

Figure 7.20 Programmer tools

It is necessary to specify the programming hardware (**USB Blaster**) and the mode (**JTAG**) that should be used. If it is not automatically detected, Click the *Hardware Setup* button and select the *USB-Blaster* in the pop-up window and select **JTAG** in the Mode box as shown in Figure 7.21 and Figure 7.22.

6640	\$						¢) 🔍 A	pplication	ns Plac	ces Sy	vstem
💾 Quartus II - /DI	PLOMA/Year2/EG21	63/g8_1/digital/stopw	atch/stopwate	ch - stopwatch	- [stopwatch.	cdf]						
<u>File E</u> dit P <u>r</u> ocessir	ng <u>T</u> ools <u>W</u> indow											
🔔 Hardware Setup	No Hardware										М	ode: JTAG 💌
Enable real-time I	SP to allow background p	rogramming (for MAX II dev	rices)									
尾 Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP	
📫 Stop	stopwatch.sof	EP2C20F484	001B6696	FFFFFFF								
Auto Detect			-									
X Delete			Hardwar	e Setup							×	
Add File			Hardwa	re Settings JTA	G Settings							
			Select	a programming h	ardware setup t	o use when	n programi	ming device	es. This prog	ramming		
Change File				are setup applies	only to the cart	ant program		ow.				
Save File			Currer	itly selected hardv	ware: USB	-Blaster (US	5B 5-1.2]					
Add Device				ilable hardware ite	ems:		1					
🕇 Up			US US	ardware iB-Blaster	Lo	erver ocal	USB	5-1.2		1ardware		
🔑 Down									Remov	ve Hardwa	re	
										CI	lose	

Figure 7.21 If Hardware Setup not detected automatically

8 \$\$	4						!	🙈 🙈 A	pplicatio	ns Pla	ces Sy	stem		
uartus II - /DIPLOMA/Year2/EG2163/g8_1/digital/stopwatch/stopwatch - stopwatch - [stopwatch.cdf]														
<u>File E</u> dit P <u>r</u> ocessir	ng <u>T</u> ools <u>W</u> indow													
🔔 Hardware Setup	etup USB-Blaster [USB 5-1.2]										М	ode: JTAG		-
Enable reaktime ISP to allow background programming (for MAX II devices)														
🏴 Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP			
Stop	stopwatch.sof	EP2C20F484	001B6696	FFFFFFF	Y									
🙀 Auto Detect														
X Delete														
🍰 Add File														
🕒 Change File														
💾 Save File														
😂 Add Device														
🔁 Up														
Down														

Figure 7.22 Correct Hardware Setup window

Click *Start*. Having downloaded the configuration data into the FPGA device, you can now test the implemented circuit. If you need to make change/s to the design, first close the Programmer window. Then make the desired change/s, compile and reprogram the board. Repeat the process until you obtain the desired results.