Lab 7: Implementation of Digital Stop Watch on Altera DE1 Board

Objective:

* To implement Digital Stop Watch design on Altera DE1 board

Open Stop Watch Project - *stopwatch*

1. Open *counter0to9* circuit and include a *clr* pin as shown in Figure 7.1.

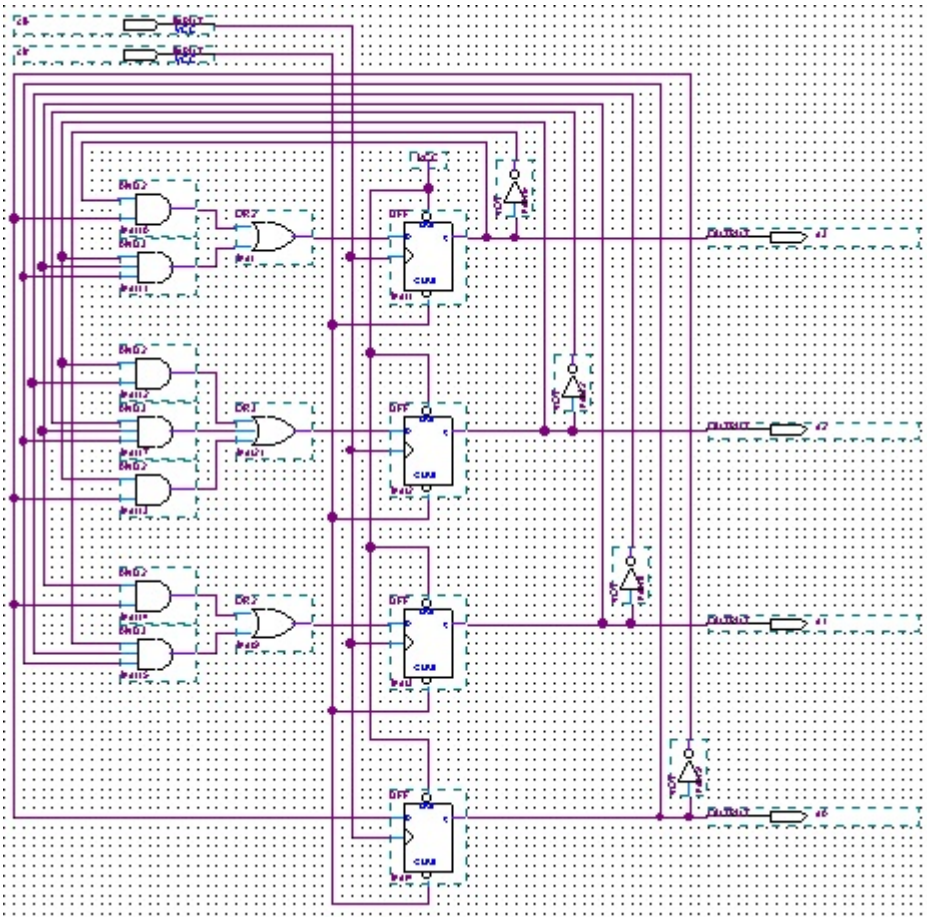

Figure 7.1 *counter0to9* circuit with *clr* pin

Input pin name: clk and clr

Output pins names: q3, q2, q1 and q0

2. Create a new symbol for *counter0to9* as shown in Figure 7.2. Overwrite the old symbol.

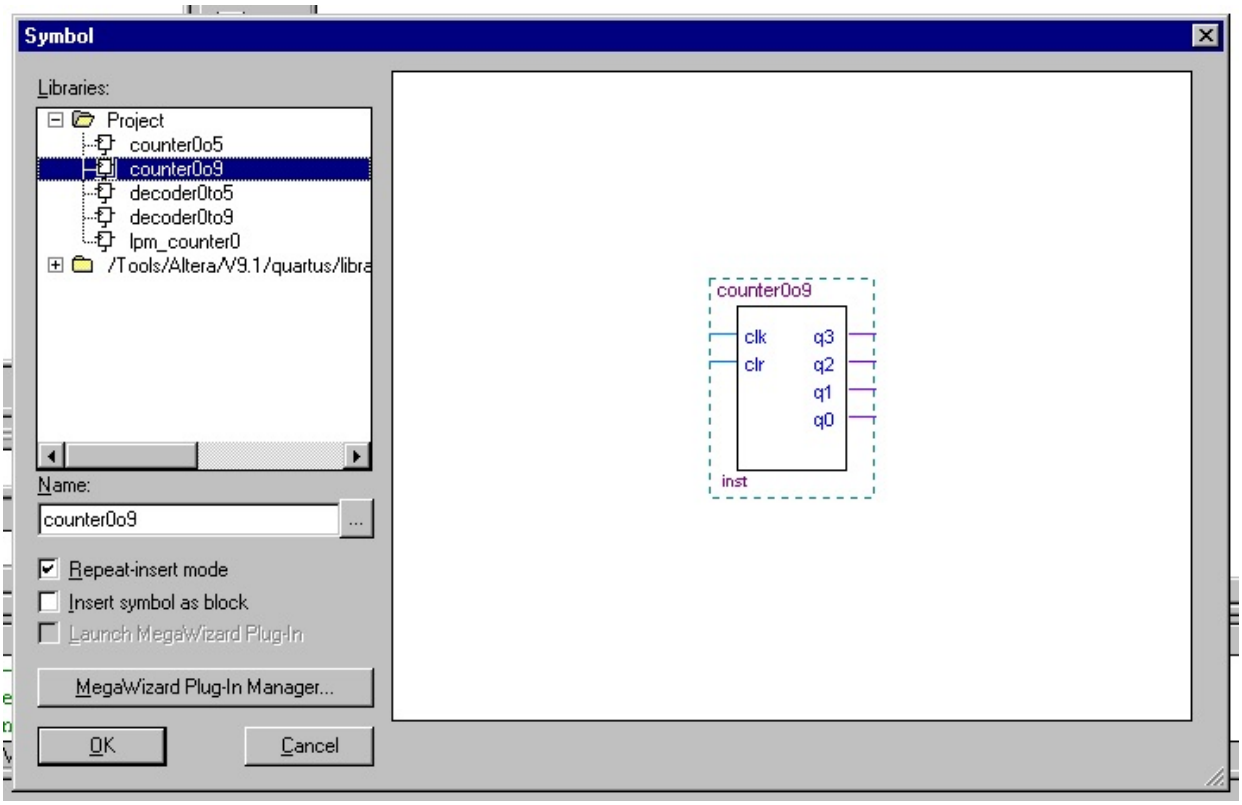

Figure 7.2 *counter0to9* symbol with *clr*

3. Open *counter0to5* circuit and include a *clr* pin as shown in Figure 7.3.

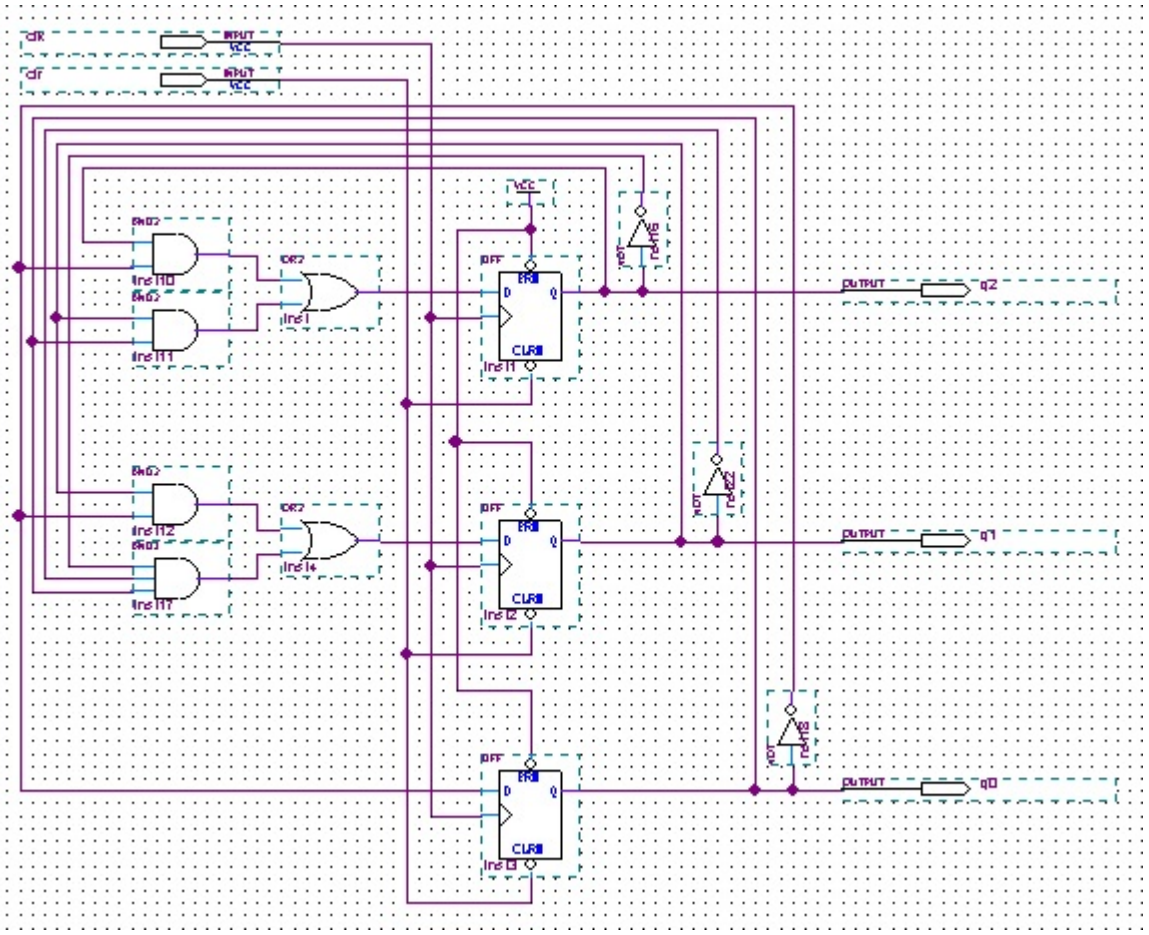

Figure 7.3 *counter0to5* circuit with *clr* pin

Input pin name: clk and clr

Output pins names: q2, q1 and q0

4. Create a new symbol for *counter0to5* as shown in Figure 7.4. Overwrite the old symbol.

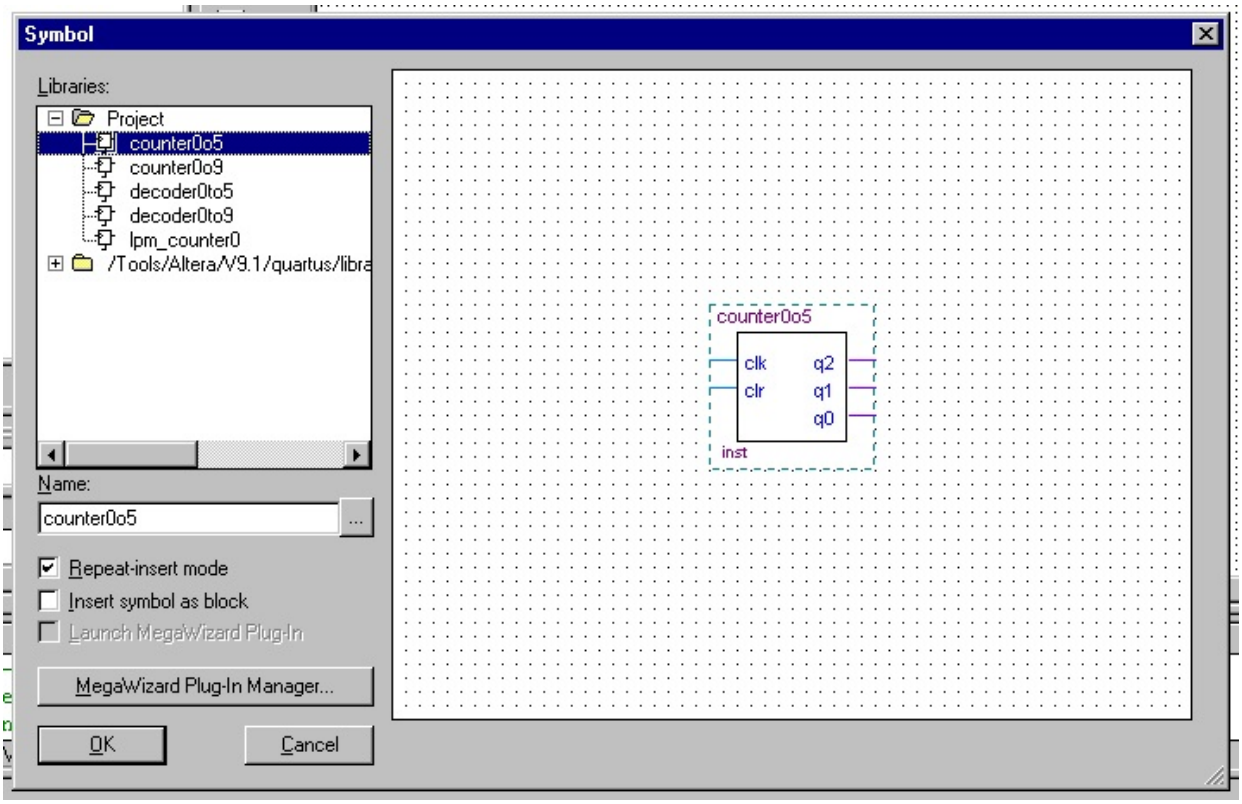

Figure 7.4 *counter0to5* symbol with clr

5. Select and delete the *lpm_counter* symbol (modulus count = 50,000,000) on the *stopwatch* circuit.

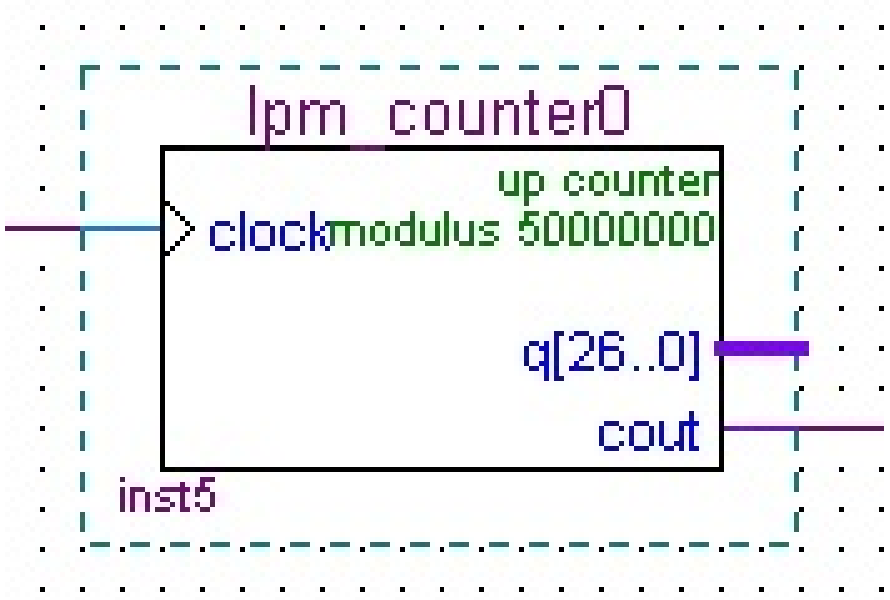

Figure 7.5 Delete *lpm_counter* symbol with modulus count = 50,000,000

6. Recreate the *lpm_counter* symbol with modulus count = 5,000,000.

Double-click on the blank space in the Graphic Editor window, or Click on the Symbol Tool icon  in the toolbar. A pop-up box in Figure 7.6 will appear. Type lpm_counter in the search bar to locate the symbol and Click ***OK***.

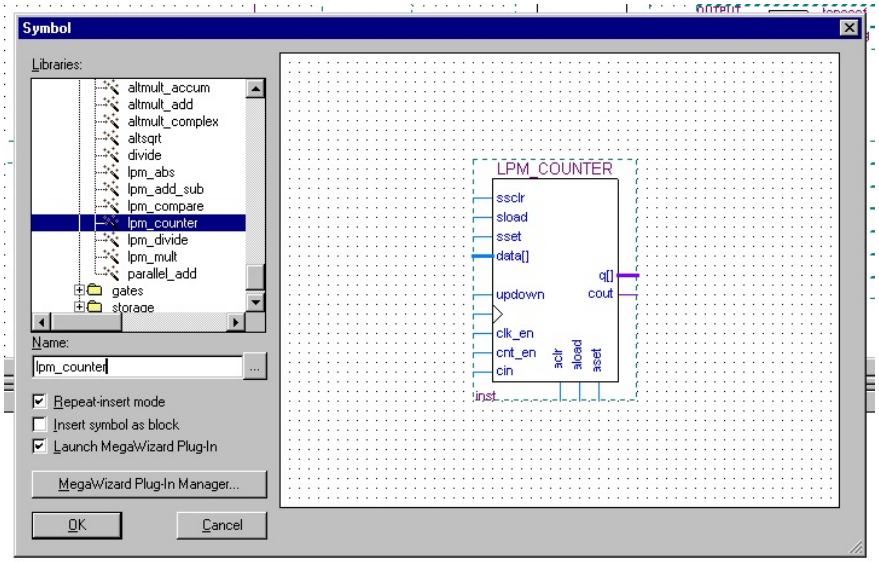

Figure 7.6 Choose *lpm_counter* from the library

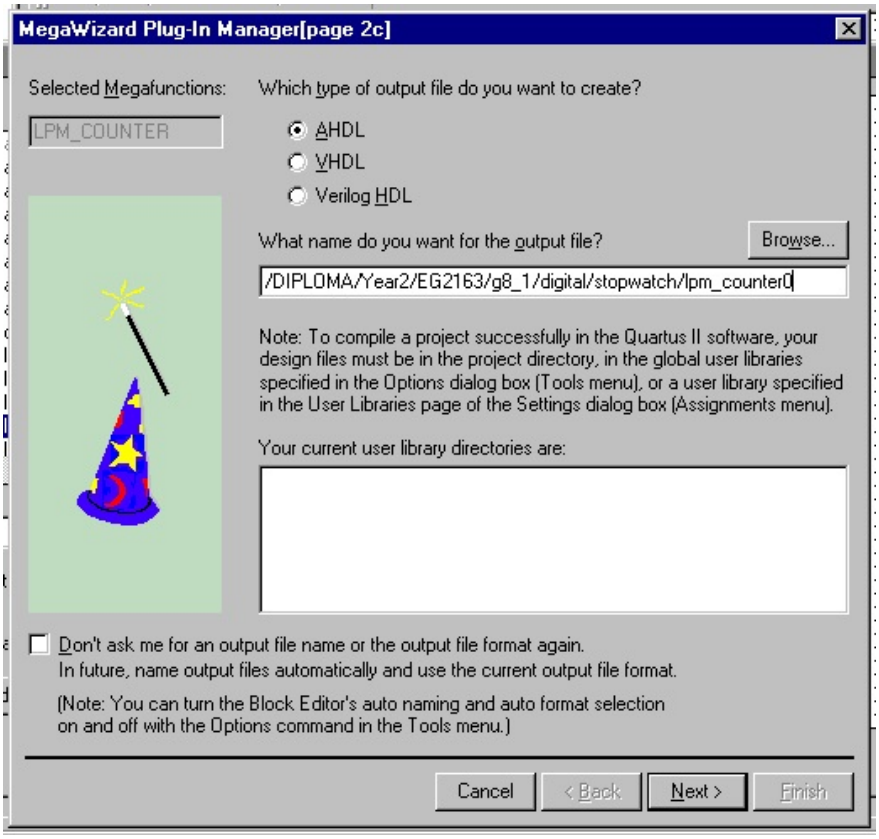

Figure 7.7 Change output file name from *lpm_counter1* to *lpm_counter0*

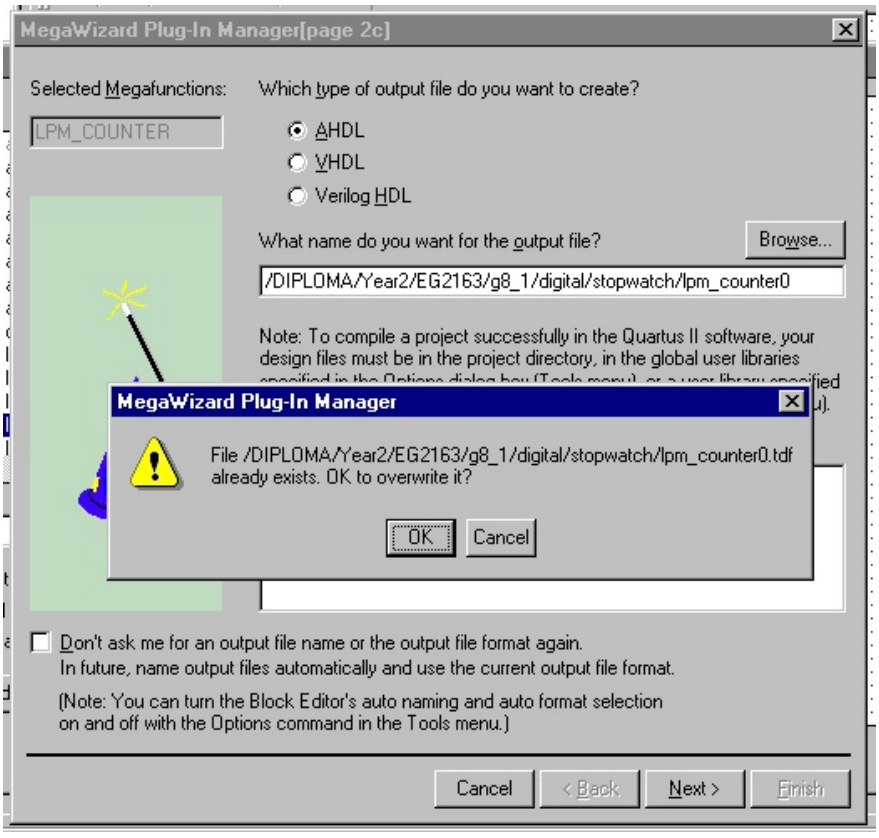

Figure 7.8 Click ***OK*** to overwrite

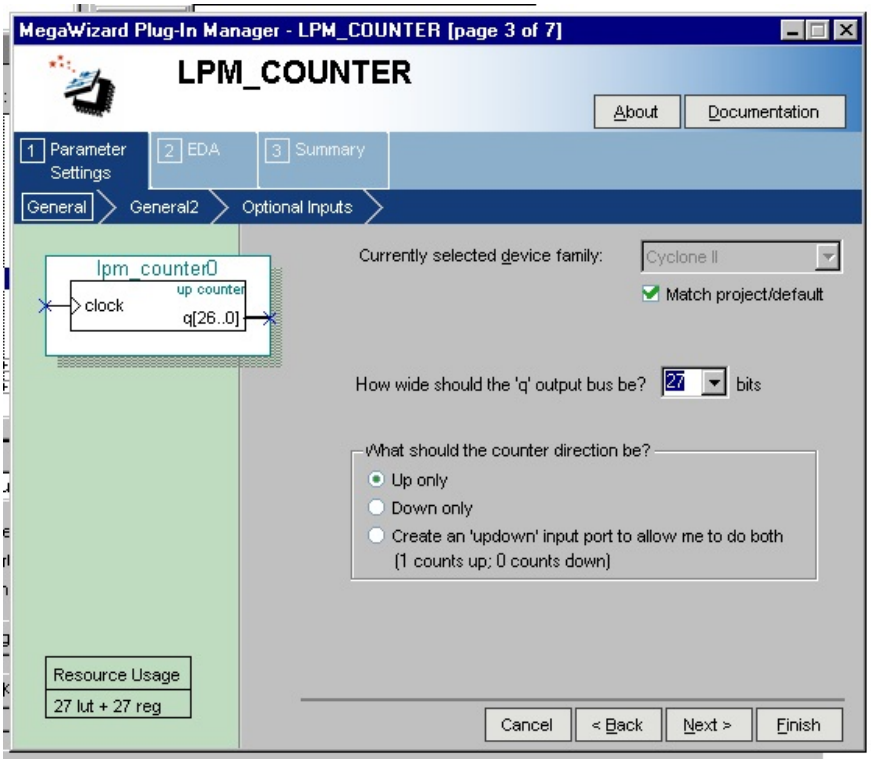

Figure 7.9 2^26 = 67,108,864 => Wide of ‘q’ output bus: 27 bits Click ***Next***

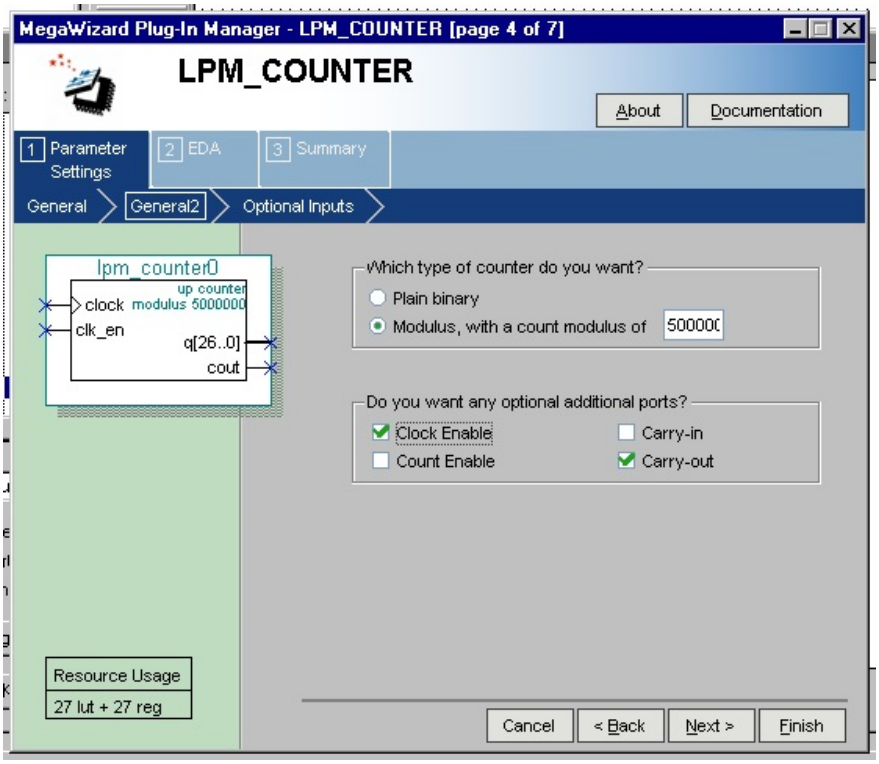

Figure 7.10 *Modulus* with count *5,000,000* with *Clock Enable* and *Carry-out* ports Click ***Next***

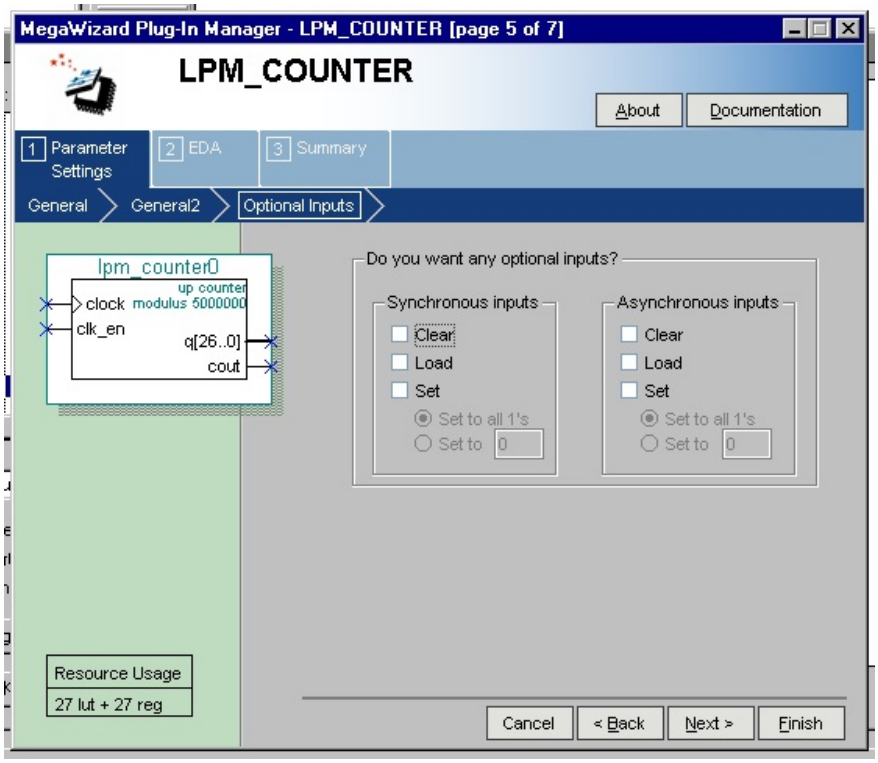

Figure 7.11 Click ***Next***

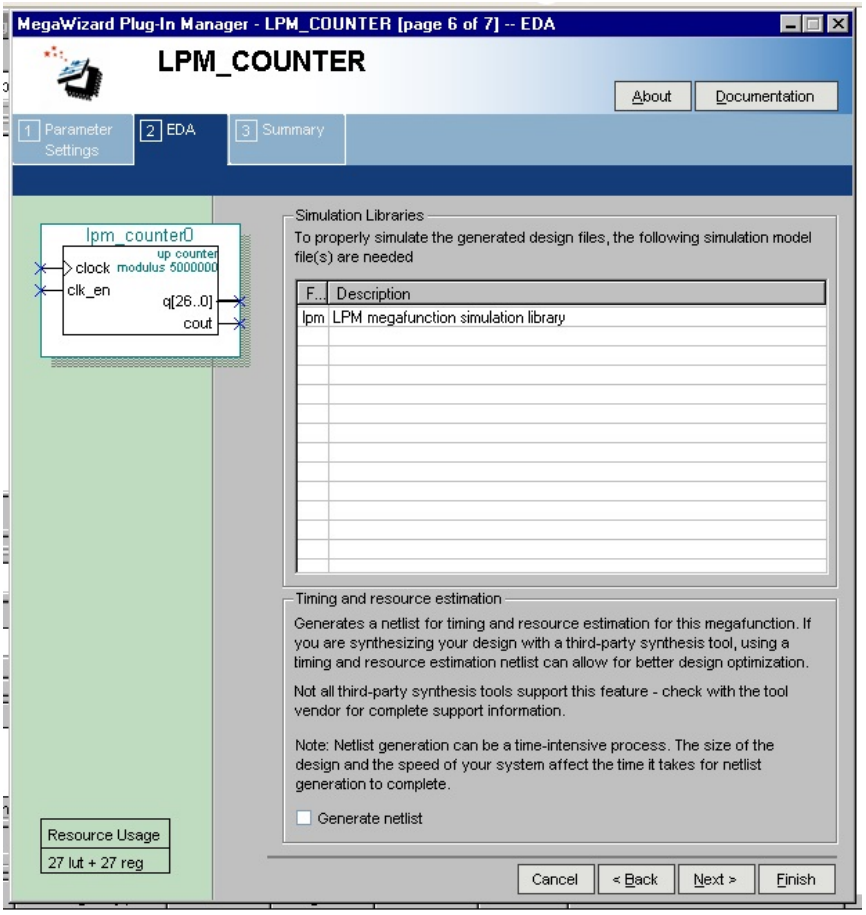

Figure 7.12 Click ***Next***

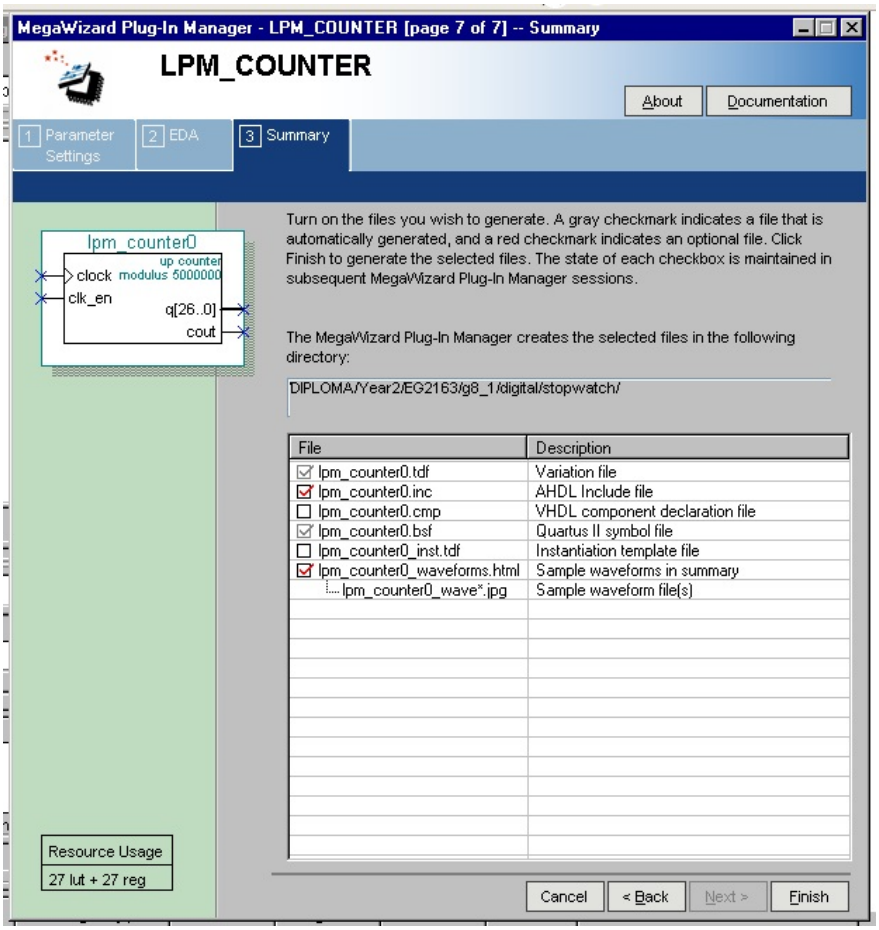

Figure 7.13 Click ***Finish***

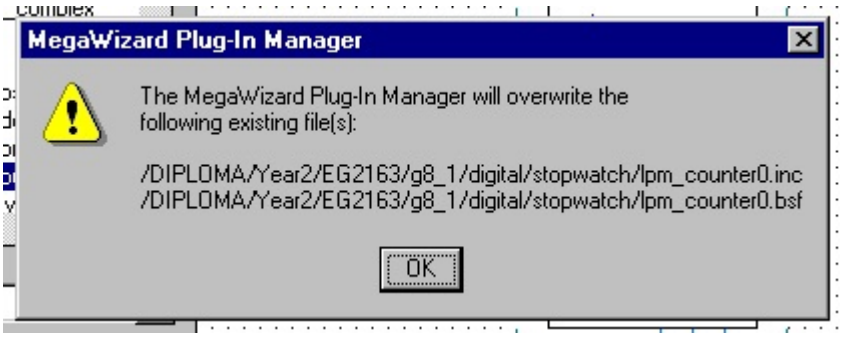

Figure 7.14 Click ***OK***

7. Complete the *stopwatch* circuit as shown in Figure 7.15. Click ***File*** > ***Save***.

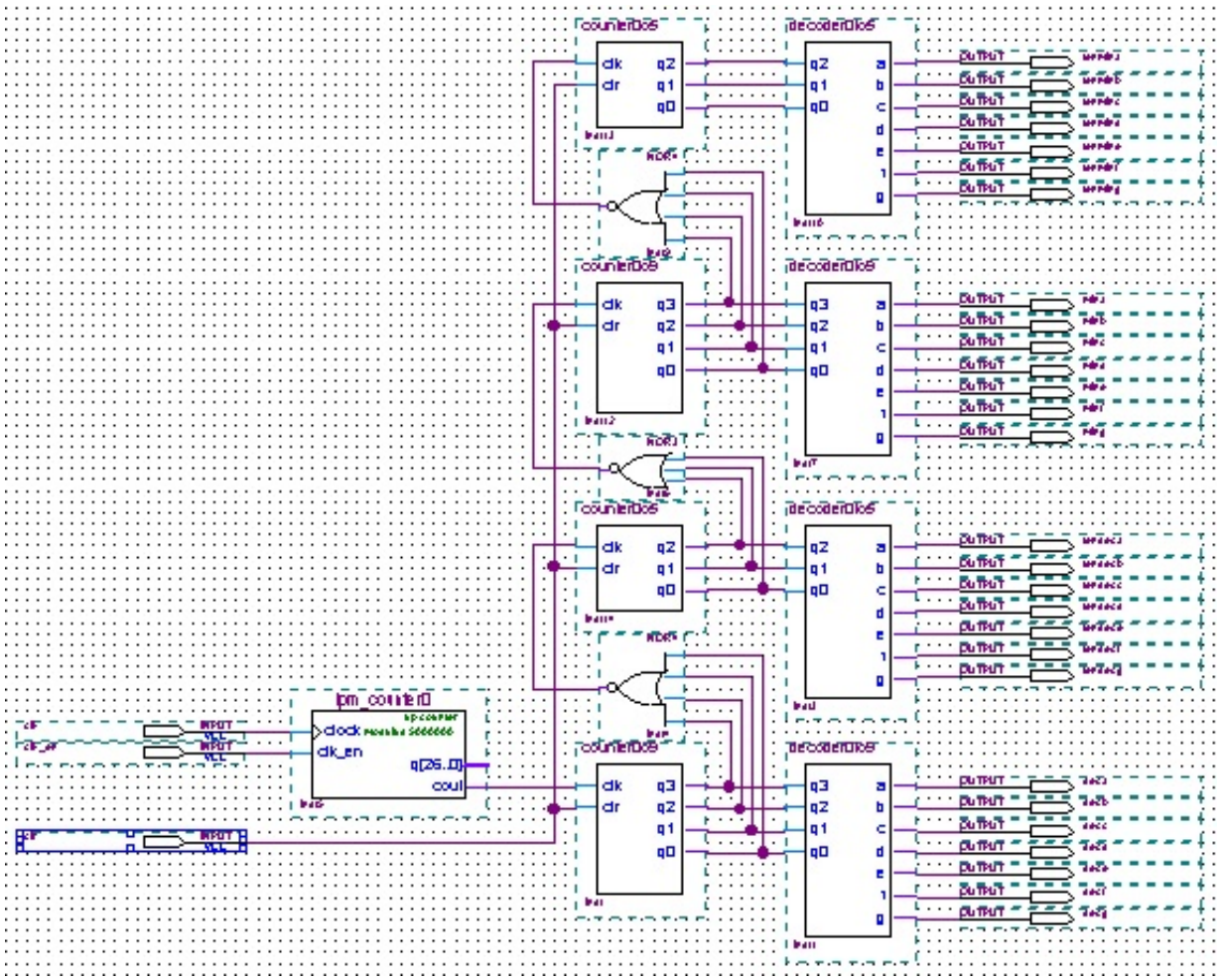

Figure 7.15 Complete stopwatch circuit

Input pin name: clk clk_en and clr

Output pins names: *tenmina, tenminb, tenminc, tenmind, tenmine, tenminf and tenming*
mina, minb, minc, mind, mine, minf and ming
tenseca, tensecb, tensecc, tensecd, tensece, tensecf and tensecg
seca, secb, secc, secd, sece, secf and secg

8. Pin Assignment

You can import pin assignments by choosing ***Assignments > Import Assignments***. This opens the dialogue in Figure 7.16 to select the file to import.

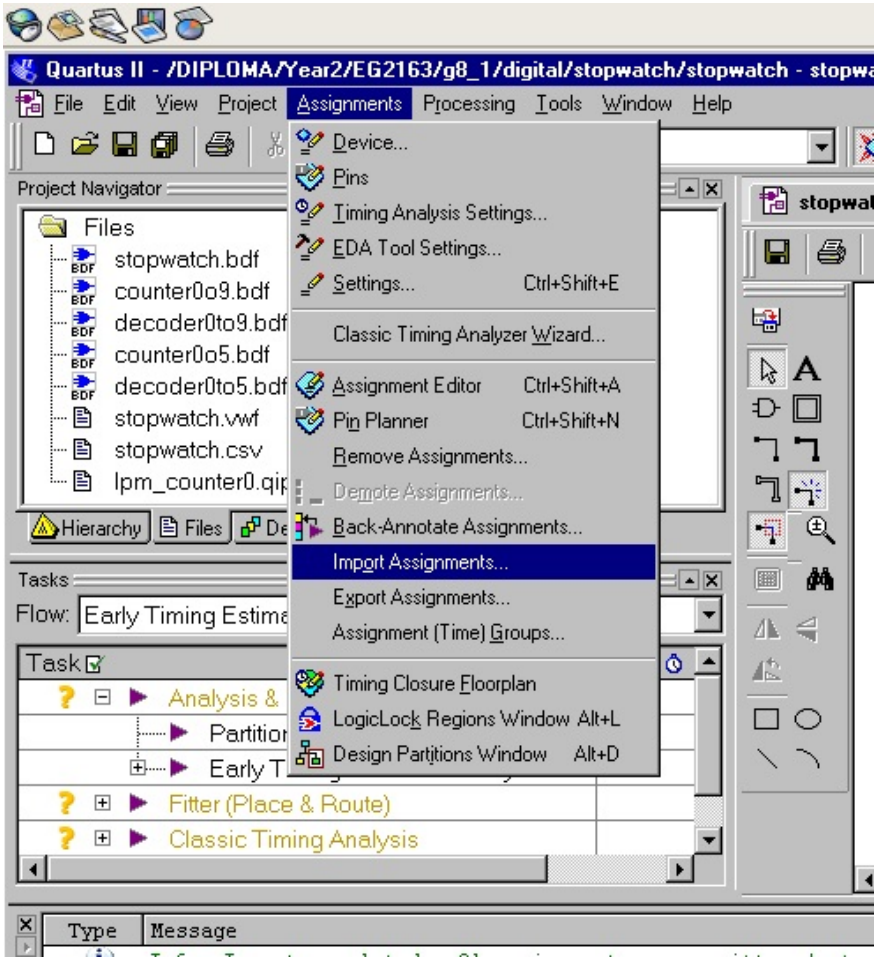

Figure 7.16 Importing the pin assignments

Browse to select the desired file *stopwatch.csv*. Click ***Open***.

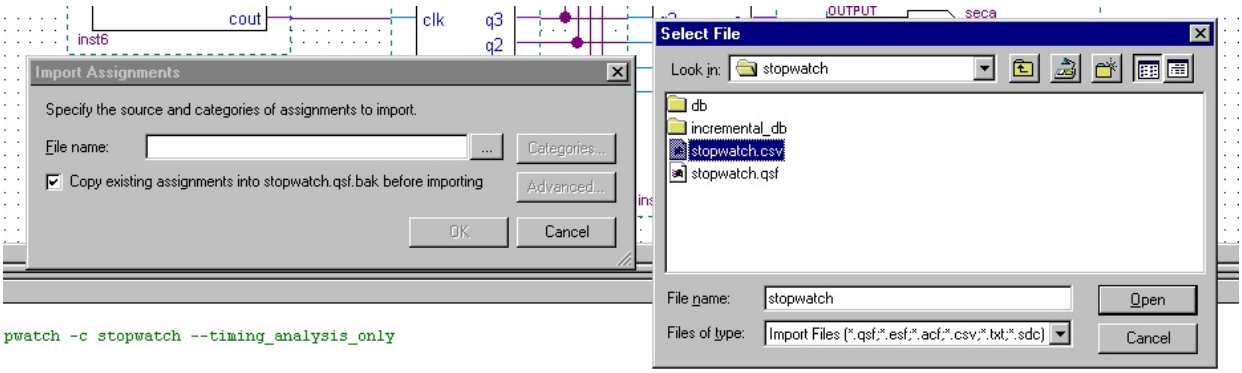

Figure 7.17 Select *stopwatch.csv*

Click ***OK*** to confirm pins assignments file *stopwatch.csv*.

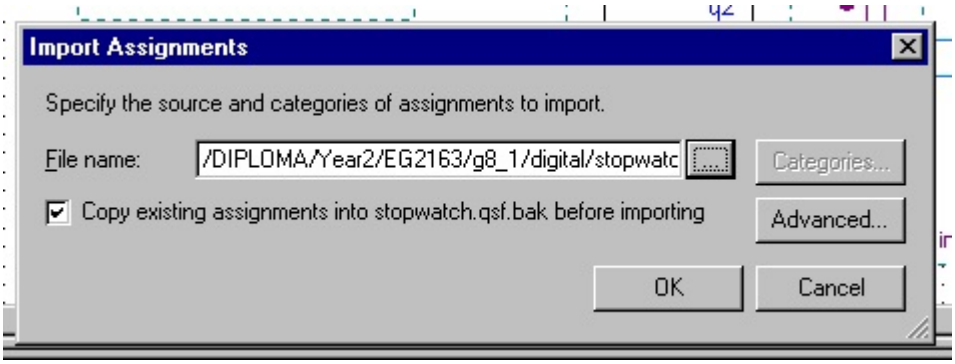

Figure 7.18 Confirm pin assignments file *stopwatch.csv*

9. Compile the circuit with pin assignments as shown in Figure 7.19 and ensure no error (Ignore warning/s).

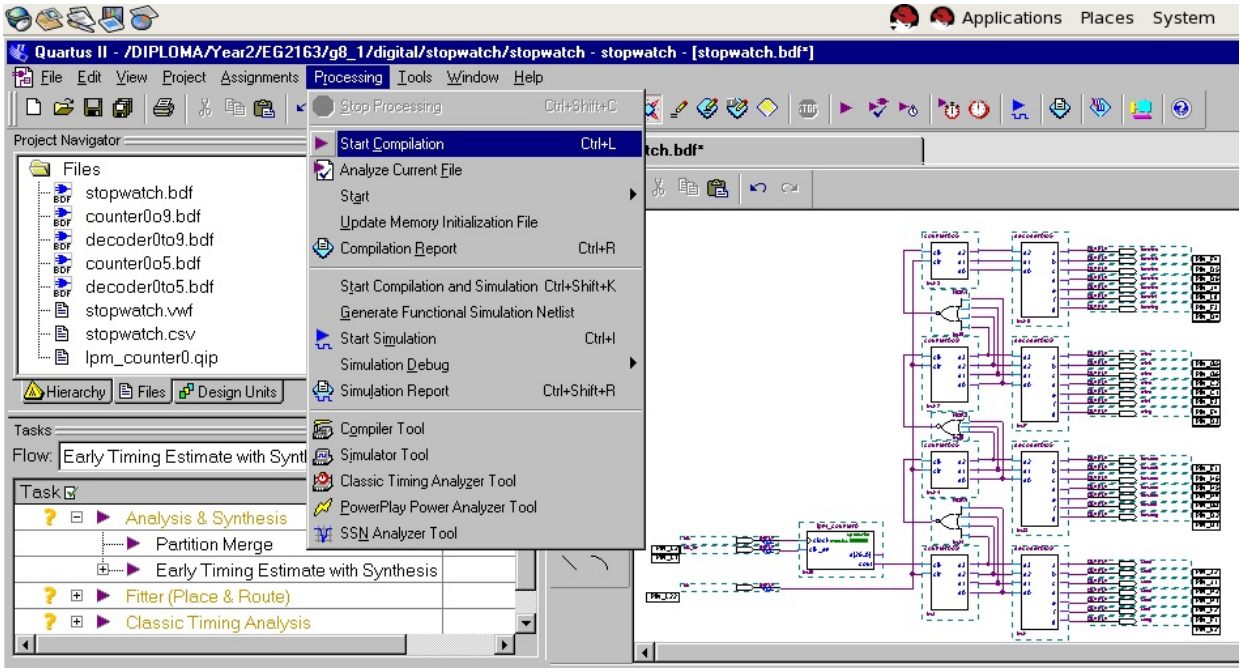

Figure 7.19 Compile the complete stopwatch circuit with pin assignments

10. Programming and Configuring the FPGA Device

Select ***Tools*** > ***Programmer*** as shown in Figure 7.20.

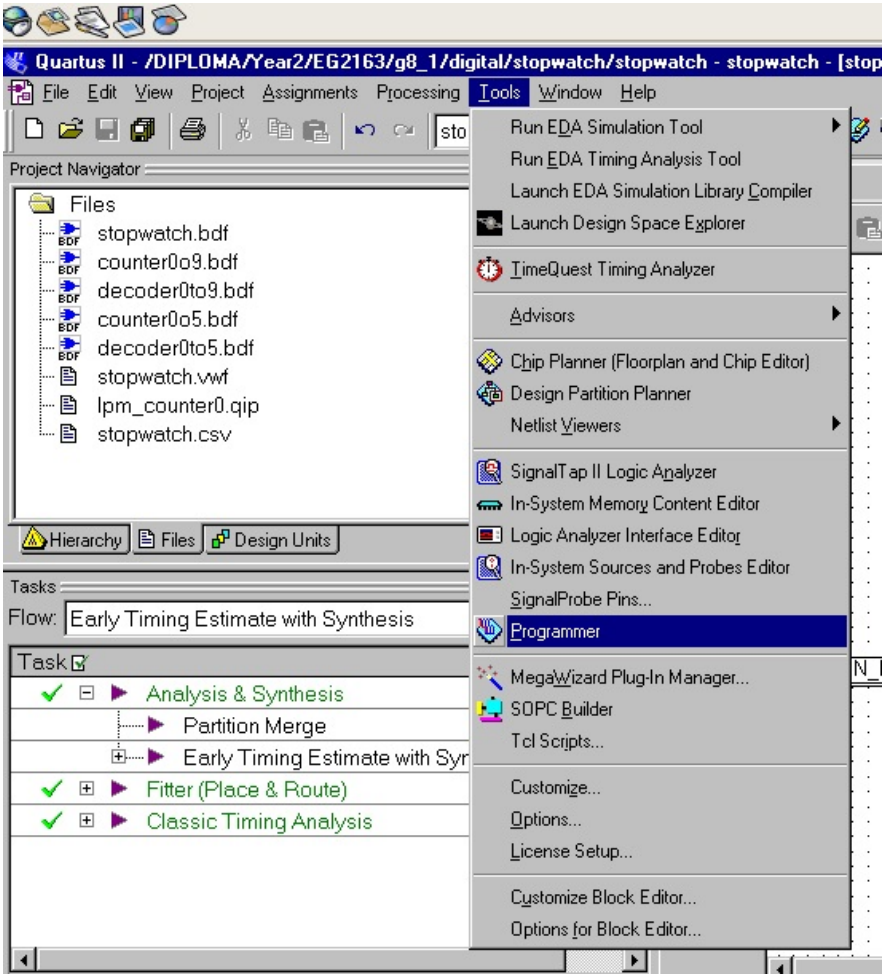

Figure 7.20 Programmer tools

It is necessary to specify the programming hardware (**USB Blaster**) and the mode (**JTAG**) that should be used. If it is not automatically detected, Click the *Hardware Setup* button and select the *USB-Blaster* in the pop-up window and select **JTAG** in the Mode box as shown in Figure 7.21 and Figure 7.22.

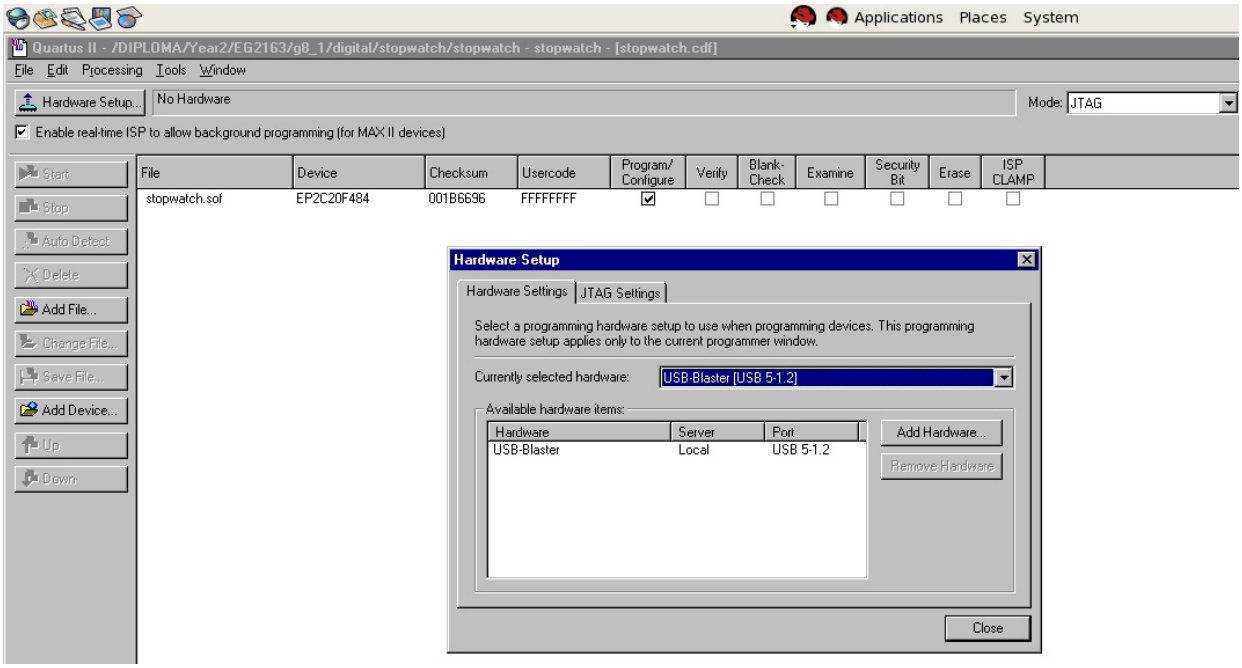

Figure 7.21 If Hardware Setup not detected automatically

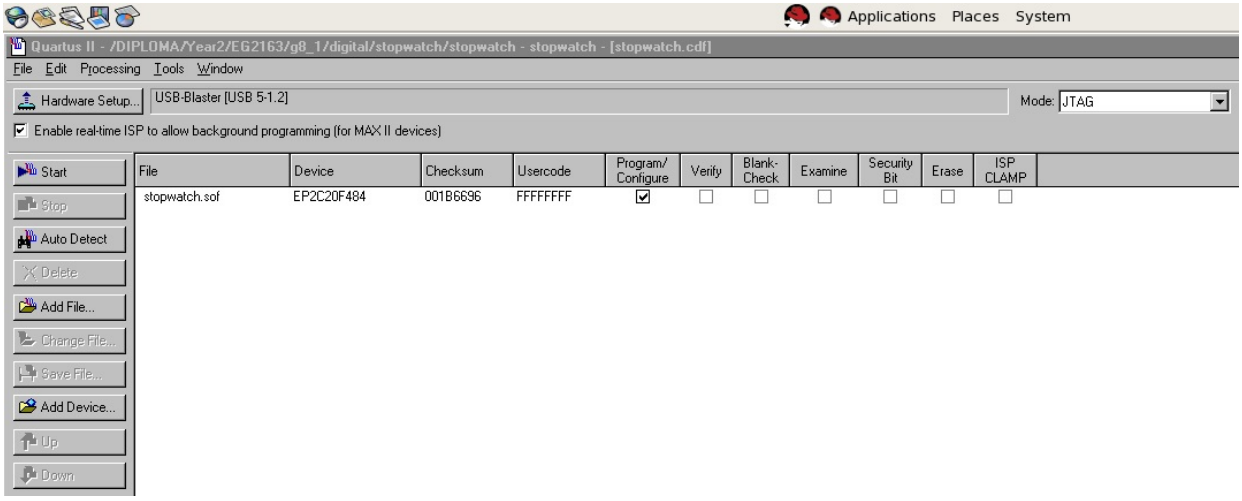

Figure 7.22 Correct Hardware Setup window

Click ***Start***. Having downloaded the configuration data into the FPGA device, you can now test the implemented circuit. If you need to make change/s to the design, first close the Programmer window. Then make the desired change/s, compile and reprogram the board. Repeat the process until you obtain the desired results.