## Lab 6: Design of Digital Stop Watch (*counter0to59, decoder0to59* and *lpm_counter*)

---

Objective:

* To design a Digital Stop Watch using concepts of digital system partitioning

---

**Digital Stop Watch – *counter0to59, decoder0to59* and *lpm_counter***

**Open *stopwatch.bdf* and connect the *counter0to5* to *counter0to9* as shown in Figure 6.1 to obtain 0 to 59 counting and decoding**

1. Connect ***counter0to5*** to ***counter0to9*** shown in Figure 6.1.

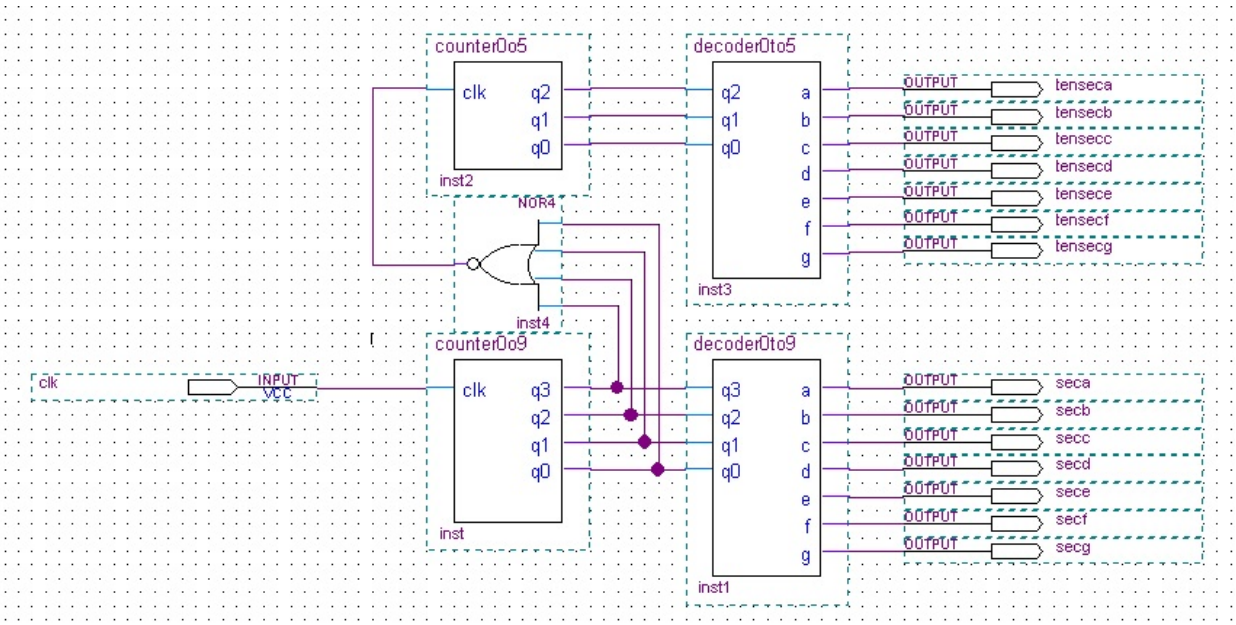


Figure 6.1 *stopwatch.bdf* with *counter0to5* connected to *counter0to9*

2. To add Symbol: Altera Megafunction lpm_counter

Double-click on the blank space in the Graphic Editor window, or Click on the Symbol Tool icon  in the toolbar. A pop-up box in Figure 6.2 will appear. Type lpm_counter in the search bar to locate the symbol and Click ***OK***.

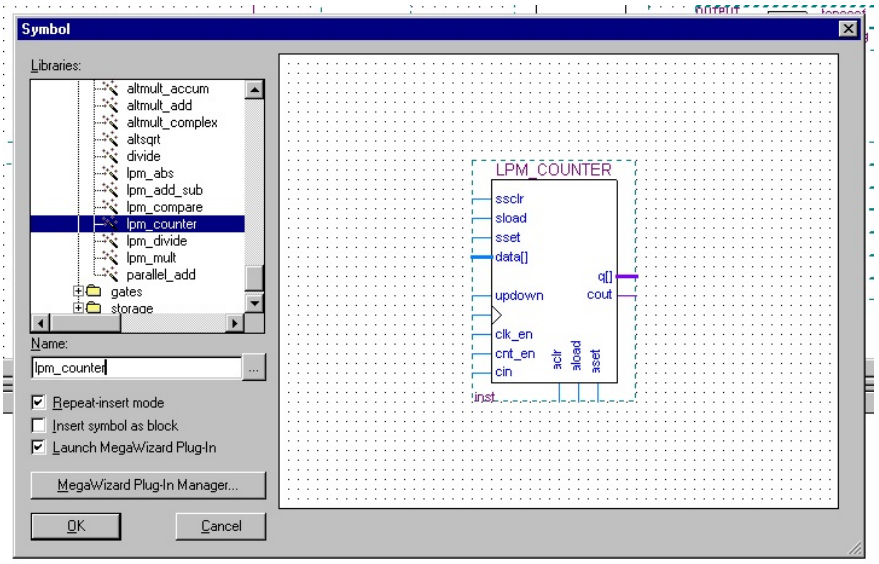


Figure 6.2 Choose *lpm_counter* from the library

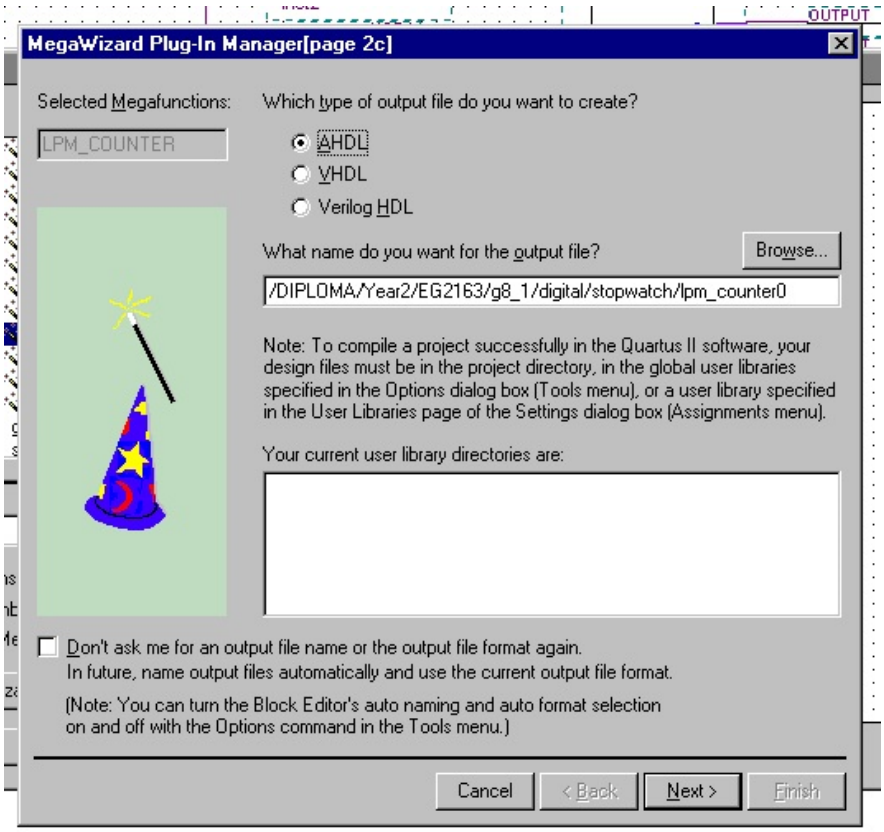


Figure 6.3 Type of output file: AHDL

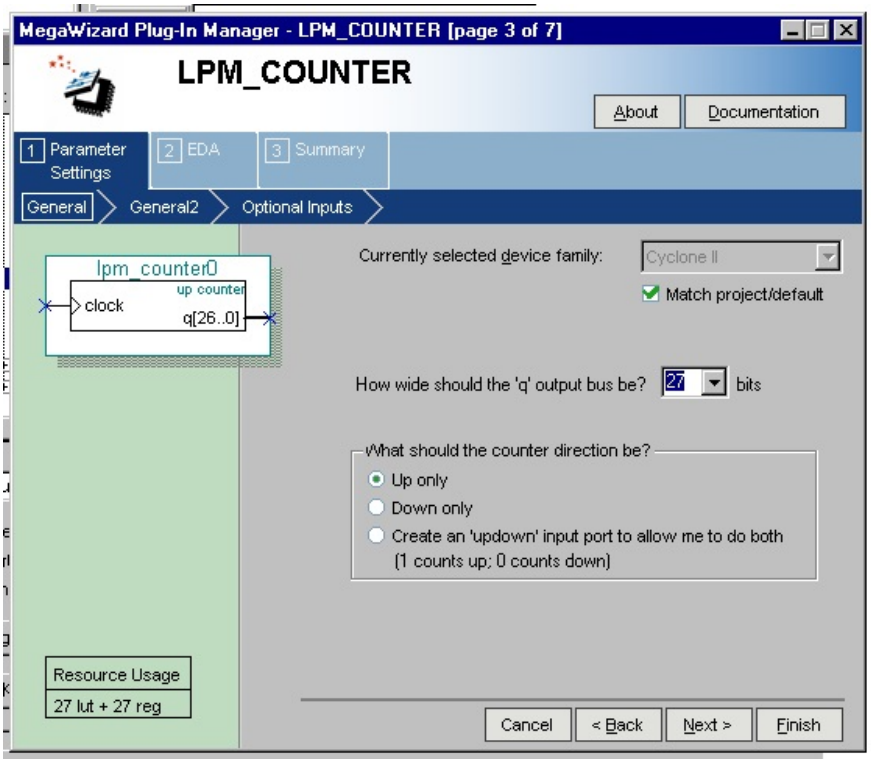


Figure 6.4 2^26 = 67,108,864 => Wide of ‘q’ output bus: 27 bits

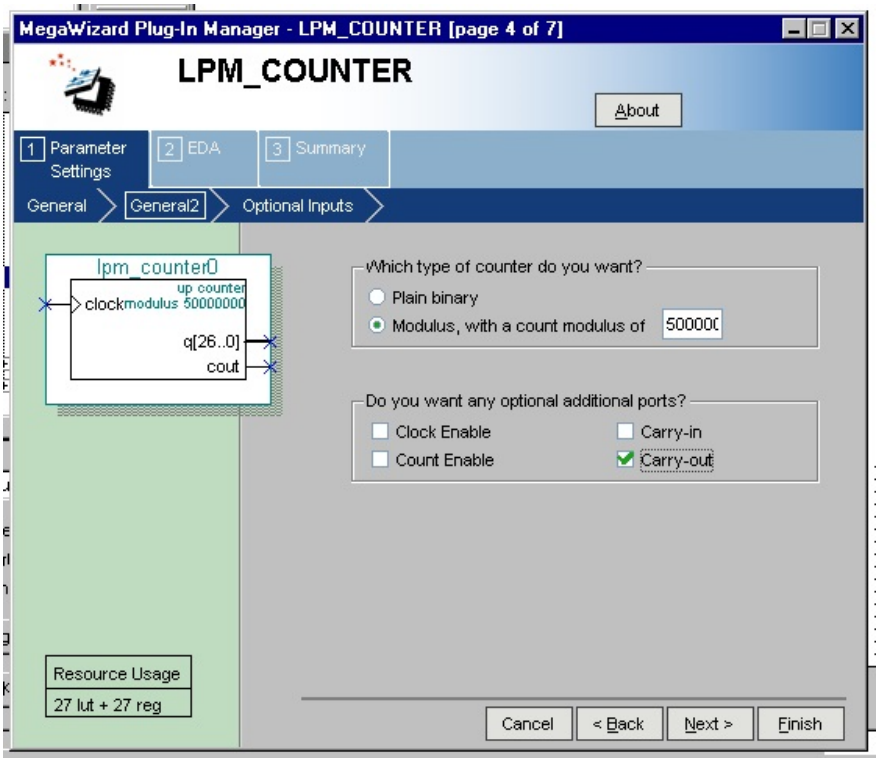


Figure 6.5 *Modulus* with count *50,000,000* and with *Carry-out* port

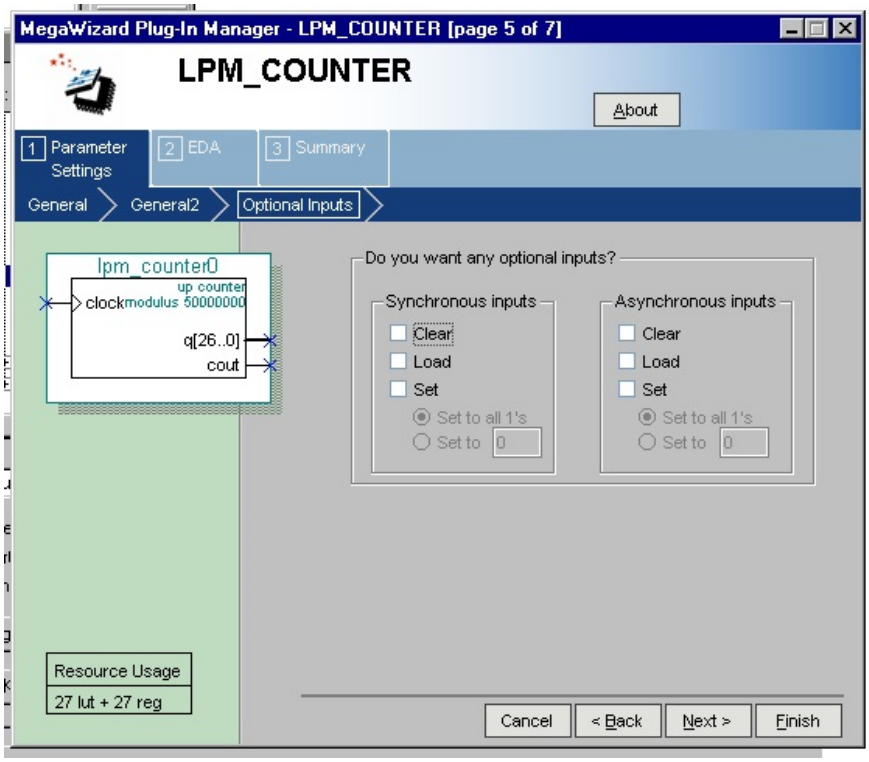


Figure 6.6 Click *Next*

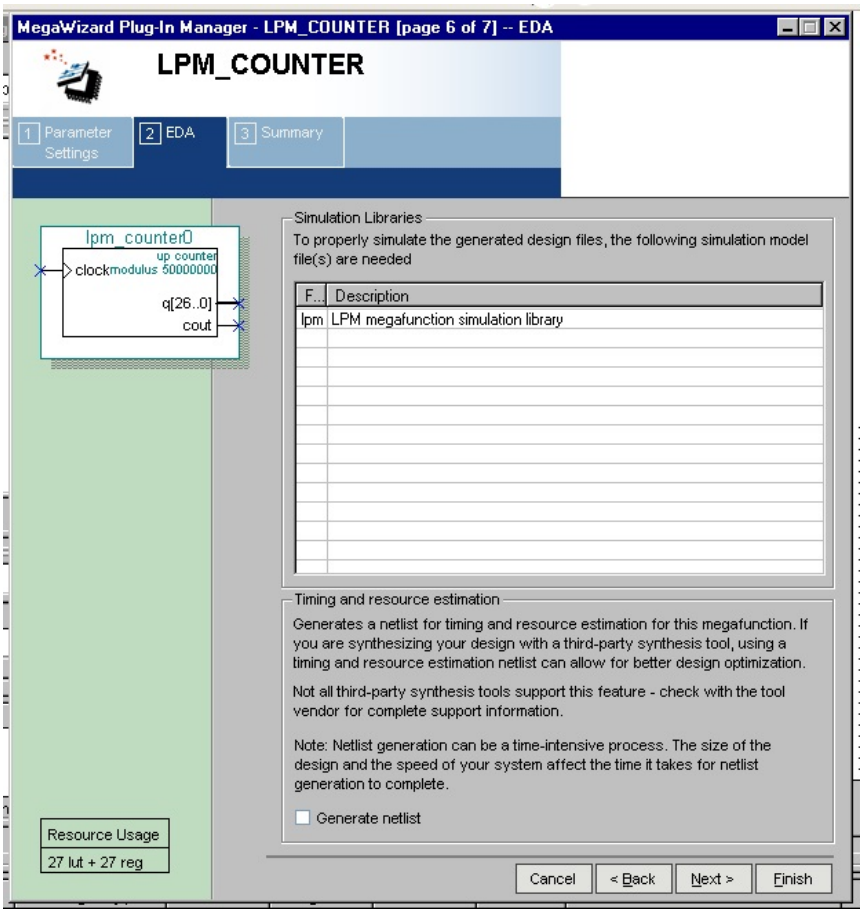


Figure 6.7 Click *Next*

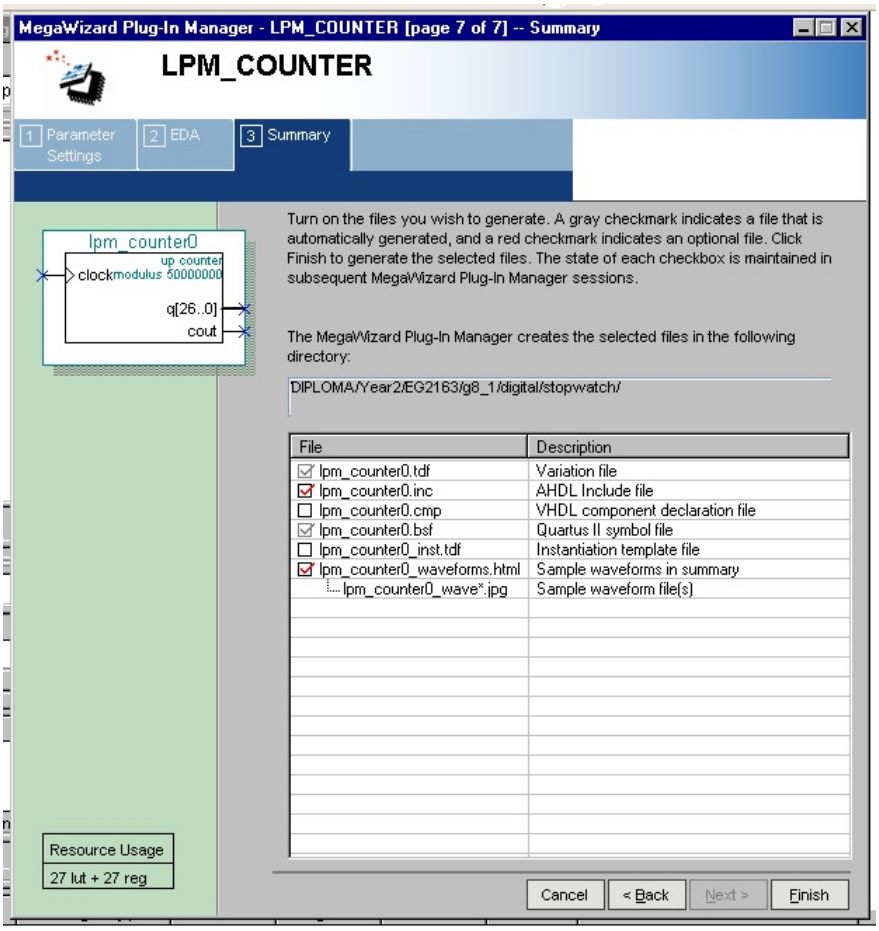


Figure 6.8 Click *Finish*


Figure 6.9 Click *Yes*

2. Complete the circuit with *lpm_counter* as shown in Figure 6.10. Click ***File*** > ***Save***.

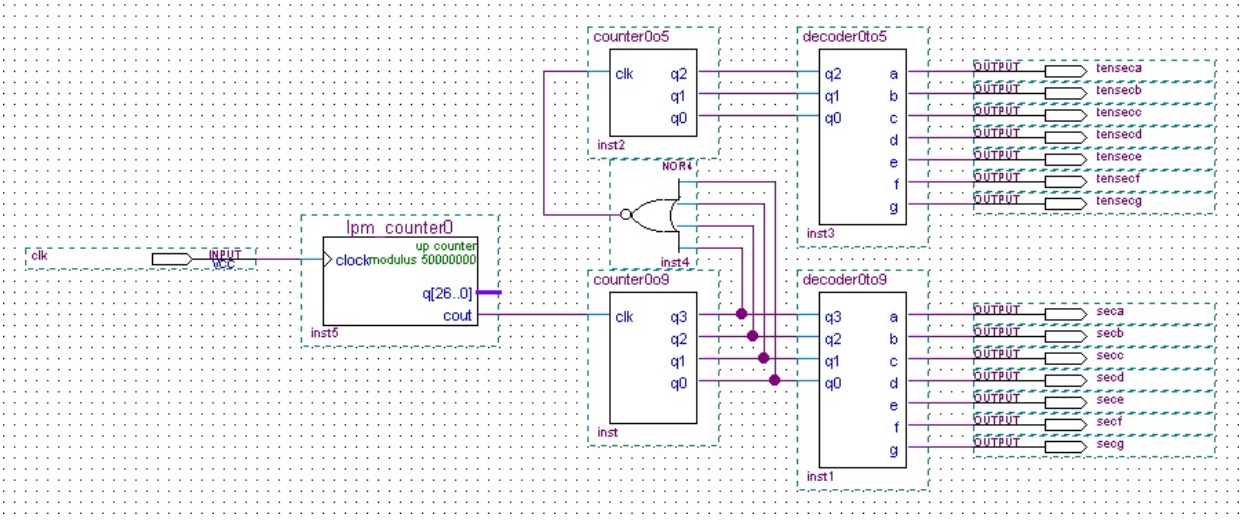


Figure 6.10 Circuit with *lpm_counter*

3. Pin Assignments

During previous compilations, the Quartus II Compiler was free to choose any pins on the selected FPGA to serve as inputs and outputs. However, the training board (DE1) has hardwired connections between the FPGA pins and the other components on the board. The DE1 board has fixed pin assignments. A useful Quartus II feature allows the user to import the pin assignments from a special file format (*.csv*). You can import pin assignments by choosing ***Assignments*** > ***Import Assignments***. This opens the dialogue in Figure 6.11 to select the file to import.

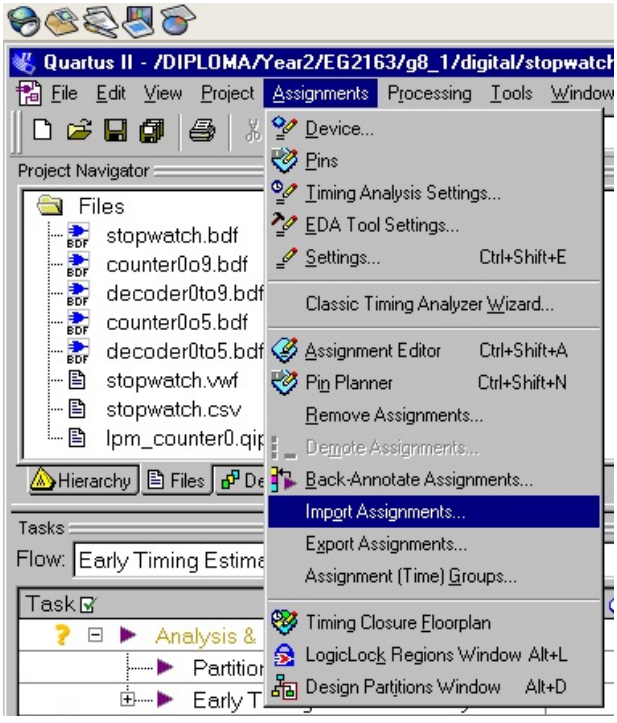


Figure 6.11 Importing the pin assignments

Browse to select the desired file *stopwatch.csv*. Click ***Open***.

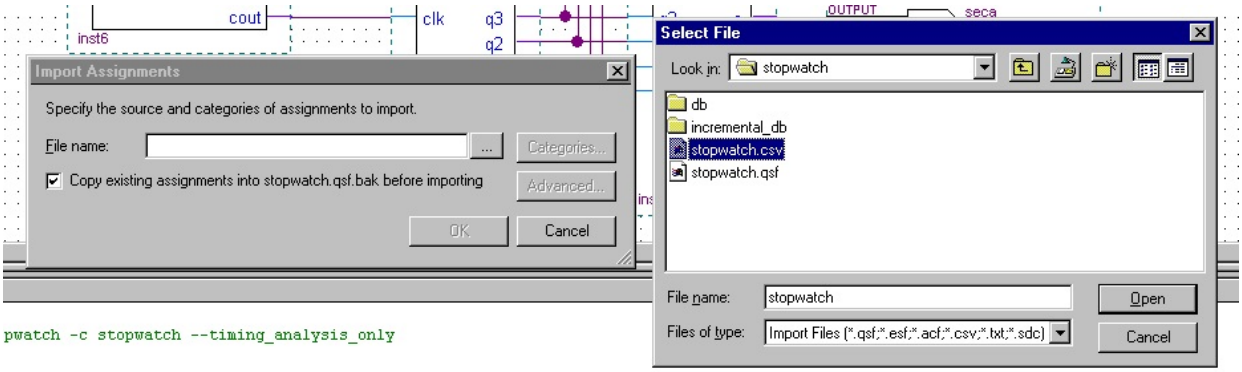


Figure 6.12 Select *stopwatch.csv*

Click ***OK*** to confirm pins assignments file *stopwatch.csv*.

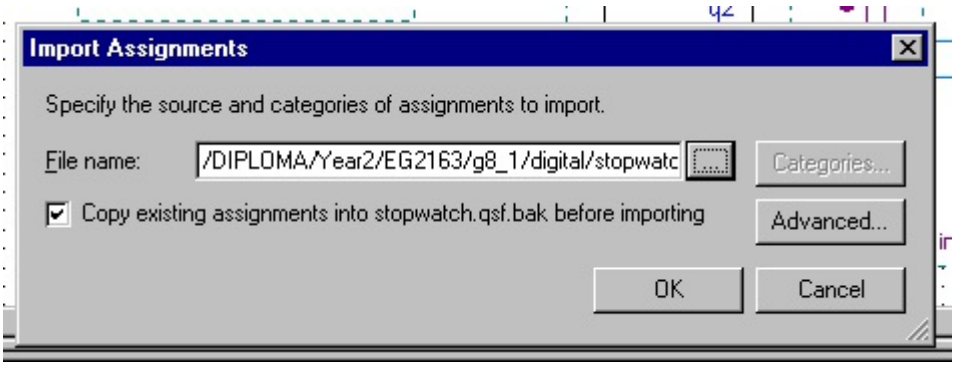


Figure 6.13 Confirm pin assignments file *stopwatch.csv*

4. Compile the circuit with pin assignments as shown in Figure 6.14 and ensure no error (Ignore warning/s).

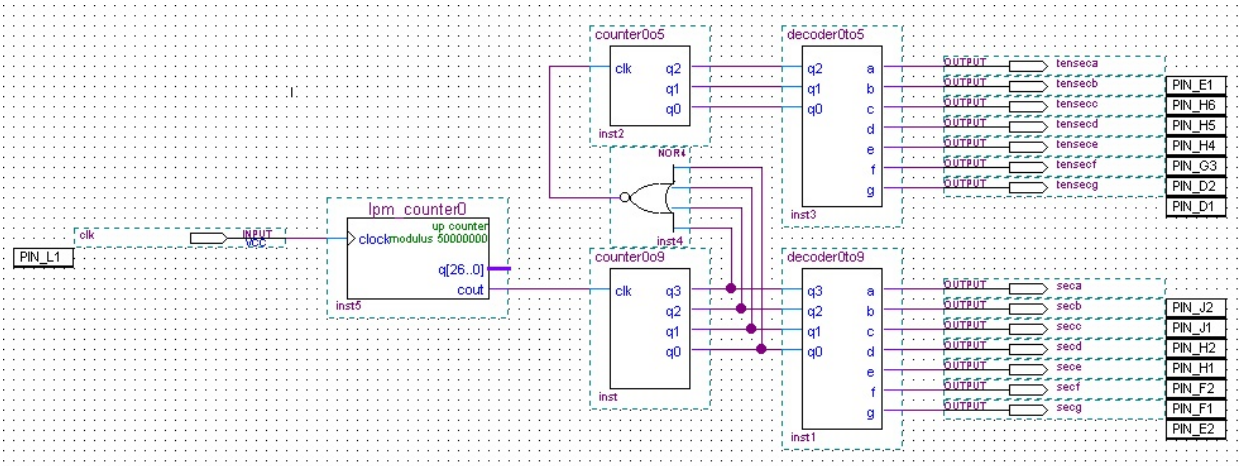


Figure 6.14 Compile the circuit with pin assignments

## 5. Programming and Configuring the FPGA Device

The FPGA device must be programmed and configured to implement the designed circuit. The required configuration file is generated by the Quartus II Compiler's Assembler module. Altera's DE1 board allows the configuration to be done in two different ways, known as **JTAG** (Joint Test Action Group) and **AS** (Active Serial) modes. The configuration data is transferred from the host computer (which runs the Quartus II software) to the board by means of a cable that connects a USB port on the host computer to the leftmost USB connector on the board. Before using the board, make sure that the USB cable is properly connected and turn on the power supply switch on the board.

The choice between the two modes is made by the **RUN/PROG** switch on the DE1 board. The **RUN** position selects the **JTAG** mode, while the **PROG** position selects the **AS** mode. In the **JTAG** mode, the configuration data is loaded directly into the FPGA device. JTAG defined a simple way for testing digital circuits and loading data into them, which became an IEEE standard. FPGA configured by JTAG will retain its configuration as long as the power remains turned on. The configuration information is lost when the power is turned off.

Here we set JTAG programming. Select ***Tools*** **>** ***Programmer*** as shown in Figure 6.15.

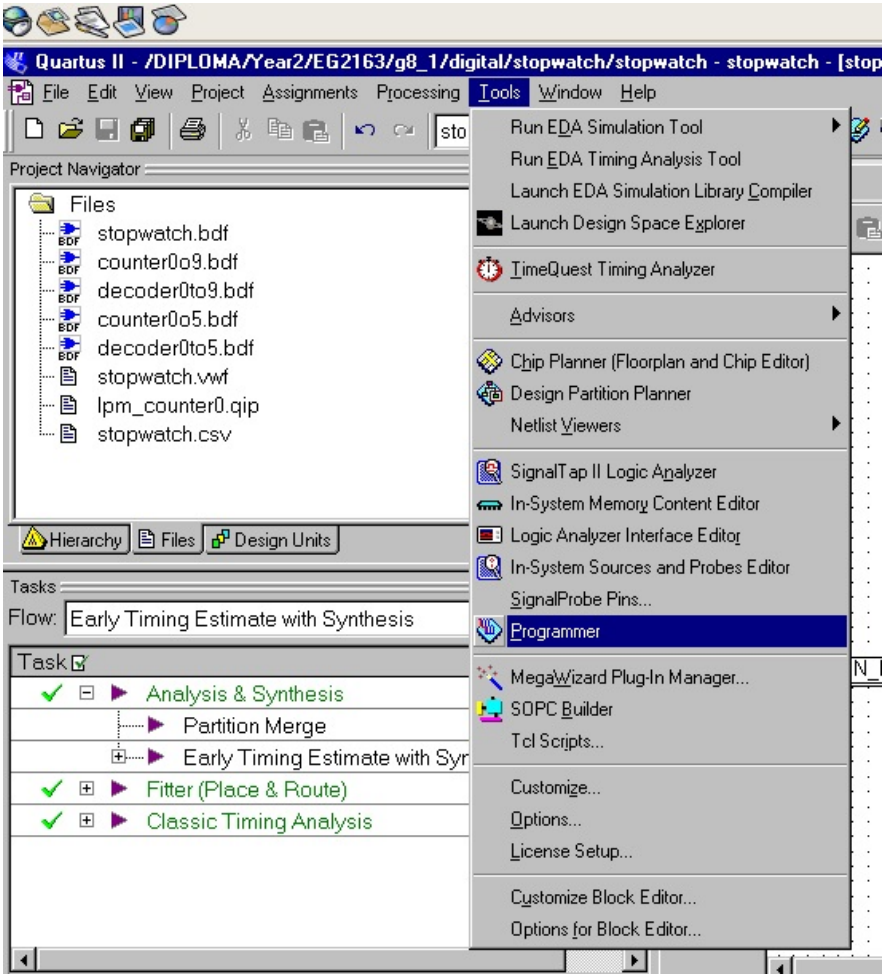


Figure 6.15 Programmer tools

It is necessary to specify the programming hardware (**USB Blaster**) and the mode (**JTAG**) that should be used. If it is not automatically detected, Click the *Hardware Setup* button and select the *USB-Blaster* in the pop-up window and select **JTAG** in the Mode box as shown in Figure 6.16 and Figure 6.17.

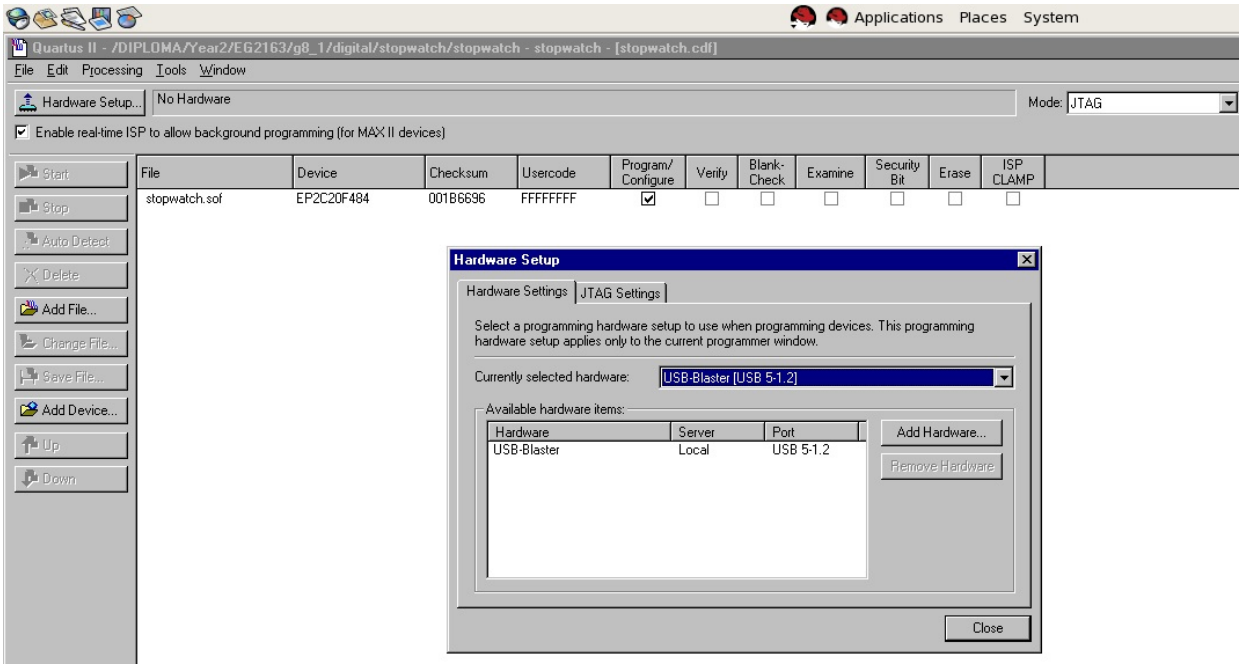


Figure 6.16 If Hardware Setup not detected automatically

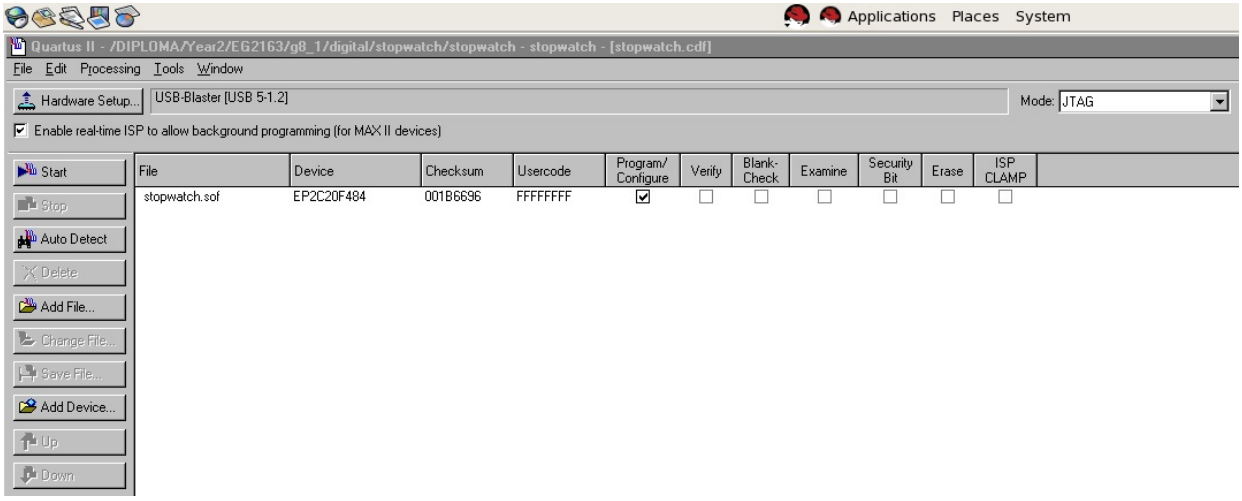


Figure 6.17 Correct Hardware Setup window

Observe that the configuration file ***stopwatch.sof*** is listed in Figure 6.17. This is a binary file produced by the Compiler's Assembler module, which contains the data needed to configure the FPGA device. The extension ***.sof*** stands for **SRAM Object File**. Note also that the device selected is **EP2C20F484C7**, which is the FPGA device used on the DE1 board. Make sure the Program/Configure check box is ticked, Click ***Start***. Having downloaded the configuration data into the FPGA device, you can now test the implemented circuit. If you need to make change/s to the design, first close the Programmer window. Then make the desired change/s, compile and reprogram the board. Repeat the process until you obtain the desired results.