Objective:

* To design a Digital Stop Watch using concepts of digital system partitioning

Digital Stop Watch - counter0to9

1. Open Digital Stop Watch Project – *stopwatch*:

To start the Quartus II software.

cd cd_digital source_.cshrc_linux quartus&

You should see a display similar to the one in Figure 3.1.



Figure 3.1 The main Quartus II display

To open the *stopwatch* project, Click *Open Existing Project* and you should see a display shown in Figure 3.2.

	Getting Started With Quartus® II Software	x
QUA	Look in: a digital	
Start D Designing w requires a pr	ab lab1 stopwatch are	
Creat (New Opt	File name:	
Open Rect stopwat lab1	Files of type: Quartus II Project File (*.qpf;*.quartus;*.qar) Cancel	
Matchst Matchst	ick ick	
Don [®] t show t	iterature Training Online Demos Support	

Figure 3.2 To open existing stopwatch folder

Double-click to open the *stopwatch* folder.

Getting Started With Quartus [®] II Software	×
Open Project Look in: stopwatch Image: Stopw	
Open Rect Stopwat Iab1 Matchstick Matchstick Matchstick	
Literature Training Online Demos Support	

Figure 3.3 To open existing *stopwatch* project

Select the *stopwatch* project file and Click *Open*.

2. Click **OK** if the below pop-up appear (ignore the pop-up). To draw the **counter0to9** circuit, Click **Files** and select to open **counter0to9.bdf** from the menu as shown in Figure 3.4.

Quartus II Can't connect to the Altera web site to check for updates - check your I	nternet connec	X tion and/or browser settings
る	watch - stop	watch - [counter0o9.bdf]
🗅 😂 🗄 🕼 🕹 🕺 🖻 💼 🗠 🗠 🔤 stopwatch	•	🕱 🖉 🧐 🔗 🗎 🗊
Project Navigator	🔡 count	er0o9.bdf
 Files stopwatch.bdf counter0o9.bdf decoder0to9.bdf counter0o5.bdf decoder0to5.bdf 		
▲ Hierarchy ■ Files ▲ Design Units Tasks ■ X Flow: Early Timing Estimate with Synthesis		
Task ☑ Time ③ □ Analysis & Synthesis □ □ Partition Merge □ ⊡ Early Timing Estimate with Synthesis □ ⊡ Fitter (Place & Route) □ ⊡ Classic Timing Analysis □		
▲ X Type Message		





Draw the *counter0to9* circuit as shown in Figure 3.5.

Figure 3.5 counter0to9 circuit

Symbols used: and2, and3, or2, or3, not, dff and vcc

Pins used: input and output

Input pin name: clk

Output pins names: q3, q2, q1 and q0

3. Create symbol for the *counter0to9* circuit. *Select File > Create/Update > Create Symbol for Current File* as shown in Figure 3.6.

6600000000000000000000000000000000000		🧠 🧠 Applications Places System
😻 Quartus II - /DIPLOMA/Year2/EG21	53/g8_1/digital/stopwatch/stopwatch - stopwatch - [c	counter0o9.bdf*]
File Edit View Project Assignments	Processing <u>I</u> ools <u>W</u> indow <u>H</u> elp	
Ctrl+N	🕨 🖙 🔀 🖉 🖓	🏽 😻 🔶 💷 🕨 🤝 🏷 🕐 🏷 🙋 🖉
Prc 😂 Open Ctrl+O	×X P source le bat	
Ctrl+F4		
New Project Wizard		🖺 🗠 🗠
📓 Open Project Ctrl+J		
Convert MAX+PLUS II Project		
Save Project		
Close Project	Ð 🗌 👘	#0
Save Ctrl+S		
Save <u>A</u> s		
Save Current Report Section As	Ę	M
File Properties		
Tas		
Fic Expert	Create Sumbol Files for Current File	
Convert Programming Files	Create AHDL Include Files for Current File	
	Create ⊻erilog Instantiation Template Files for Current File	
A Drink Drawiew	Create VHDL Component Declaration Files for Current File	
A Print ChilaP		
Contraction Contraction		No
Recent Files		
Recent Projects		A
Exit Alt+F4		
	Create/Update IPS File	
	Create Board-Level Boundary-Scan File	
	Consta Tan Lauri Danim Ele Ener Ele Danas	
X Type Message	Create Tobrevel Design File From Fin Hanver	

Click *Save* and then Click *OK*.

	Create Symbol File
	Save jn: 🔄 stopwatch 💽 🖻 蔖 📴 🥅
	ab ■ incremental_db
	File name: counter0o9 Save as type: Symbol File (*.bsf) Cancel
	Quartus II Created Block Symbol File /DIPLOMA/Year2/EG2163/g8_1/digital/stopwatch/counter0o9.bsf
•	

Figure 3.6 Create symbol for the *counter0to9* circuit

4. To place the *counter0to9* symbol onto the *stopwatch* circuit. Open the *stopwatch.dbf* from the menu shown in Figure 3.7.

8 C	é
🐇 Quartus II - /DIPLOMA/Year2/EG2163/g8_1/digital/stopwatch/stop	watch - stopwatch - [stopwatch.bdf]
Eile Edit View Project Assignments Processing Tools Window Help	
🗋 🗅 🚅 🗐 🎒 🕺 🥇 🖻 🛍 🗠 🕫 🔂 stopwatch	🔄 🔀 🖉 🤣 🛇 💷 🕨 🐯
Project Navigator	📸 stopwatch.bdf
Files stopwatch.bdf counter0o9.bdf decoder0to9.bdf counter0o5.bdf decoder0to5.bdf	
Hierarchy ☐ Files d [®] Design Units Tasks Flow: Early Timing Estimate with Synthesis ▼	
Taskg Time ③ □ Analysis & Synthesis □ Partition Merge □ Early Timing Estimate with Synthesis □ Fitter (Place & Route) □ Classic Timing Analysis	
E The Incode	

Figure 3.7 Open *stopwatch.bdf*



To insert the *counter0to9* symbol onto the *stopwatch.bdf*, Click the Symbol Tool icon D and locate the *counter0to9* symbol under *Project* as shown in Figure 3.8 and Click *OK*.

Figure 3.8 Insert counterOto9 symbol onto stopwatch circuit

Place the *counter0to9* symbol onto the *stopwatch* circuit as shown in Figure 3.9.



Figure 3.9 Inserting *counter0to9* symbol

5. Complete the circuit as shown in Figure 3.10 and Click *File > Save*.



Figure 3.10 stopwatch.bdf with counter0to9 symbol

6. Compile the circuit *Processing* > *Start Compilation* as shown in Figure 3.11 or Click the ► toolbar icon.



Figure 3.11 Compile the circuit

Make sure that there is no error as shown in Figure 3.12. Ignore warning/s.



Figure 3.12 Full Compilation was successful

7. Create a Vector Waveform File – *stopwatch.vwf* to test the *counter0to9* circuit as shown in Figure 3.13. Create twenty 50% duty clock cycles (one clock cycle 100 ns). Hence set *End* Time = 2000 ns (20 x 100 ns) and *Grid Size* = 50 ns. (Refer to Lab 1 if you have forgotten how to create Vector Waveform File).



Figure 3.13 stopwatch Vector Waveform File

8. Simulate *stopwatch – counter0to9* as shown in Figure 3.14.

Assignments > Settings – Simulation mode: Functional

ategory:	
General	Simulator Settings
Libraries	Select simulation options.
Device	
Voltage	Simulation mode: Functional
Temperature	Cinculation insult Istamustale and
Compilation Process Settings	
Early Timing Estimate	- Simulation period
- Incremental Compilation	C. Due simulation until all upster stimuli are upsed
Physical Synthesis Optimizations	
EDA Tool Settings	© End simulation at: ns ▼
- Design Entry/Synthesis	
Simulation	Gitch filtering options:
- Timing Analysis	
Formal Verification	More Settings
Physical Synthesis	
Board-Level	
Analysis & Synthesis Settings	
Verilog HUL Input	
Either Cettinge	
Timing Applusic Settings	
Assembler	
- Design Assistant	
SignalTap II Logic Analyzer	Description:
Logic Analyzer Interface	Specifies the type of simulation to perform for the current Simulation focus.
⊡- Simulator Settings	
Simulation Verification	
Simulation Output Files	
- PowerPlay Power Analyzer Settings	
SSN Analuzer	

Processing > Generate Functional Simulation Netlist

8 42				ions Places System
& Quartus II - /DIPLOMA/Year2/EG21	63/g8 1/digital/stopwatch/stopwatch - stopwa	atch - [stopwatch.vwf]		
File Edit View Project Assignments	Processing Tools Window Help			
_D ≥ E Ø 5 X h @ ×	Stop Processing Ctrl+Shift+C	🏹 🦉 🧐 🔶 👅	🕨 🦻 🍋 🏷 🕒 💺	🕘 🕸 📃 💿
Project Navigator	Start Compilation Ctrl+L	:h.bdf		Í 🕘
🗎 🗎 Files	Analyze Current File			
stopwatch.bdf	St <u>a</u> rt	ster Time Bar:	Ups	Pointer:
decoder0to9.bdf	Update Memory Initialization File		0 ps 100.0 ns 200.0 n	s 300.0 ns 400.0 ns 5
- to counter0o5.bdf	Compilation Report Ctrl+R	Name	0 ps	
decoder0to5.bdf	Start Compilation and Simulation Ctrl+Shift+K		P.	
🔄 🕒 🗈 stopwatch.vwf	Generate Functional Simulation Netlist	•0 clk		
	≿ Start Simulation Ctrl+I	o1 q3		*****
	Simulation Debug	2 q2		******************
	. 🧛 Simulation Report Ctrl+Shift+R	2 q1		*****
Hierarchy] E Files] & Design Units]	🛱 Compiler Tool	qu qu		*****
Tasks	Simulator Tool			
Flow: Early Timing Estimate with Synt	🖄 Classic Timing Analyzer Tool			
Task 🛛	🖉 PowerPlay Power Analyzer Tool			
🗸 🗉 🕨 Analysis & Synthesis	₩ SS <u>N</u> Analyzer Tool			
Partition Merge	<u></u>			
🗄 🕨 Early Timing Estima	ate with Synthesis 🛛 😽 🛃			
🖌 🗉 🕨 Fitter (Place & Route)	00:00:12			
🖌 포 🕨 Classic Timing Analysi	s 00:00:04			

Processing > Start Simulation

86000000000000000000000000000000000000		🦰 🧠 Applications Places System
😻 Quartus II - /DIPLOMA/Year2/EG21	53/g8_1/digital/stopwatch/stopwatch - stopwatch - [stopwa	tch.vwf]
Eile Edit ⊻iew Project Assignments	Processing Tools Window Help	
D 🚅 🗉 🕼 🍜 X 🖻 🛍 🖌	🔵 Stop Processing Ctrl+Shift+C 🕺 🖉 🤣	◇ 🎟 🕨 🍫 🏍 🍓 🌭 😓 🛞
Project Navigator	Start Compilation Ctrl+L th.bdf	6
🔁 Files	Analyze Current Eile	
stopwatch.bdf	Start 🕨 ster Time Bar:	0 ps Pointer:
counter0o9.bdf	Update Memory Initialization File	0 ns 100 0 ns 200 0 ns 300 0 ns 400 0 ns 5
decoder0to9.bdf	Compilation Report Ctrl+R	ame 0 po
decoder0teE.bdf	Start Compilation and Simulation Citle Shifts K	ops
B stopwatch wit	Generate Europianal Simulation Natist	
	Start Simulation City 1 03	
	Circulation Debug	
	Ch Sindation Deput	
Hierarchy 🖹 Files 🗗 Design Units		
	E Compiler Tool	
Tasks	👜 Simulator Tool	
Flow: Early Timing Estimate with Synt	😂 Classic Timing Analyzer Tool	
Task 😰	💋 PowerPlay Power Analyzer Tool	
🗸 🗉 🕨 Analysis & Synthesis	₩ SS <u>N</u> Analyzer Tool	
Partition Merge	X2 XB	
	ate with Synthesis 🛛 🖧 🗛	
✓	00:00:12	
🗸 🗉 🕨 Classic Timing Analysi	s 00:00:04	

Figure 3.14 Simulate *stopwatch* (*counter0to9*)

Expected waveform is shown in Figure 3.15.

Simu Sin	Simulation Waveforms													
Mast	er Time I	Bar:	0 ps	Pointer:	25.74	ns	Interval:		25.74 ns	Start:		End:		
R			0 ps	200.0 ns	400.0 ns	600.0 ns	1	800.0 ns	1.0 us	1.2 us	1.4 us	1.6 us	1.8 us	2.0 us
A		Name	0 ps											
₩ E	■)0	clk	F											
C)	•2×1 •2≥2	цэ q2			$\vdash \vdash \vdash$		Ħ							
<i>#</i> 4	3	q1 a0	\vdash	+	++	=		++	++++	\neq	\square $+$ $=$		$\rightarrow + +$	+
<u>*</u>		-												
80														
2↓														

Figure 3.15 stopwatch (counter0to9) waveform