

## Lab 2: Digital design (4-bit synchronous counter)

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Objective:

- \* To design a 4-bit synchronous counter
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### Digital design – 4-bit synchronous counter

#### 1. Design assignment

Design a 4-bit synchronous counter using D flip-flop base on the assignment table given below.

- (i) Draw the state diagram of the counter.
- (ii) Create the transition table for the counter.
- (iii) Use K-map to design the necessary equations.
- (iv) Create the schematic for the counter.
- (v) Simulate the functionality of the counter.

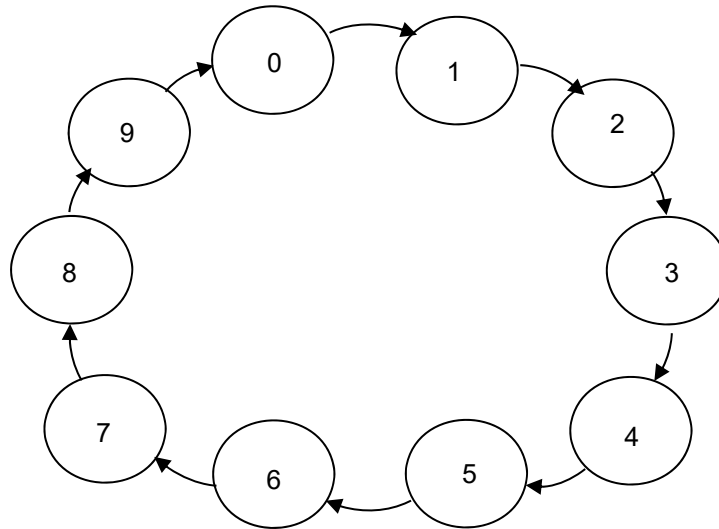
Account		Counter
gx_1	gx_13	0 – 14
gx_2	gx_14	0 – 13
gx_3	gx_15	0 – 12
gx_4	gx_16	0 – 11
gx_5	gx_17	0 – 10
gx_6	gx_18	0 – 8
gx_7	gx_19	14 – 0
gx_8	gx_20	13 – 0
gx_9	gx_21	12 – 0
gx_10	gx_22	11 – 0
gx_11	gx_23	10 – 0
gx_12	gx_24	8 – 0

Table 2.1 4-bit synchronous counter assignment table

Example: *counter0to9*

Step 1

Draw a State diagram corresponding to the counter



State diagram

Step 2

From the State diagram prepare the Transition table

Present State				Next State			
Q3	Q2	Q1	Q0	Q3*	Q2*	Q1*	Q0*
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

Transition table

Step 3

Use K-maps to determine the excitation equations (D/Q\*)

		Q1Q0			
		00	01	11	10
Q3Q2	00	0	0	0	0
	01	0	0	1	0
	11	X	X	X	X
	10	1	0	X	X

$$Q3^* = D3 = Q3.Q0B + Q2.Q1.Q0$$

		Q1Q0			
		00	01	11	10
Q3Q2	00	0	0	1	0
	01	1	1	0	1
	11	X	X	X	X
	10	0	0	X	X

$$Q2^* = D2 = Q2B.Q1.Q0 + Q2.Q1B + Q2.Q0B$$

		Q1Q0			
		00	01	11	10
Q3Q2	00	0	1	0	0
	01	0	1	0	1
	11	X	X	X	X
	10	0	0	X	X

$$Q1^* = D1 = Q3B.Q1B.Q0 + Q1.Q0B$$

		Q1Q0			
		00	01	11	10
Q3Q2	00	1	0	0	1
	01	1	0	0	1
	11	X	X	X	X
	10	1	0	X	X

$$Q0^* = D0 = Q0B$$

## Step 4

Draw the schematic

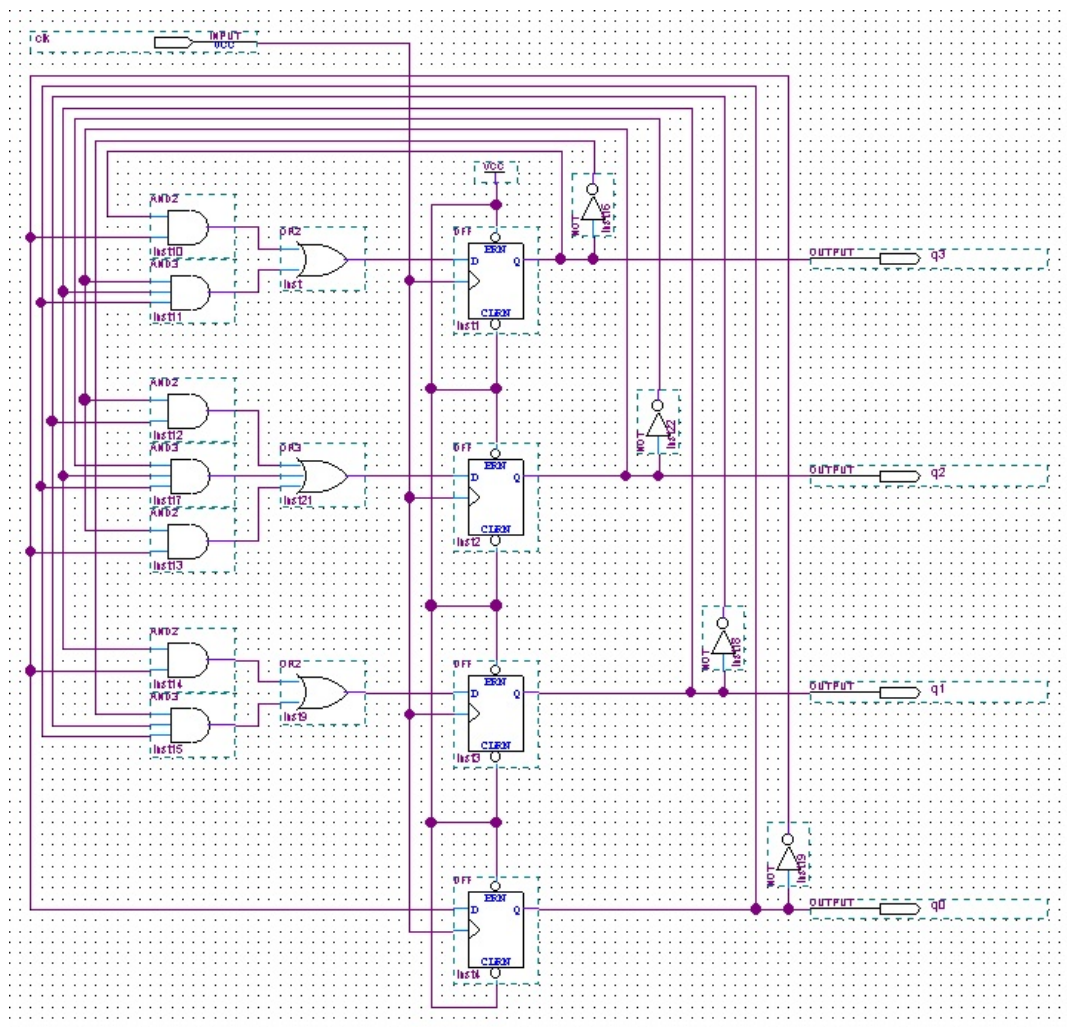


Figure 2.1 *counter0to9* circuit

## Step 5

Simulate the design

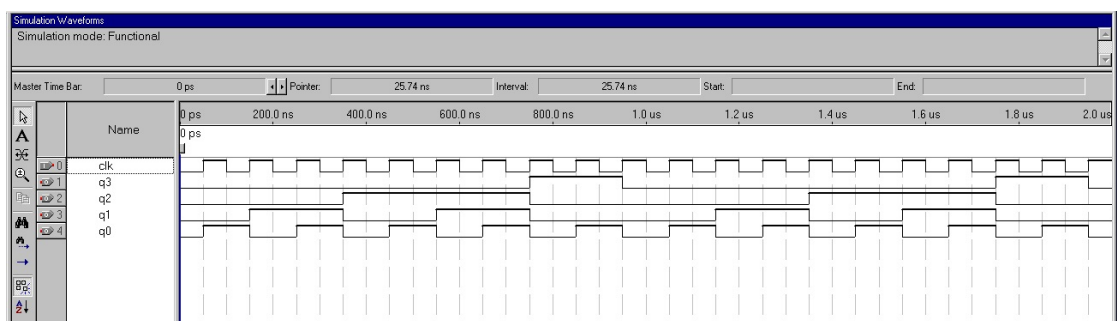


Figure 2.2 *counter0to9* waveform