Chapter 3 Digital System Design Project

This Digital System Design Project (Digital Stop Watch) is structured to focus on electronic system design and analysis through simulation and implementation adopting industry standard Electronic Design Automation methodologies. Students will apply know-how in digital design, system partitioning, design verification and implementation.

1.1 Design Project

Digital Stop Watch

Figure 3.1 Digital Stop Watch

1.2 Building Blocks of Design Project

counter0to9 (Lab 3)

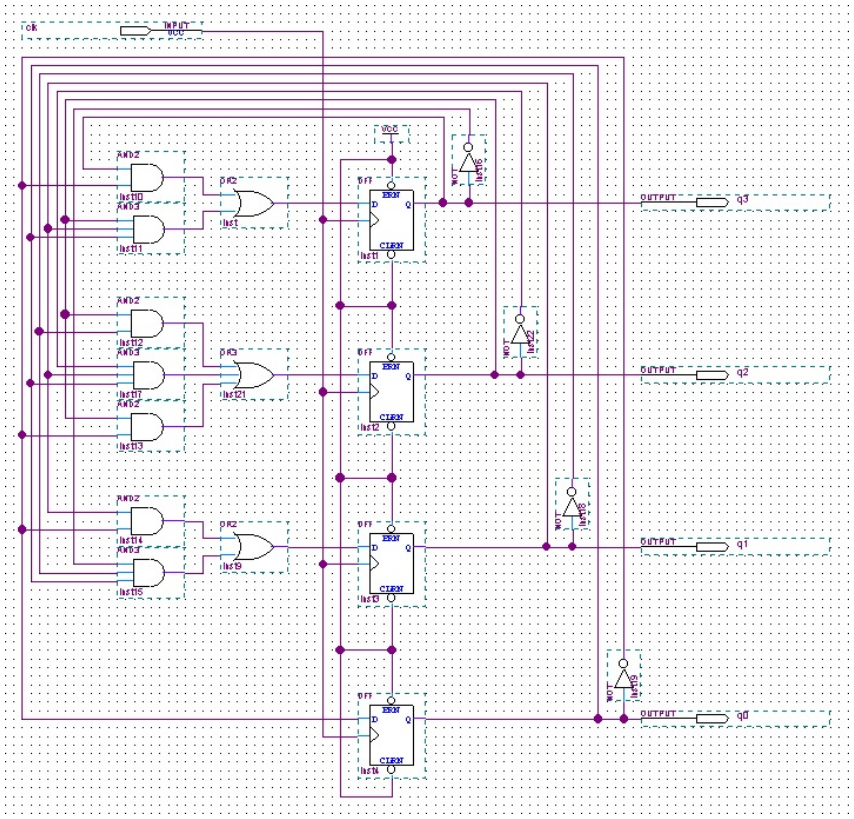

Figure 3.2 *counter0to9*

decoder0to9 (Lab 4)

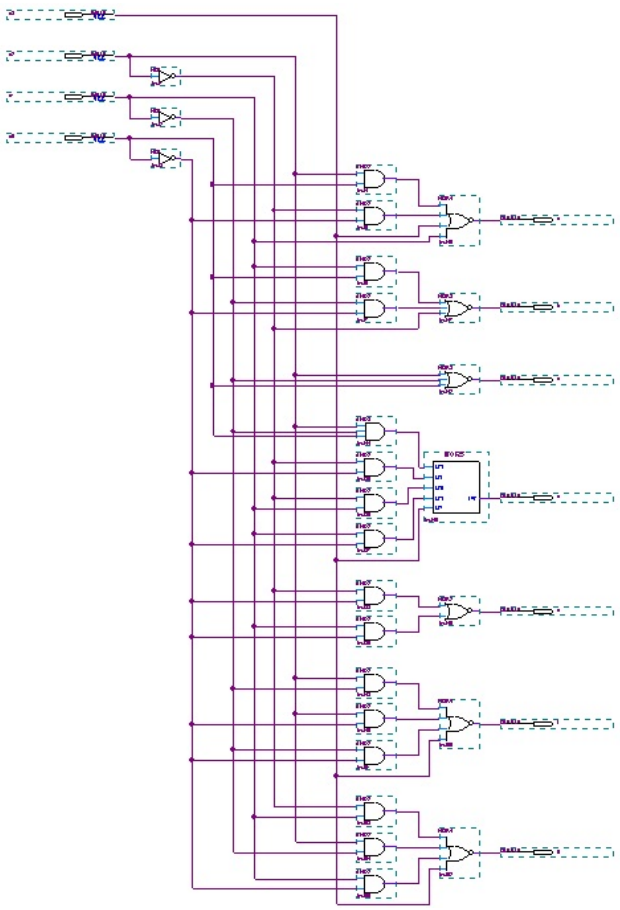

Figure 3.3 *decoder0to9*

counter0to5 & decoder0to5 (Lab 5)

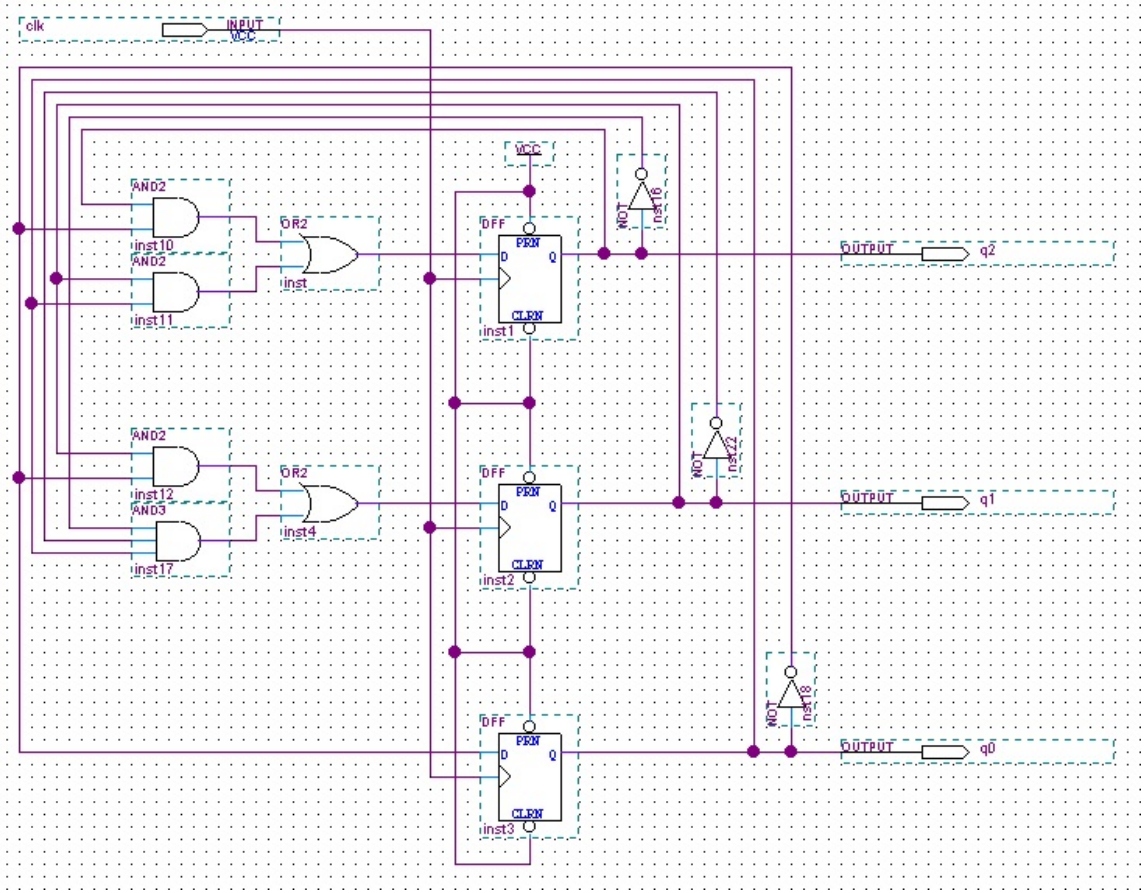

Figure 3.4 *counter0to5*

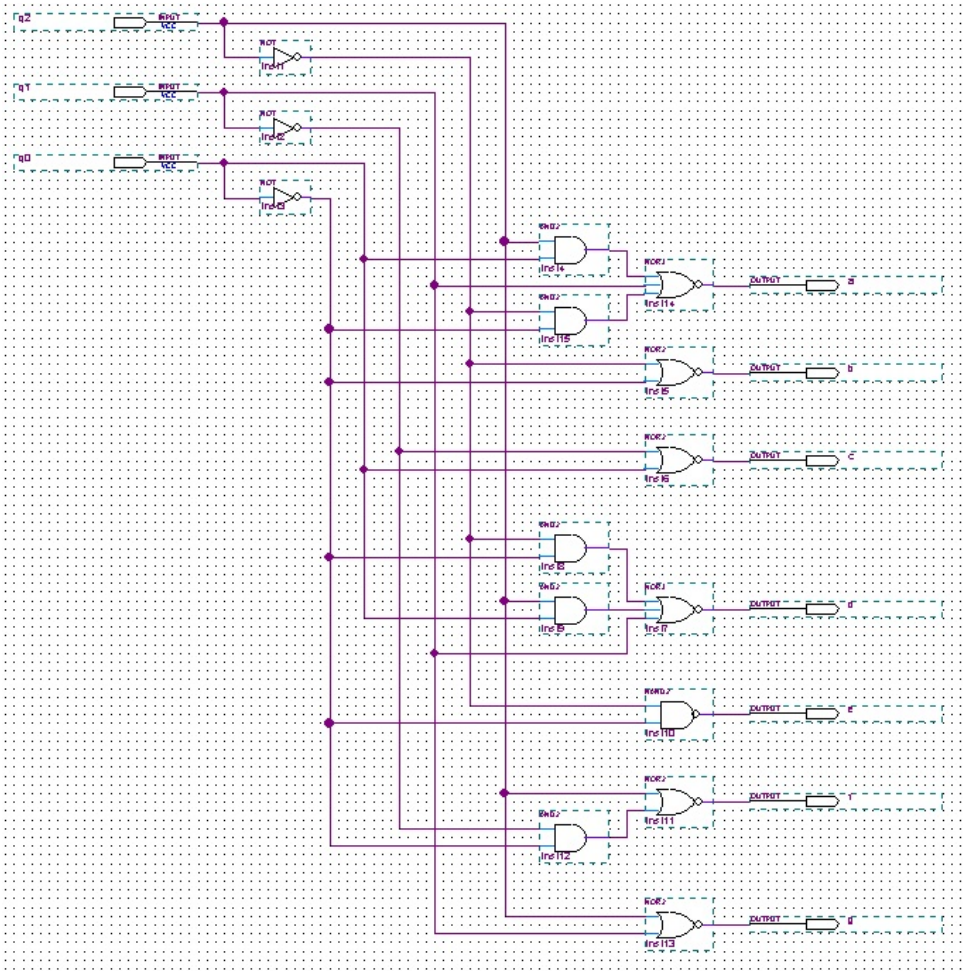

Figure 3.5 decoder0to5

counter0to59 & decoder0to59 (Lab 6)

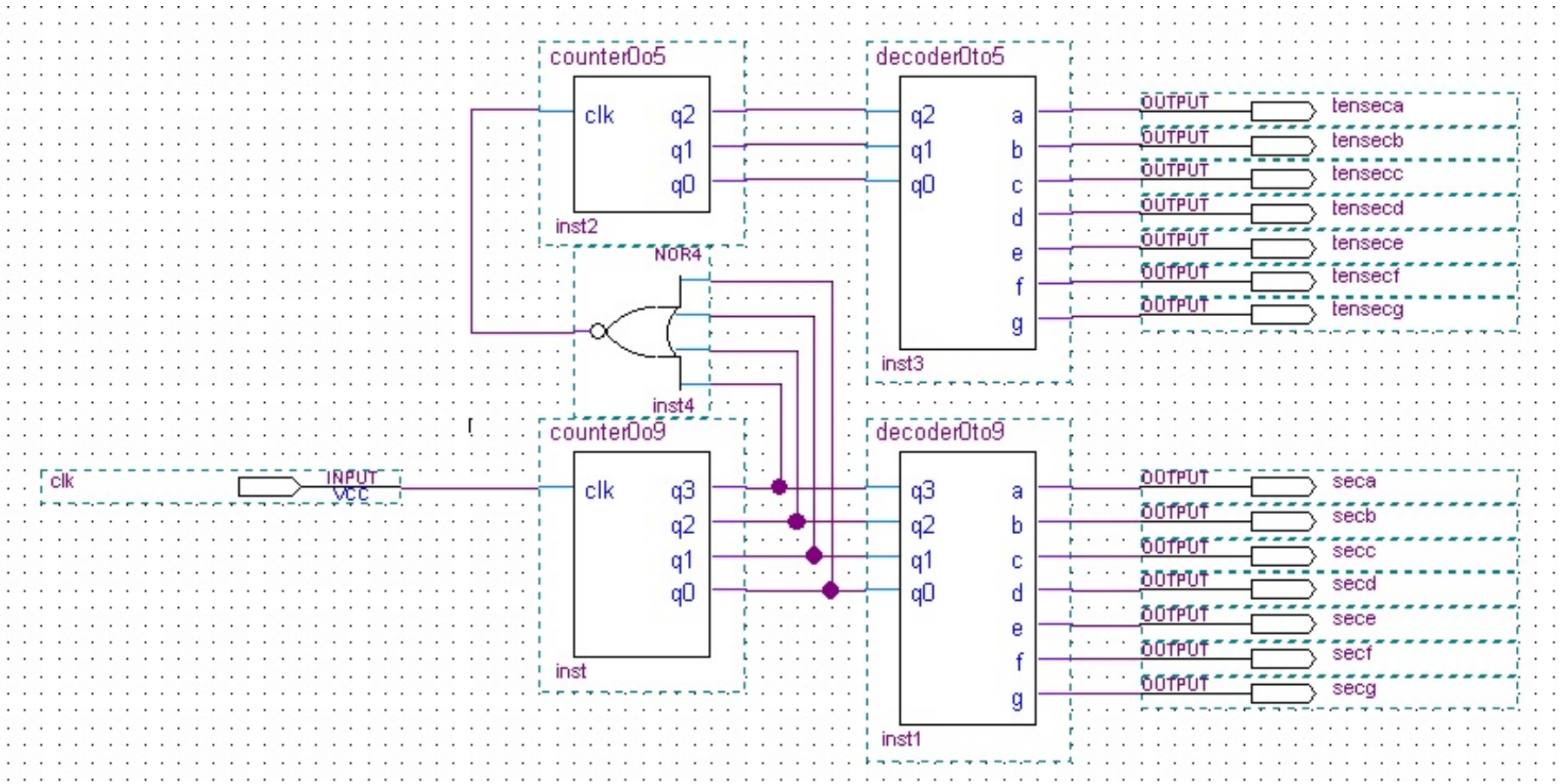

Figure 3.6 counter0to59, decoder0to59 & lpm_counter

lpm_counter Megafunction (Lab 6)

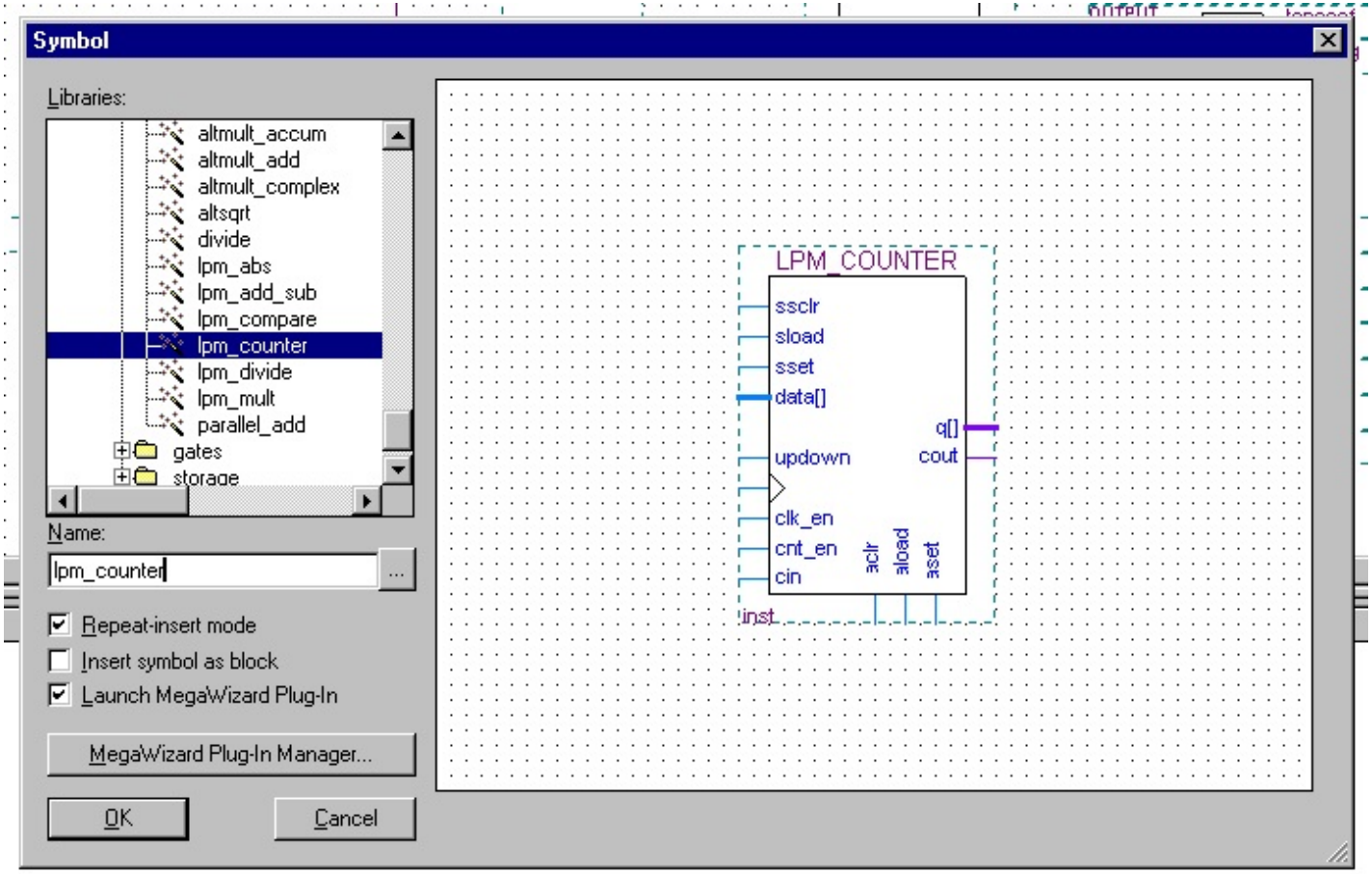

Figure 3.7 *lpm_counter*

lpm_counter is an Altera Quartus software parameterized counter megafunction. The *lpm_counter* megafunction is a full-featured binary counter with widths ranging from 1 to 256 bits that include an up, down, or up/down counter with optional synchronous or asynchronous clear, set, and load ports._The *lpm_counter* megafunction is implemented using logic elements (LEs) in the Altera FPGA devices.

stopwatch (Lab 7)

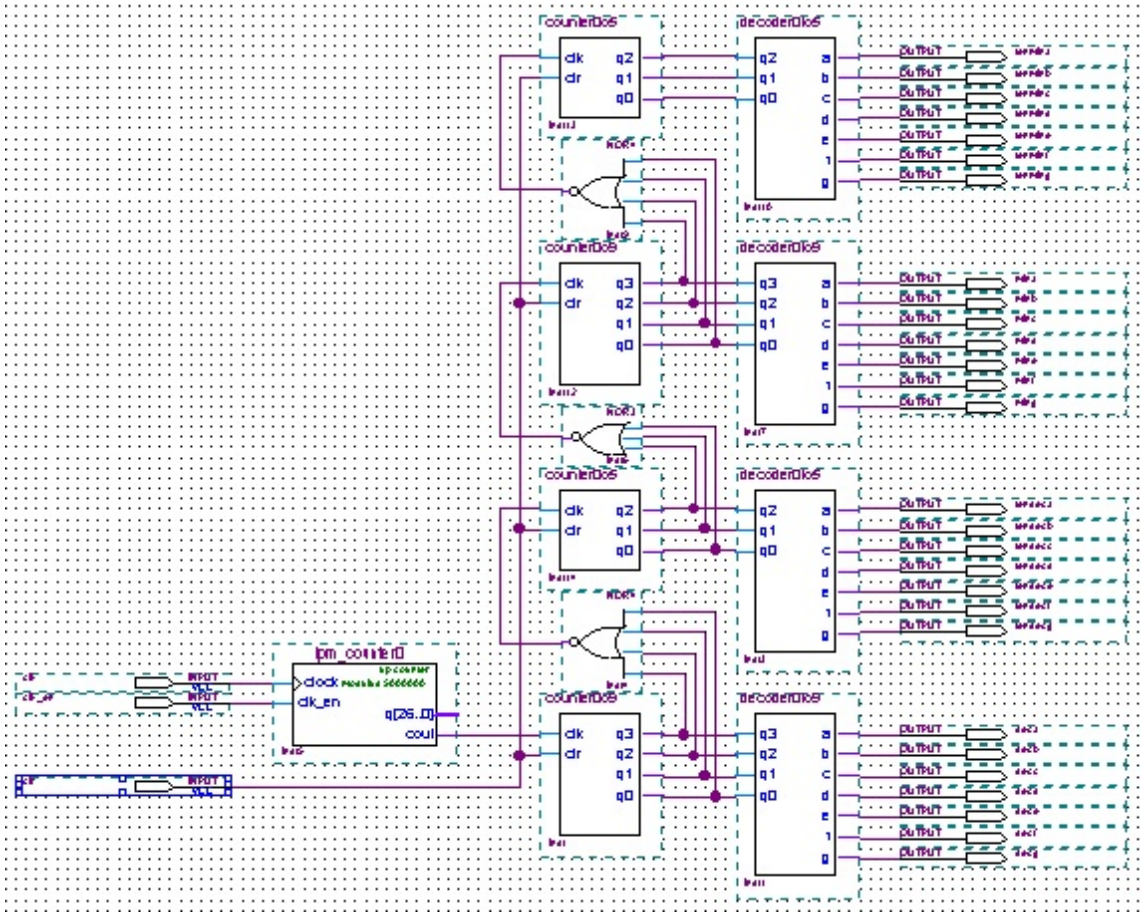

Figure 3.8 *stopwatch*