NANYANG POLYTECHNIC

2015/2016 SEMESTER 1 – SEMESTRAL EXAMINATION

Course : Diploma in Electronics, Computer and Communications Engineering

Module : EG3010 – Microelectronics

Aug/Sep 2015 Time Allowed : 2 hrs

INSTRUCTIONS TO CANDIDATES

1. This exam paper consists of **SEVEN (7)** pages including this page.

2 This examination paper contains 2 sections.

Section A: 2 Questions
Section B: 3 Questions

3. Answer ALL questions in Section A.
Answer ANY 2 questions in Section B.

4. Mask Layout Encoding Table and Stick Diagram Coding Table are provided on Page 7.

SECTION A – ANSWER ALL QUESTIONS (50 Marks)

Question 1

(a) Figure Q1 shows a METAL2 wire segment, not drawn to scale. If it has a sheet resistance of $R_s = R_{sM}\ \Omega/\square$ and a relative capacitance 0.2 $\square C_g$, compute the following:

(i) resistance of the wire, in terms of R_{sM}. (4 marks)

(ii) capacitance due to the wire, in terms of $\square C_g$. (4 marks)

(iii) time taken to travel through this segment of the wire, in terms of τ, where $\tau = R_{sn} * \square C_g$ and R_{sn} is the sheet resistance of polysilicon. (4 marks)

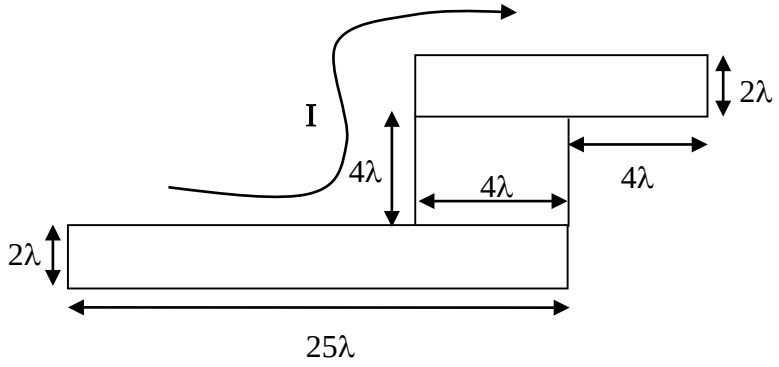


Figure Q1

(b) Justify the following design rules:

(i) 2λ poly to poly spacing. (2 marks)

(ii) 2λ overhanging of polysilicon at transistor gate. (2 marks)

(c) Latch-up is an inadvertent structure found in CMOS structure.

(i) Draw the latch-up equivalent circuit and explain what is latch-up. (5 marks)

(ii) Give two possible consequences when a latch-up occurs. (2 marks)

(iii) Suggest one method to minimize the occurrence of latch-up. (2 marks)

Question 2

For the mask layout of a CMOS circuitry shown in Figure Q2,

(a) draw its colour-coded stick diagram. (10 marks)

(b) name and explain the diffusion type used to form Part (I). State the purpose of Part (I) in a CMOS layout. (3 marks)

(c) what does the demarcation line in the stick diagram represent? (2 marks)

(d) why is diffusion not used for cross-well interconnections? (3 marks)

(e) draw its transistor level schematic and state the boolean equation for **Z**. (7 marks)

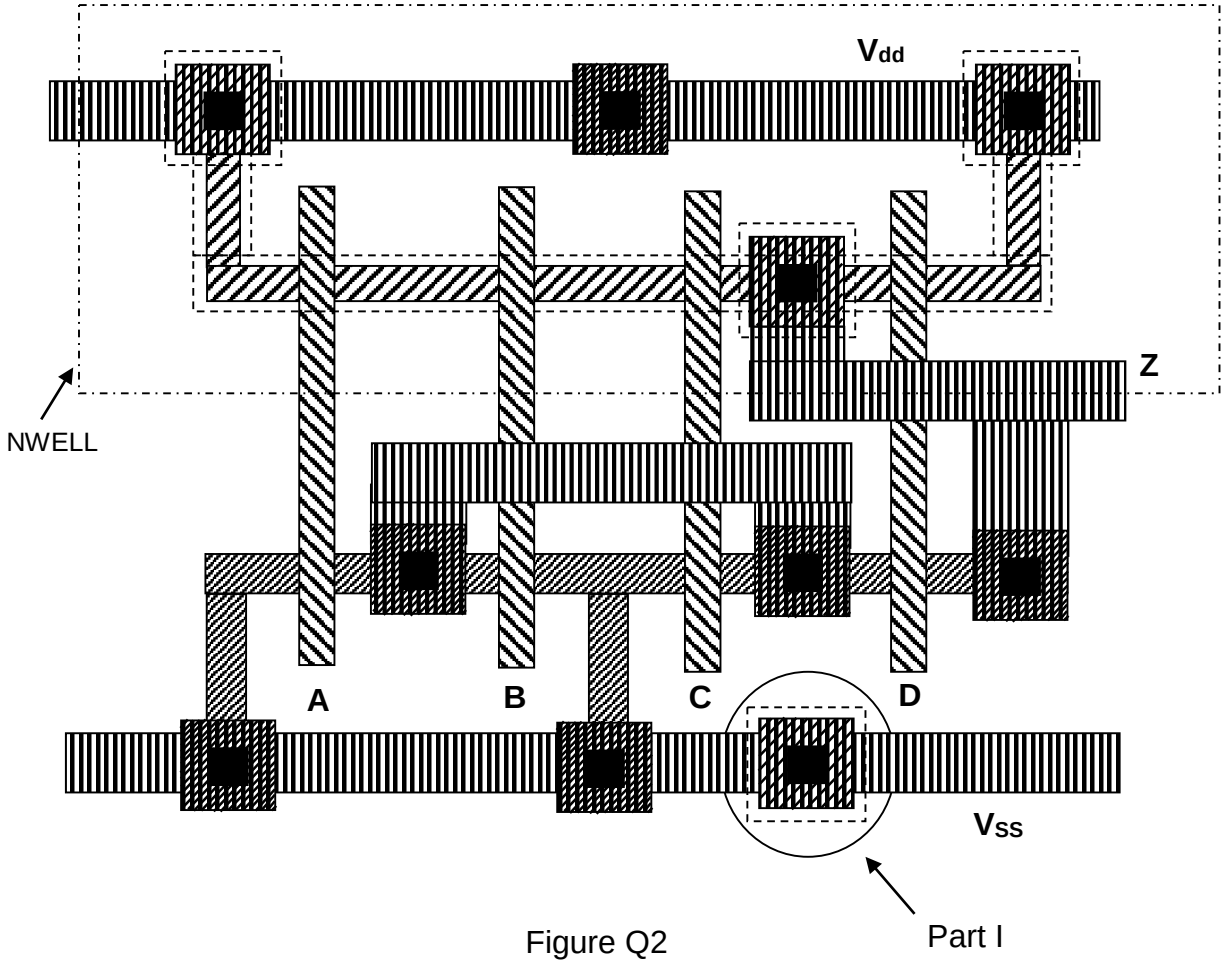


Figure Q2

END OF SECTION A

SECTION B – ANSWER ANY 2 QUESTIONS (50 Marks)

Question 3

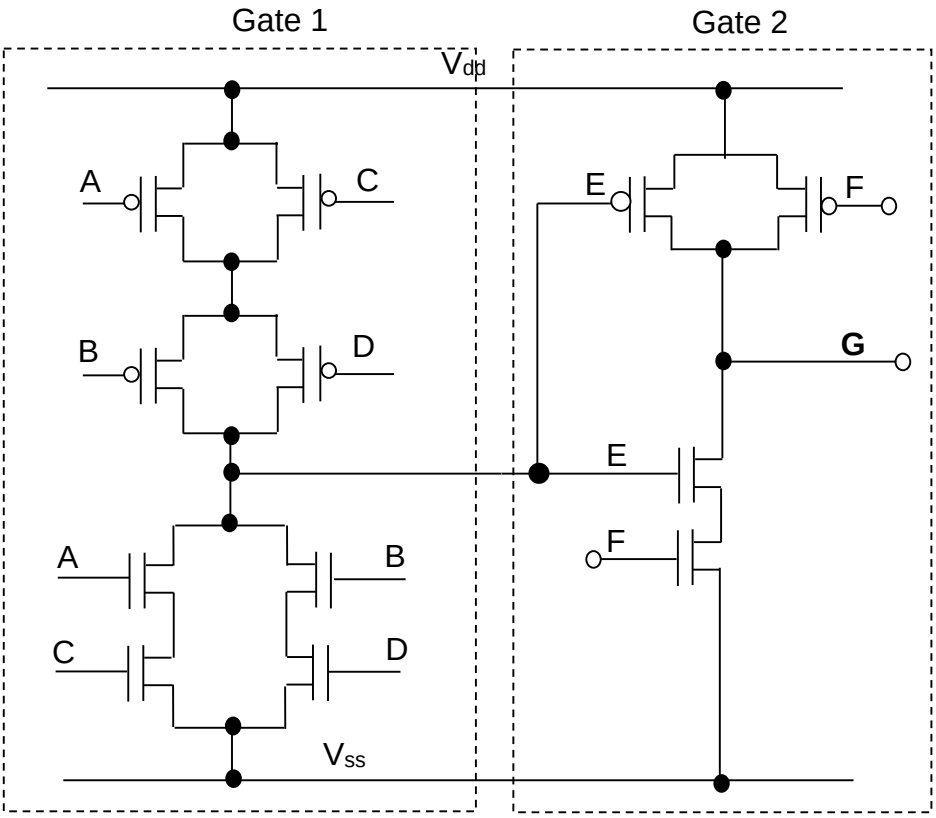


Figure Q3

(a) For the CMOS complex gate shown in Figure Q3, state the boolean equation at point ***G***. (5 marks)

(b) Using the transistor sizes given in Table Q3, calculate the delay time from **D** to **G** for A = B = F = 1, C = D = 0 for a load of $3\square C_g$.
Give the answer in terms of τ where $\tau = R_{sn} \bullet \square C_g$ and $R_{sp} \approx 2.5\ R_{sn}$.

(12 marks)

Gate	Transistor	Length (L)	Width (W)
Gate1	PMOS	2λ	16λ
	NMOS	2λ	2λ
Gate 2	PMOS	2λ	8λ
	NMOS	2λ	4λ

Table Q3

(c) CMOS devices are known to be ratioless device, yet ratio is applied to the sizing of the various transistors as shown in Table Q3.

(i) Explain the purposes of having different sized PMOS and NMOS as shown. (2 marks)

(ii) Using relevant equations, explain how the size affects the path capacitance? (2 marks)

(iii) State 2 trade-offs when using larger transistors compared to smaller ones. (4 marks)

Question 4

(a) Explain briefly the Write and Read operation of the 3-T DRAM cell shown in Figure Q4. (7 marks)

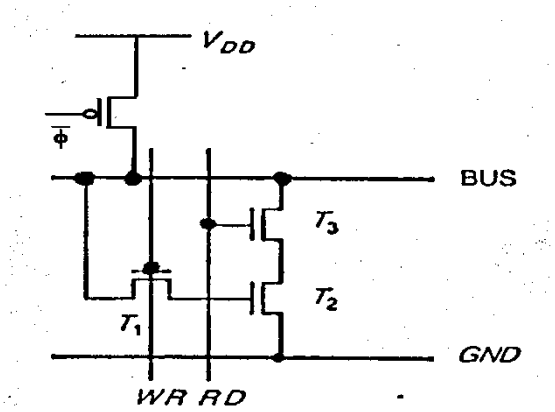


Figure Q4

(b) Explain briefly the need for sense amplifier in a RAM array. (3 marks)

(c) List three key differences between Static and Dynamic RAM. (6 marks)

(d) Explain briefly the propose of the following in integrated circuit (IC) design:

(i) Test benches (2 marks)

(ii) Functional simulation (2 marks)

(iii) Logic synthesis (2 marks)

(iv) Design Rule Checker (3 marks)

Question 5

(a) Name 3 semi-custom design techniques. Give one advantage and one disadvantage for each of the techniques named. (9 marks)

(b) For the Verilog codes given in Figure Q5:

(i) draw the block diagram and label the input and output pins. (4 marks)

(ii) is **Rst** a synchronous or asynchronous signal? Explain the purpose of this signal. (4 marks)

(iii) explain the functionality of the codes. (4 marks)

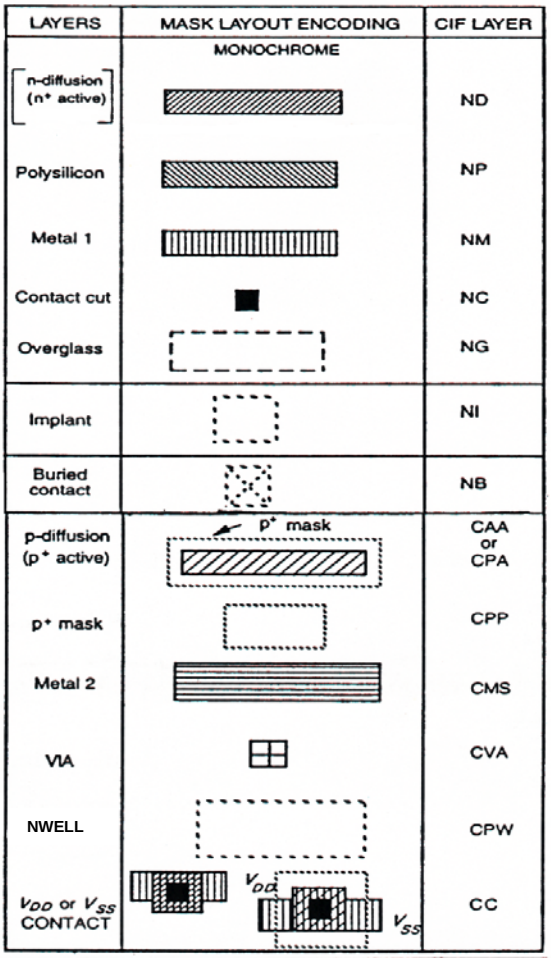
```
module Exam (Rst, Data, Clock, Q);
input Rst, Data, Clock;
output reg [3:0] Q;

always @(posedge Clock)
        if (Rst) Q <= 0;
else
begin
        Q[0] <= Q[1];
        Q[1] <= Q[2];
        Q[2] <= Q[3];
        Q[3] <= Data;
end
endmodule
```

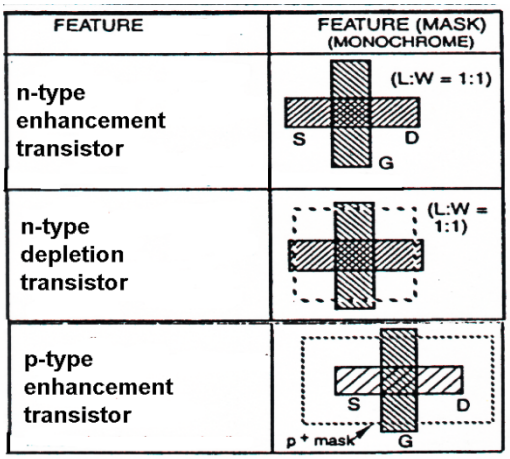
Figure Q5

(c) Two common approaches for digit circuit design are schematic capture and HDL approach. Name one advantage and one disadvantage for each of the approach. (4 marks)

END OF SECTION B

Mask Layout Encoding Table





Stick Diagram Encoding Table

Layer	Colour	Stick Encoding
n-diffusion	Yellow outline, Brown within	
p-diffusion	Dark Brown outline, Brown within	
Polysilicon	Green	
Metal 1	Blue	
Metal 2	Red	
Implant	Yellow dotted line	
Contact - Connect Poly to Metal 1 - Connect Diffusion to Metal 1	Black Solid circle	
Via - Connect 2 metals	Black	
*N-well / P-well boundary	Brown dotted line	
*Well tie / Substrate tie	Black Cross	V_{dd} / V_{ss}

* only applicable to CMOS process

END OF PAPER