NANYANG POLYTECHNIC

2014/2015 SEMESTER 2 – SEMESTRAL EXAMINATION

Course : Diploma in Electronics, Computer and Communications Engineering

Module : EG3010 – Microelectronics

Feb/Mar 2015 Time Allowed : 2 hrs

INSTRUCTIONS TO CANDIDATES

1. This exam paper consists of **EIGHT (8)** pages including this page.

2 This examination paper contains 2 sections.

Section A: 2 Questions
Section B: 3 Questions

3. Answer ALL questions in Section A.
Answer ANY 2 questions in Section B.

4. Mask Layout Encoding Table and Stick Diagram Coding Table are provided on Page 8.

SECTION A – ANSWER ALL QUESTIONS (50 Marks)

Question 1

(a) Explain briefly the need for the following CAD tools used in integrated circuit design.
(i) Design Rule Checker (3 marks)
(ii) Layout vs Schematic Checker (3 marks)

(b) For the CMOS layout shown in Figure Q1,
(i) draw the corresponding colour-coded stick diagram. (7 marks)
(ii) draw the corresponding transistor level schematic and state the output equation at **X** of the circuit. (9 marks)

(c) Briefly explain why diffusion is not allowed to cross the substrate-well boundary. (3 marks)

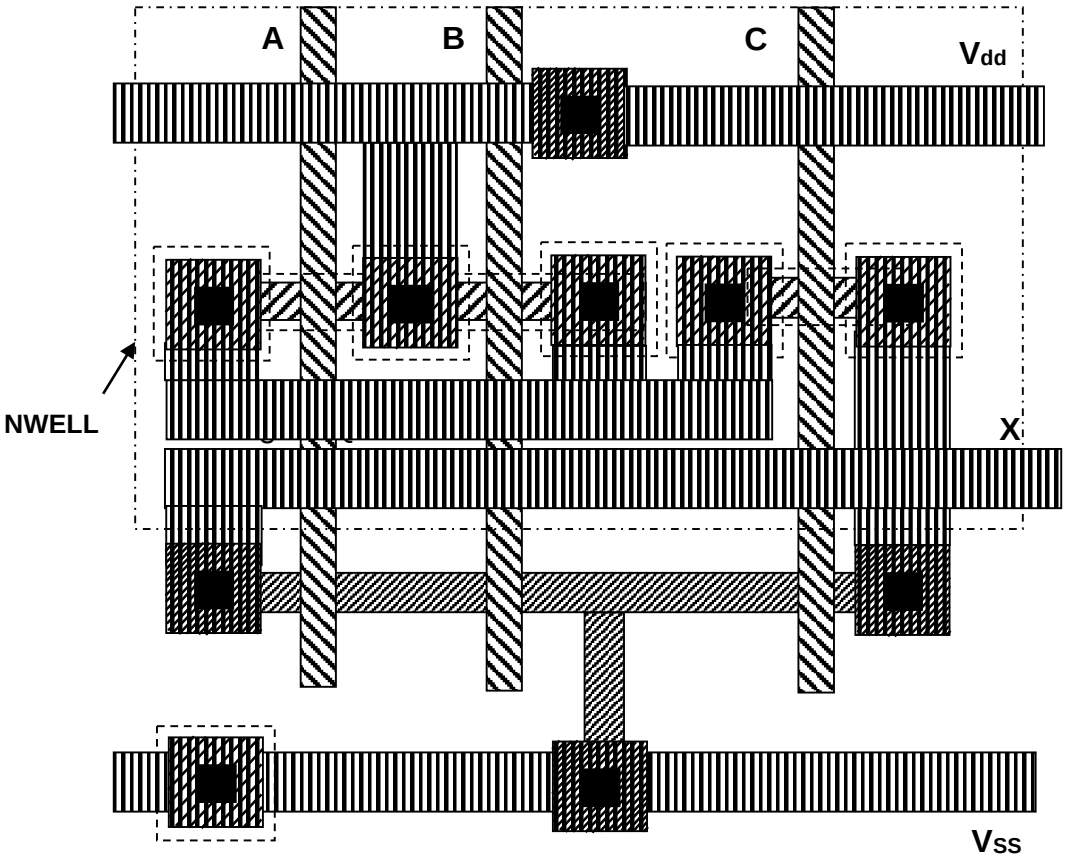


Figure Q1

Question 2

(a) Draw the layout of an NMOS transistor of Width = 4λ and Length = 2λ. Indicate the width and length accordingly. (4 marks)

(b) Explain how channel length and width of a transistor affects its resistance. Substantiate your answer with relevant equation. (3 marks)

(c) Name any two of the basic MOS layers and briefly state their characteristics. (4 marks)

(d) Sketch and label carefully the cross-sectional structure of a CMOS inverter using Nwell process. (6 marks)

(e) Latch-up is an inadvertent structure found in CMOS structure.
(i) Draw the latch-up equivalent circuit and explain what is latch-up. (4 marks)
(ii) Give two possible consequences when a latch-up occurs. (2 marks)
(iii) Suggest one method to minimize the occurrence of latch-up. (2 marks)

END OF SECTION A

SECTION B – ANSWER ANY 2 QUESTIONS (50 Marks)

Question 3

(a) For the combinational circuit shown in Figure Q3,

(i) write the Boolean equation for output, **F**. (2 marks)

(ii) draw the transistor level implementation using CMOS **standard gate** concept. (6 marks)

(iii) draw the transistor level implementation using CMOS **static complex gate** concept. (8 marks)

Assume negated signals are readily available.

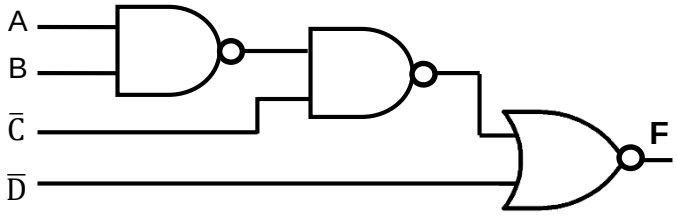


Figure Q3

(b) For a 2-input NAND gate driving a load of 1C_g:

(i) determine its tpHL (4 marks)

(ii) determine its best case tpLH (5 marks)

Assume all transistors used are minimum-sized transistors and $R_{sp} \approx 2.5\ R_{sn}$. Give the answer in term of $\tau = R_{sn} \bullet C_g$.

Question 4

(a) Figure Q4 shows a polysilicon wire segment, not drawn to scale. If it has a sheet resistance of $R_s = R_{spoly}\ \Omega/\square$ and a relative capacitance of polysilicon-to-substrate of 1.0 $\square C_g$, compute the following:-

(i) resistance of the polysilicon wire, in terms of R_{spoly}. (4 marks)

(ii) capacitance of the polysilicon to substrate, in terms of $\square C_g$. (4 marks)

(ii) time taken to travel this segment of the wire as indicated by the arrow, in terms of τ, where $\tau = R_{sn} * \square C_g$. (4 marks)

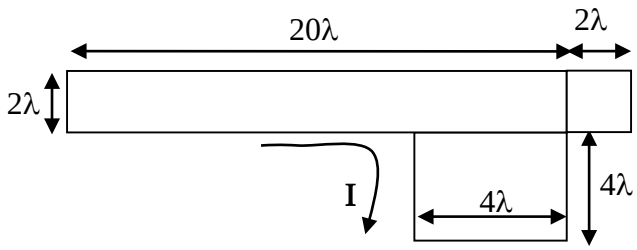


Figure Q4

(b) Explain, with the aid of diagrams, the operation of a NMOS pass transistor when:

(i) transferring logic High. (5 marks)

(ii) transferring logic Low. (5 marks)

(c) Name and draw the MOS switch that will pass both logic ‘1’ and ‘0’ without degradation. (3 marks)

Question 5

(a) Figure Q5a shows a 6-transistor SRAM. Using the diagram provided,

(i) explain its read and write operation. (6 marks)

(ii) explain the need for the sense amplifier circuit. (3 marks)

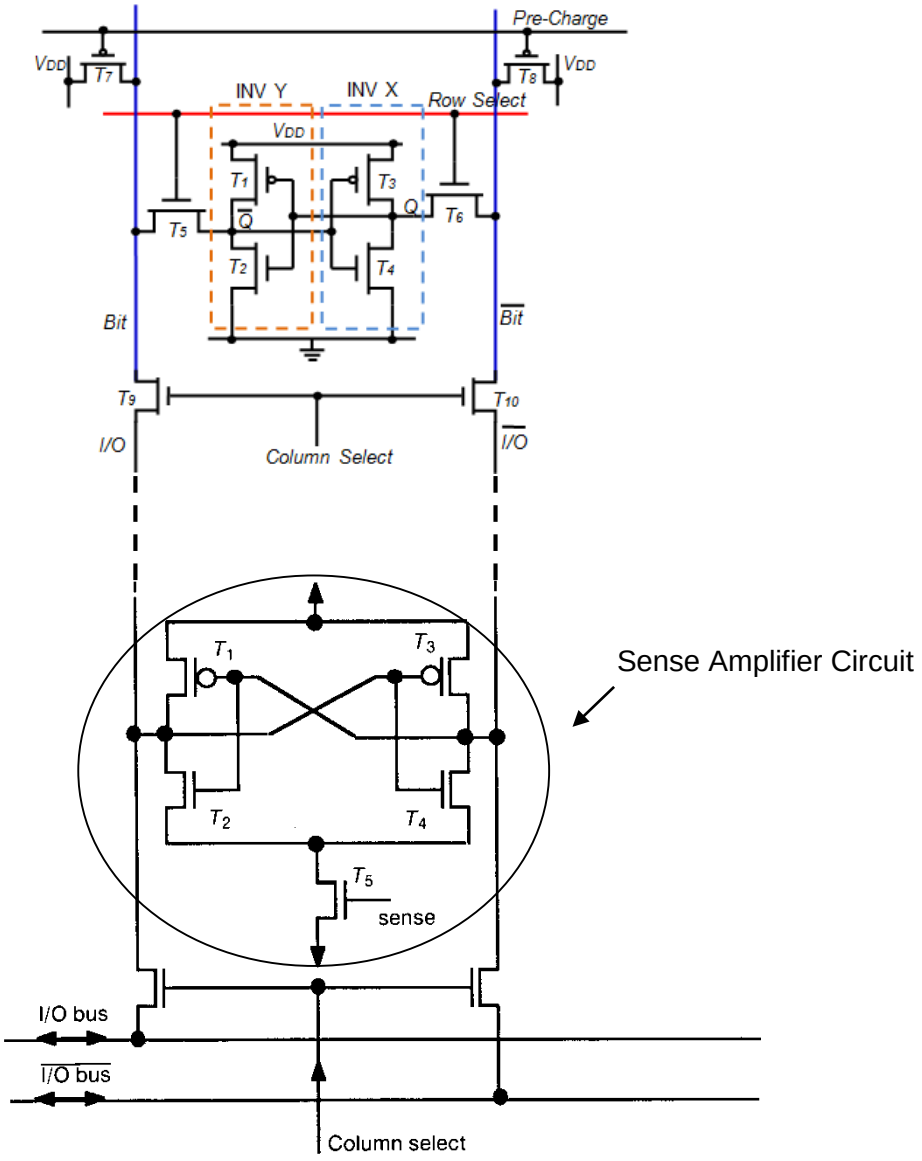


Figure Q5a

(b) List three key differences between Static and Dynamic RAM. (6 marks)

(c) For the Verilog codes given in Figure Q5b,

(i) draw the block diagram and label the input and output pins. (4 marks)

(ii) Is **clr** a synchronous or asynchronous signal? Explain . (2 marks)

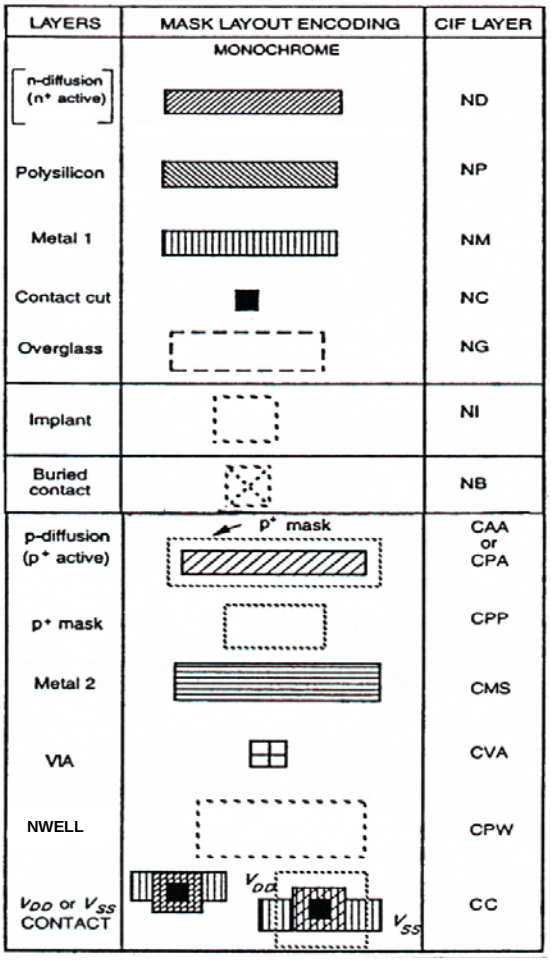
(iii) explain the functionality of the codes. (4 marks)

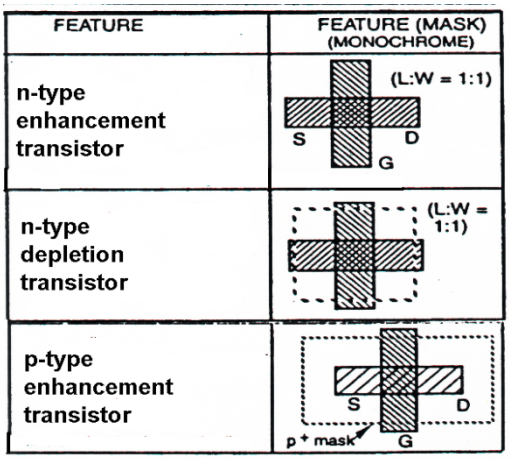
```
module Exam (clk, clear, up_down, q);
input clk, clr, up_down;
output [3:0] q;
reg [3:0] tmp;

assign q = tmp;

always @(posedge clk)
begin
  if (clr)
      tmp <= 4'b0000;
  else if (up_down)
      tmp <= tmp + 1'b1;
  else
      tmp <= tmp - 1'b1;
end
endmodule
```

Figure Q5b

END OF SECTION B

Mask Layout Encoding Table





Stick Diagram Encoding Table

Layer	Colour	Stick Encoding
n-diffusion	Yellow outline, Brown within	
p-diffusion	Dark Brown outline, Brown within	
Polysilicon	Green	
Metal 1	Blue	
Metal 2	Red	
Implant	Yellow dotted line	
Contact - Connect Poly to Metal 1 - Connect Diffusion to Metal 1	Black Solid circle	
Via - Connect 2 metals	Black	
*N-well / P-well boundary	Brown dotted line	
*Well tie / Substrate tie	Black Cross	V_{dd} / V_{ss}

* only applicable to CMOS process

END OF PAPER