NANYANG POLYTECHNIC

2014/2015 SEMESTER 1 – SEMESTRAL EXAMINATION

Course : Diploma in Electronics, Computer and Communications Engineering

Module : EG3010 – Microelectronics

Aug/Sep 2014 Time Allowed : 2 hrs

INSTRUCTIONS TO CANDIDATES

1. This exam paper consists of **SEVEN (7)** pages including this page.

2 This examination paper contains 2 sections.

Section A: 2 Questions
Section B: 3 Questions

3. Answer ALL questions in Section A.
Answer ANY 2 questions in Section B.

4. Mask Layout Encoding Table and Stick Diagram Coding Table are provided on Page 7.

SECTION A – ANSWER ALL QUESTIONS (50 Marks)

Question 1

(a) Figure Q1 shows a polysilicon wire segment, not drawn to scale. If it has a sheet resistance of $R_s = R_{sM}\ \Omega/\square$ and a relative capacitance 0.3 $\square C_g$, compute the following:

(i) resistance of the wire, in terms of R_{sM}. (4 marks)

(ii) capacitance due to the wire, in terms of $\square C_g$. (4 marks)

(iii) time taken to travel through this segment of the wire, in terms of τ, where $\tau = R_{sn} * \square C_g$. (4 marks)

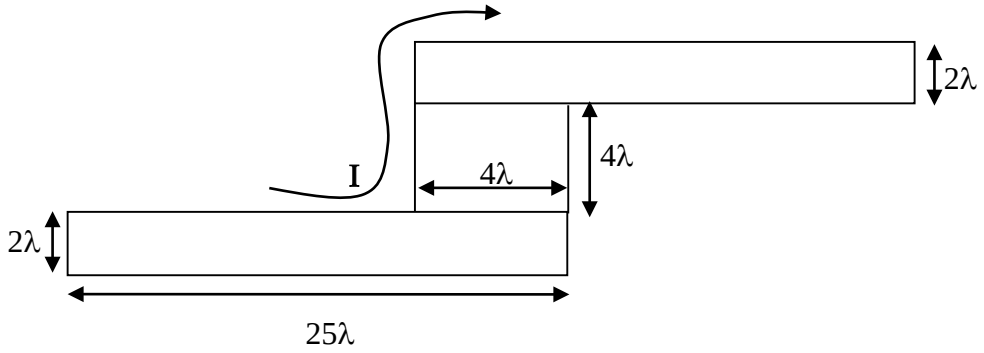


Figure Q1

(b) Justify the following design rules:

(i) 2λ poly to poly spacing. (2 marks)

(ii) 2λ overhanging of polysilicon at transistor gate. (2 marks)

(c) Latch-up is an inadvertent structure found in CMOS structure.

(i) Draw the latch-up equivalent circuit and explain what is latch-up. (5 marks)

(ii) Give two possible consequences when a latch-up occurs. (2 marks)

(iii) Suggest one method to minimize the occurrence of latch-up. (2 marks)

Question 2

For the CMOS layout shown in Figure Q2,

(a) draw the corresponding colour-coded stick diagram. (10 marks)

(b) draw the corresponding transistor level schematic and state the output equation at **Z** of the circuit. (10 marks)

(c) briefly explain why diffusion is not allowed to cross the substrate-well boundary. (3 marks)

(d) name the diffusion used to form the well-tie and substrate-tie. (2 marks)

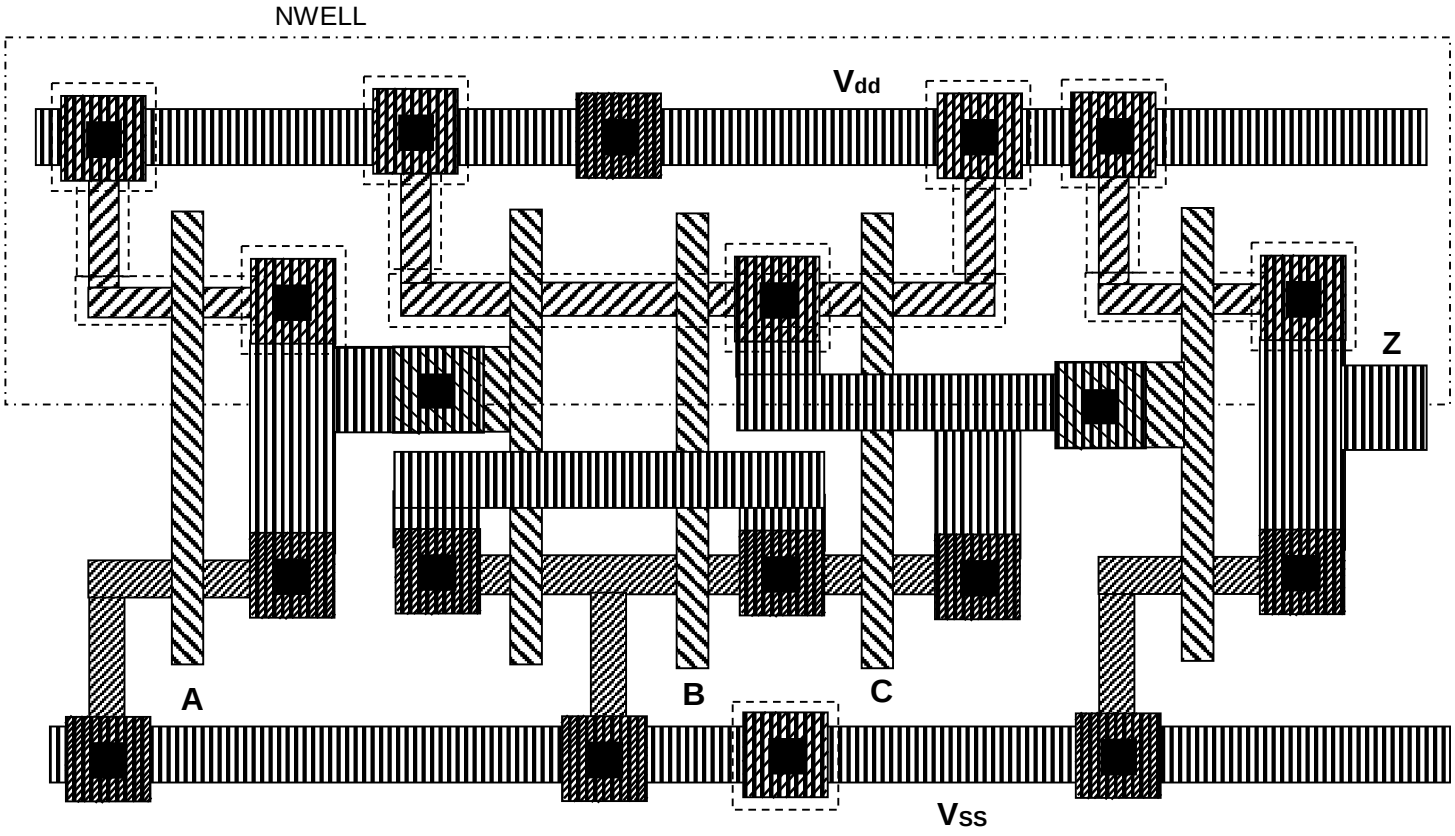


Figure Q2

END OF SECTION A

SECTION B – ANSWER ANY 2 QUESTIONS (50 Marks)

Question 3

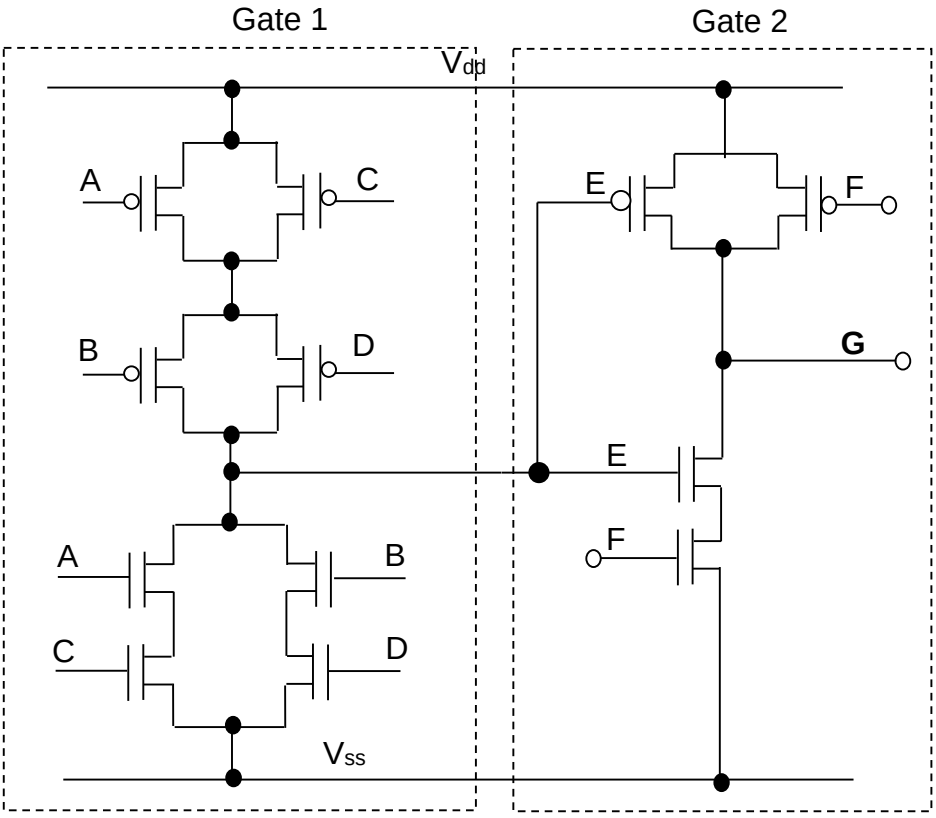


Figure Q3

(a) For the CMOS complex gate shown in Figure Q3, state the boolean equation at point ***G***. (5 marks)

(b) Using the transistor sizes given in Table Q3, calculate the delay time from **D** to **G** for A = B = F = 1, C = D = 0 for a load of $3 \square C_g$.
Give the answer in terms of τ where $\tau = R_{sn} \bullet \square C_g$ and $R_{sp} \approx 2.5\ R_{sn}$. (12 marks)

Gate	Transistor	Length (L)	Width (W)
Gate1	PMOS	2λ	16λ
	NMOS	2λ	2λ
Gate 2	PMOS	2λ	8λ
	NMOS	2λ	4λ

Table Q3

(c) CMOS devices are known to be ratioless device, yet ratio is applied to the sizing of the various transistors as shown in Table Q3.

(i) Explain the purposes of having different sized PMOS and NMOS as shown. (2 marks)

(ii) Using relevant equations, explain how the size affects the path capacitance? (2 marks)

(iii) State 2 trade-offs when using larger transistors compared to smaller ones. (4 marks)

Question 4

(a) For each of the extrinsic semiconductors (n-type and p-type) :

(i) name 2 suitable dopants (4 marks)

(ii) state the majority carriers found in the semiconductor. (2 marks)

(b) Draw the layout of an NMOS transistor of Length = 2λ and width = 4λ. Indicate the length and width accordingly. (4 marks)

(c) Explain how channel length and width of a transistor affects its resistance. Substantiate your answer with relevant equation. (3 marks)

(d) Explain why dynamic MOS circuits operate faster than static MOS circuits. (4 marks)

(e) Figure Q4 shows an n-channel P-E logic. Explain its operation in terms of:

(i) Precharge Phase (4 marks)

(ii) Evaluation Phase (4 marks)

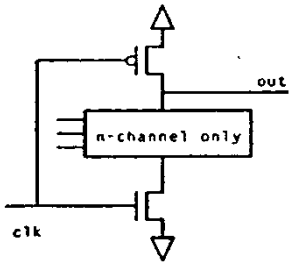


Figure Q4

Question 5

(a) IC design flow can be divided into 2 major phases namely frontend and backend.

(i) Name 2 languages commonly used in the frontend for digital circuit design. (2 marks)

(ii) Name 4 key processes in the backend phase. (4 marks)

(b) Explain briefly the purpose of the following in IC design:

(i) Test benches (2 marks)

(ii) Functional simulation (2 marks)

(iii) Logic synthesis (2 marks)

(c) For the codes given in Figure Q5,

(i) draw the block diagram and label the input and output pins. (4 marks)

(ii) explain the functionality of the codes. (6 marks)

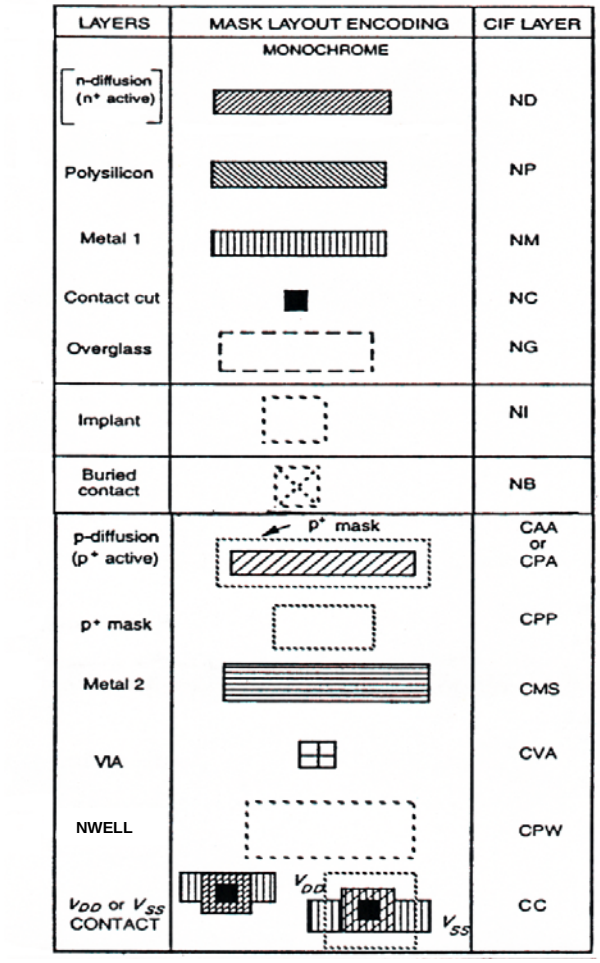
(iii) the module represents a combinational or sequential circuit? Justify your answer. (3 marks)

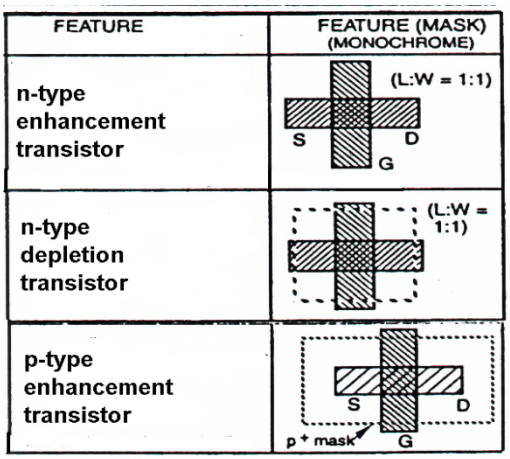
```
module exam ( clk, clear, load, data, up_down, oData );

input clk, clear, load, up_down;
input [7:0] data;
output  [7:0] oData;
reg     [7:0] cnt;
assign oData = cnt;

always @ (posedge clk)
begin
    if (!clear)
        cnt = 8'h00;
    else if (load)
        cnt = data;
    else if (up_down)
        cnt = cnt + 1;
    else
        cnt = cnt - 1;
end

endmodule
```

Figure Q5

END OF SECTION B

Mask Layout Encoding Table





Stick Diagram Encoding Table

Layer	Colour	Stick Encoding
n-diffusion	Yellow outline, Brown within	
p-diffusion	Dark Brown outline, Brown within	
Polysilicon	Green	
Metal 1	Blue	
Metal 2	Red	
Implant	Yellow dotted line	
Contact - Connect Poly to Metal 1 - Connect Diffusion to Metal 1	Black Solid circle	
Via - Connect 2 metals	Black	
*N-well / P-well boundary	Brown dotted line	
*Well tie / Substrate tie	Black Cross	V_{dd} / V_{ss}

* only applicable to CMOS process

END OF PAPER