CHAPTER 5

DIGITAL IC SUBSYSTEMS DESIGN

5.1 VLSI DESIGN AND CONSIDERATIONS

When designing large complex systems, a logical and systematic approach is essential; otherwise, the whole system may become obsolete even before it is off the drawing block. A common approach is the top-down design approach. With this approach, a complex system is partitioned into various subsystems based on functionality and modularity.   Each module is further subdivided into smaller modules until the complexities of the sub-modules are at a comprehensible level of details. Subsequently, high degree of regularity within the sub-modules/subsystems are either identified or created before the actual design is embarked on.

Logical connections and number of interconnections between the various subsystems are also important considerations during the design phase.   Power routing, data bus routing and control signal routing are important routes that need careful planning.

Testing requirements are also major considerations right at the start of the design process. Additional circuitries to test the functionality of the various blocks within the IC are designed during the design phase. The testing circuitry may take up as much as 30% of the total chip area.

5.1.1 System Partitioning

Figure 5-1 shows the system partitioning of a 4-bit Arithmetic Logic Unit (ALU), which generally performs operations such as arithmetic, logic and shifting operations as well as provide temporary storage for the operands.   It can be divided into 3 subsystems as shown.

The register array acts as a temporary storage for the operands. It stores data coming from the I/O port as well as the output of the adder. The adder unit performs arithmetic and logic operations on the data from the register array.   The shifter shifts the output of adder, if necessary, before sending it to the register array or communicate it to other subsystems through the I/O port. Control over the functions to be performed is effected by the control signals as indicated.
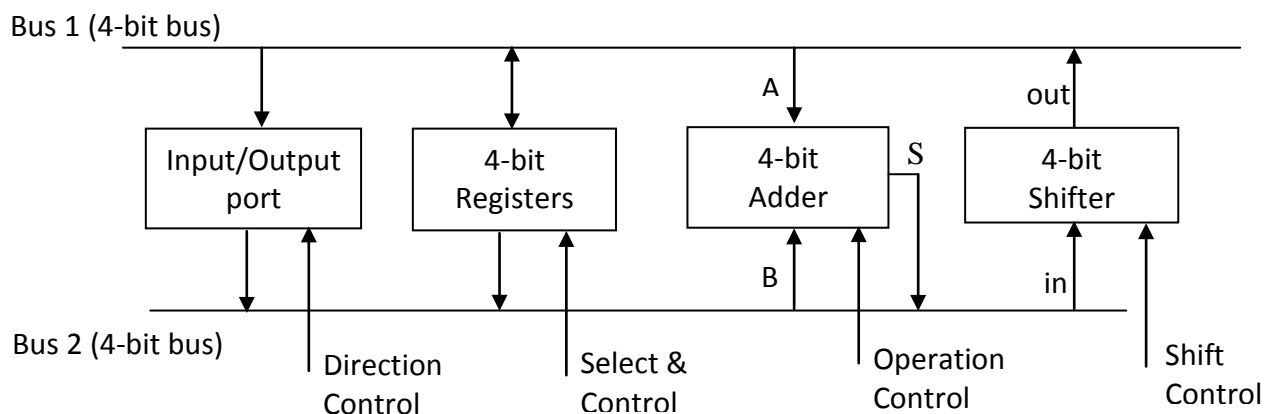
Bus 1 (4-bit bus)

Input/Output port	4-bit Registers	4-bit Adder	4-bit Shifter

Bus 2 (4-bit bus)

Direction Control   Select & Control   Operation Control   Shift Control

Figure 5-1   Basic Two Bus Architecture of 4-bit ALU

5.2   DESIGN OF AN ADDER

5.2.1 Requirements For an n-bit Adder

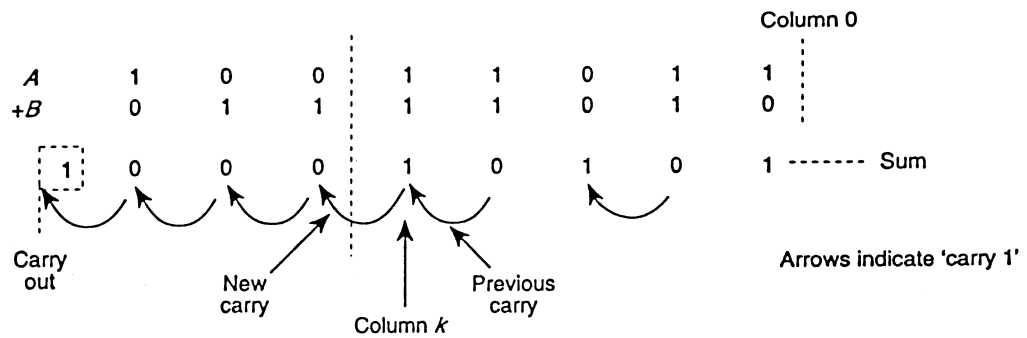Consider the addition of two binary numbers A + B as follows:

Figure 5-2   Addition of Two Binary Numbers

From the above, it is shown that for any addition of a "1" to column K, this bit actually act as a third input to the adder hence a truth table with three inputs A_k, B_k, C_{k-1} and two outputs S_k and C_k is required as shown in Table 5-3.

Inputs			Outputs	
A_k	B_k	C_{k-1}	S_k (Sum)	C_k (Carry)
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Table 5-3   Truth Table of a 1-bit Full Adder

Using SOP,

$$\text{Sum, } S_k = \overline{A}_k B_k \overline{C}_{k-1} + A_k \overline{B}_k \overline{C}_{k-1} + \overline{A}_k \overline{B}_k C_{k-1} + A_k B_k C_{k-1}$$

$$S_k = \overline{C}_{k-1}(\overline{A}_k B_k + A_k \overline{B}_k) + C_{k-1}(\overline{A}_k \overline{B}_k + A_k B_k)$$

Let $\quad H_k = (\overline{A}_k B_k + A_k \overline{B}_k)$

Thus $\quad S_k = H_k \overline{C}_{k-1} + \overline{H}_k C_{k-1} = H_k \oplus C_{k-1}$

Similarly, using SOP, $\quad C_k = A_k B_k + H_k C_{k-1}$

Based on the above equations, the followings are derived for implementation into stick diagrams.

If $A_k = B_k$ then $H_k = 0$ thus $S_k = C_{k-1}$ and
$$C_k = A_k = B_k$$

else, $\quad H_k = 1$ and $S_k = \overline{C}_{k-1}$ and
$$C_k = C_{k-1}$$

Figure 5-4 shows the block diagram of a 1-bit adder with its input and output pins/interconnections and their access direction. The access direction is of great importance as it dictates how subsequent adder bits can be cascaded. Figure 5-5 shows the stick diagram connections for C_k and S_k based on the Boolean equations derived previously.
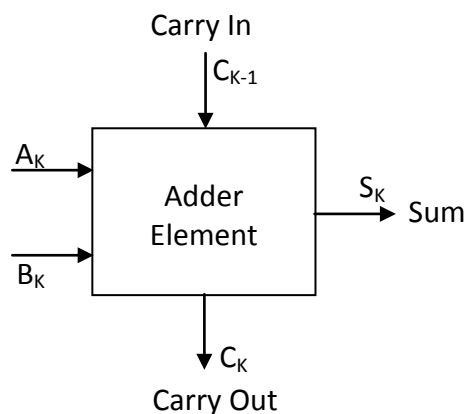

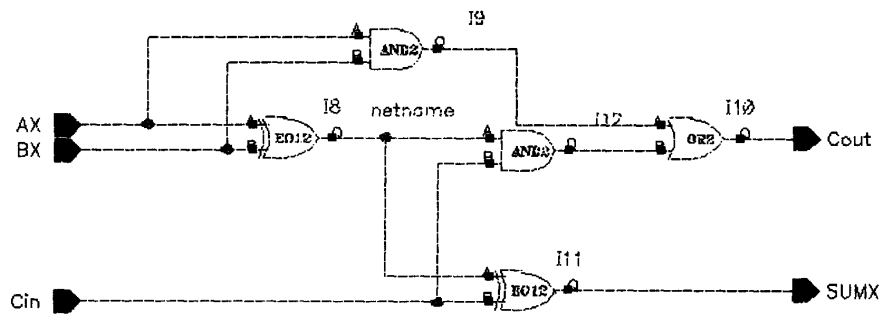Figure 5-4 Block Diagram of 1-bit Full Adder with Access Pins defined

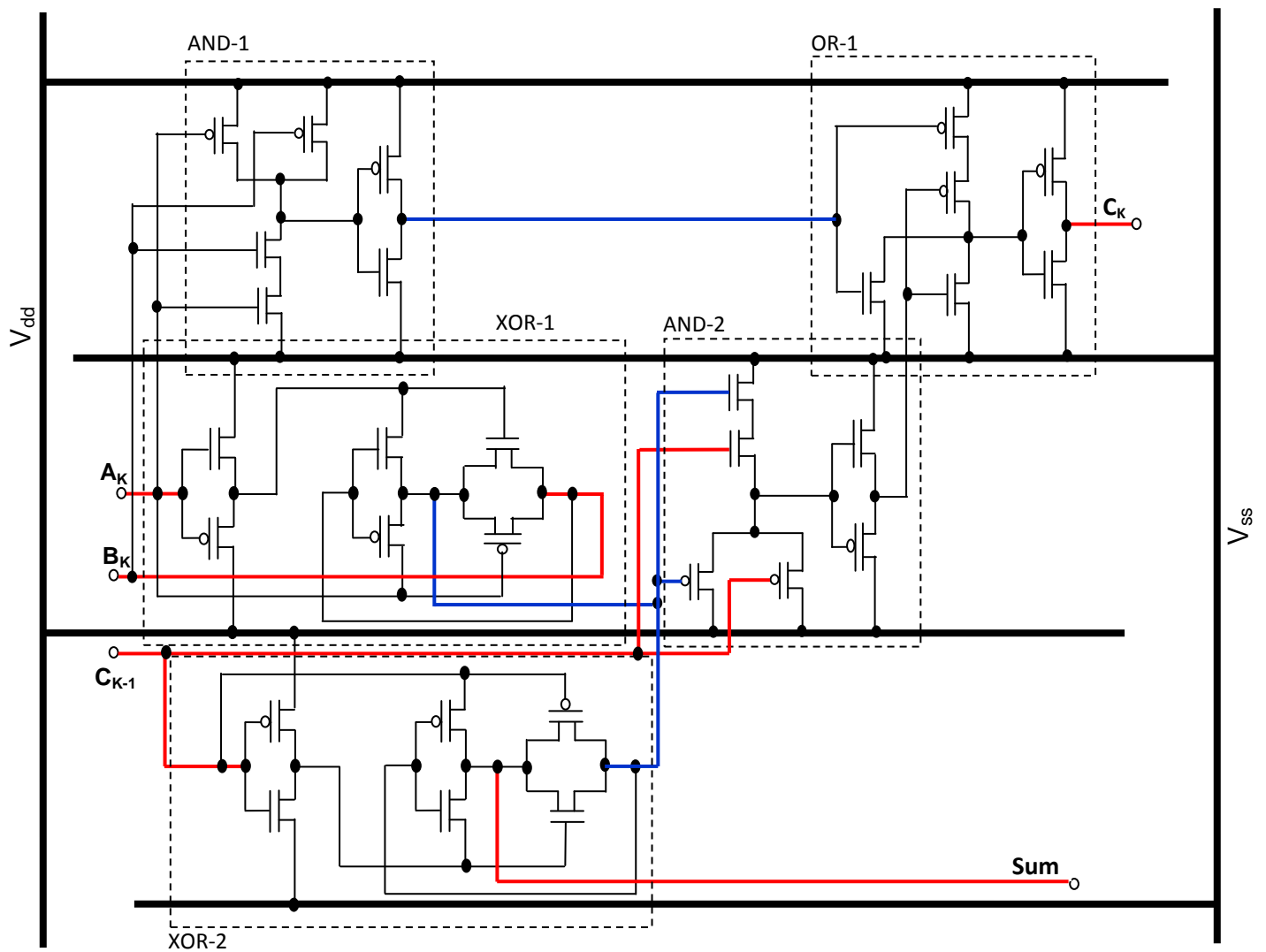Figure 5-5 Gate-Level schematic of 1-bit Full Adder

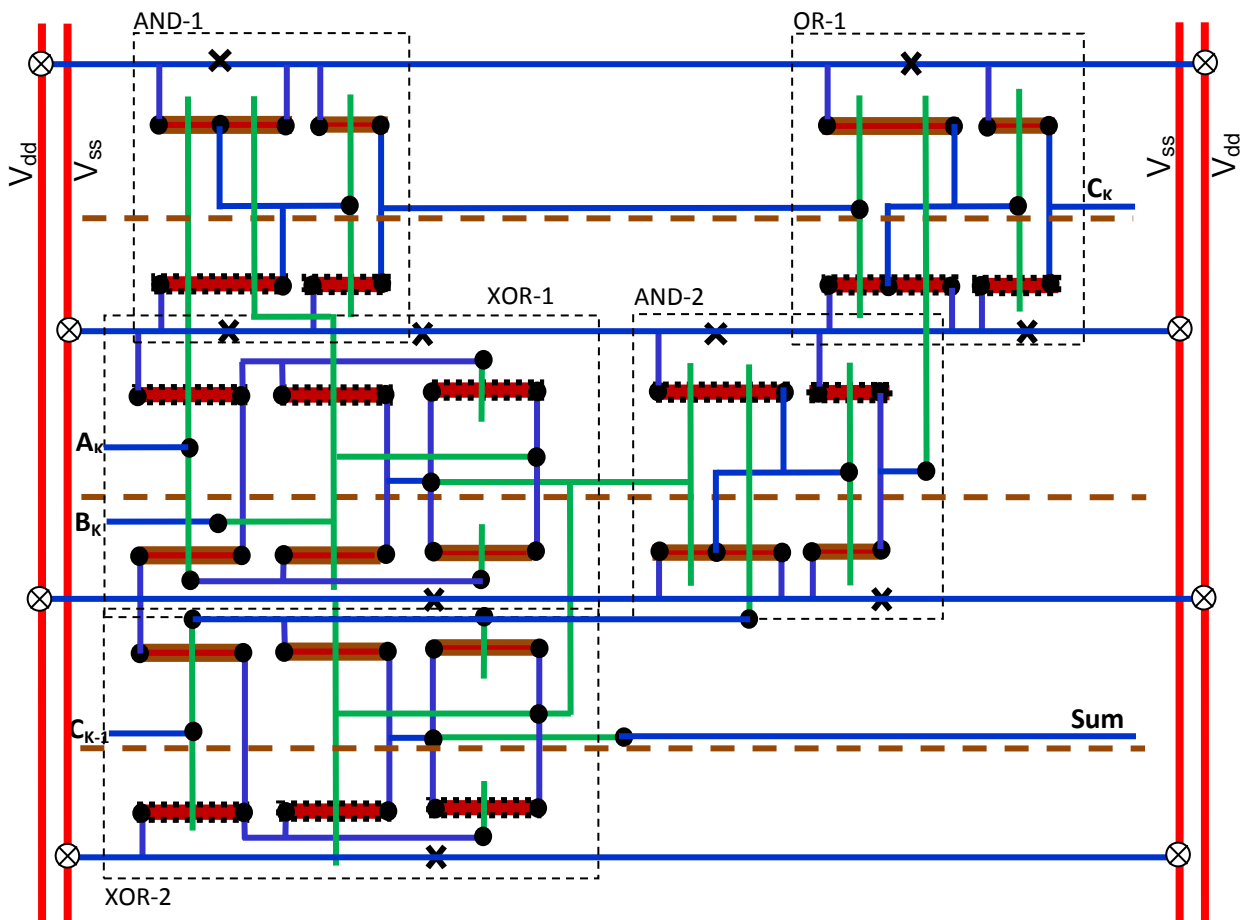Figure 5-6 Transistor-Level schematic of 1-bit Full Adder

Figure 5-7   Stick Diagram of Single bit Adder using CMOS technology

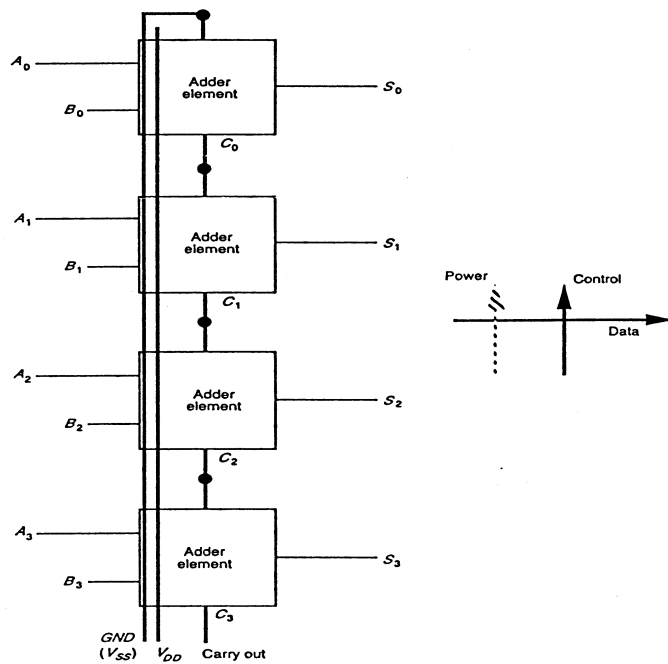A 4-bit adder is then formed by cascading four added elements as indicated in Figure 5-8.

Figure 5-8   4-bit Adder Block Layout Structure

5.3 DESIGN OF A SHIFTER

A shifter performs shift operation on its inputs before sending the results out onto a data bus. For the example shown in Figure 5-1, the shifter receives the output of the adder, perform a shift operation ranging from no shifting to 3-bit shift, before sending the results onto another 4-bit bus back to the register array.

5.3.1 Requirements For an n-bit Shifter

For the 4-bit shifter shown in Figure 5-9, four mutually *exclusive* shift control inputs are required to select between different shifting operations available as shown by the truth table.

Shift Control Inputs				Outputs				Remarks
sh_0	sh_1	sh_2	sh_3	Out_0	Out_1	Out_2	Out_3	
1	0	0	0	In_0	In_1	In_2	In_3	No Shift
0	0	0	1	In_1	In_2	In_3	In_0	Shift left by 1 bit
0	0	1	0	In_2	In_3	In_0	In_1	Shift left by 2 bits
0	1	0	0	In_3	In_0	In_1	In_2	Shift left by 3 bits

The shifting of bits is done by turning on the CMOS transmission gate to re-direct the input bits onto the output bus.
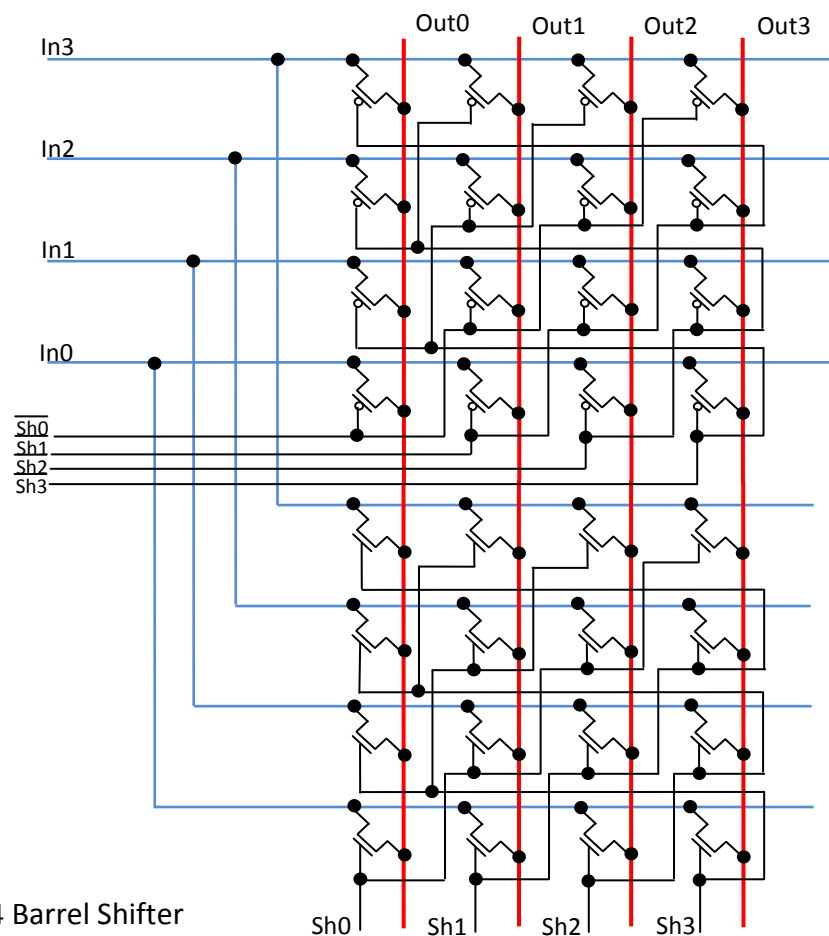

Figure 5-9   4x4 Barrel Shifter

Figure 5-9 shows a barrel shifter made up of switch arrays. The interbus switches are connected in a staircase fashion to facilitate the shift operation. The shifter does not have storage capability and its structure is of high regularity, giving rise to ease of layout.

5.4 DESIGN OF REGISTER ARRAY

Registers are memory/storage elements and can be used to store single bit data. It can be achieved using a variety of means. For dynamic shift registers, capacitive means are applied in the storing of data. In the case of static shift registers, clock signals are required to synchronize the transfer of data into the registers, hence bi-stable devices such as flip-flops are used.

5.4.1 Dynamic Shift Register Cell

Figure 5-10 and Figure 5-11 show basic dynamic storage cell implemented using CMOS technology.
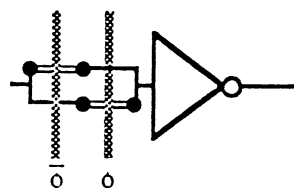

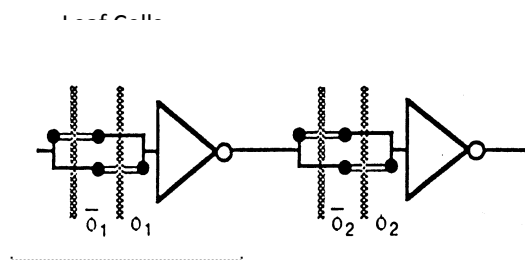Figure 5-10   Basic Inverting Dynamic Storage Cells

Figure 5-11   Non-inverting Dynamic Storage Cell

In the case of non-inverting dynamic storage cell, on ϕ_1 , data is clocked into inverter 1 and on ϕ_2 , true data is presented at the output of inverter 2.

5.4.1.1 Operation of 4-bit Dynamic Shift Register Cell

Figure 5-12 shows the implementation of a dynamic 4-bit shift register using 4 non-inverting dynamic storage cells cascaded as shown. Data entered into the register are transferred on the triggering edge of the clock pulse.
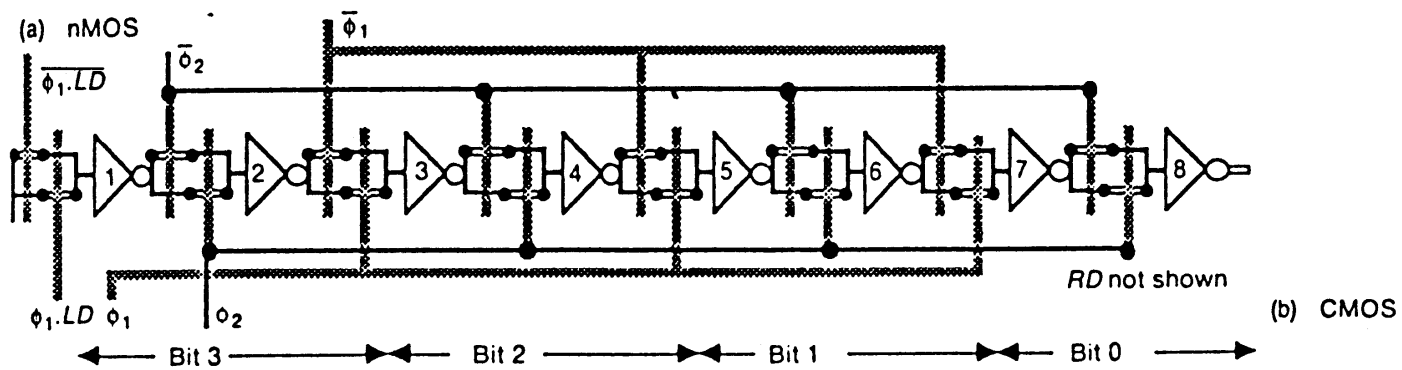
Figure 5-12 4-bit Dynamic Shift Register

Data bits are shifted in when $\phi.LD$ is present, one bit being entered on each ϕ_1 signal (provided *LD* is at logic 1). Each bit is stored in C_{g1} as it is entered, and then transferred complemented into C_{g2} during the next ϕ_2. Thus, after a ϕ_1 followed by ϕ_2 signal, the stored bit is present at the output of inverter 2. On the next ϕ_1, the next input bit is stored in C_{g1} and simultaneously the first bit stored is passed on to inverter pair 3 and 4 by being stored in C_{g3}, and so on. Once 4 bits are stored, data can be made available in either serial or parallel form.
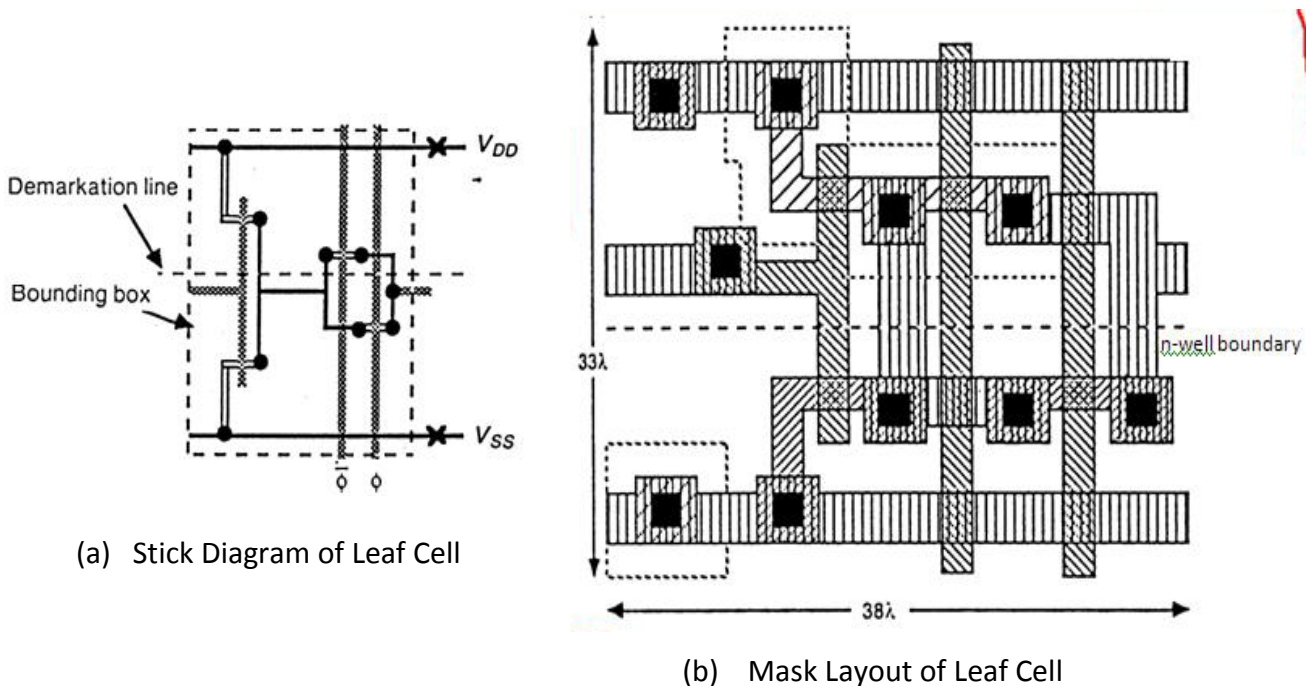

(a) Stick Diagram of Leaf Cell

(b) Mask Layout of Leaf Cell

Figure 5-13   Leaf Cell of Inverting Dynamic Storage Cell

5.5 DESIGN OF STATIC AND DYNAMIC RAM

Random Access Memories (RAM) are volatile memories because data written into the storage circuits are lost when power is disconnected. It is used for storing data that are frequently changing. They are classified into two broad categories namely, Static RAM and Dynamic RAM.

5.5.1 RAM Array Architecture

Figure 5-14 shows a RAM array architecture. The address bus ($A_0 - A_{13}$) provides inputs to the row decoder and the column decoder to select the desired row and column memory cell in the array. The pulse generator provides the timing for turning on the pre-charge circuitry. The pre-charged circuitry provides pre-charging of the data bus in the columns. There is one sense amplifier located at the bottom of each column in the array.
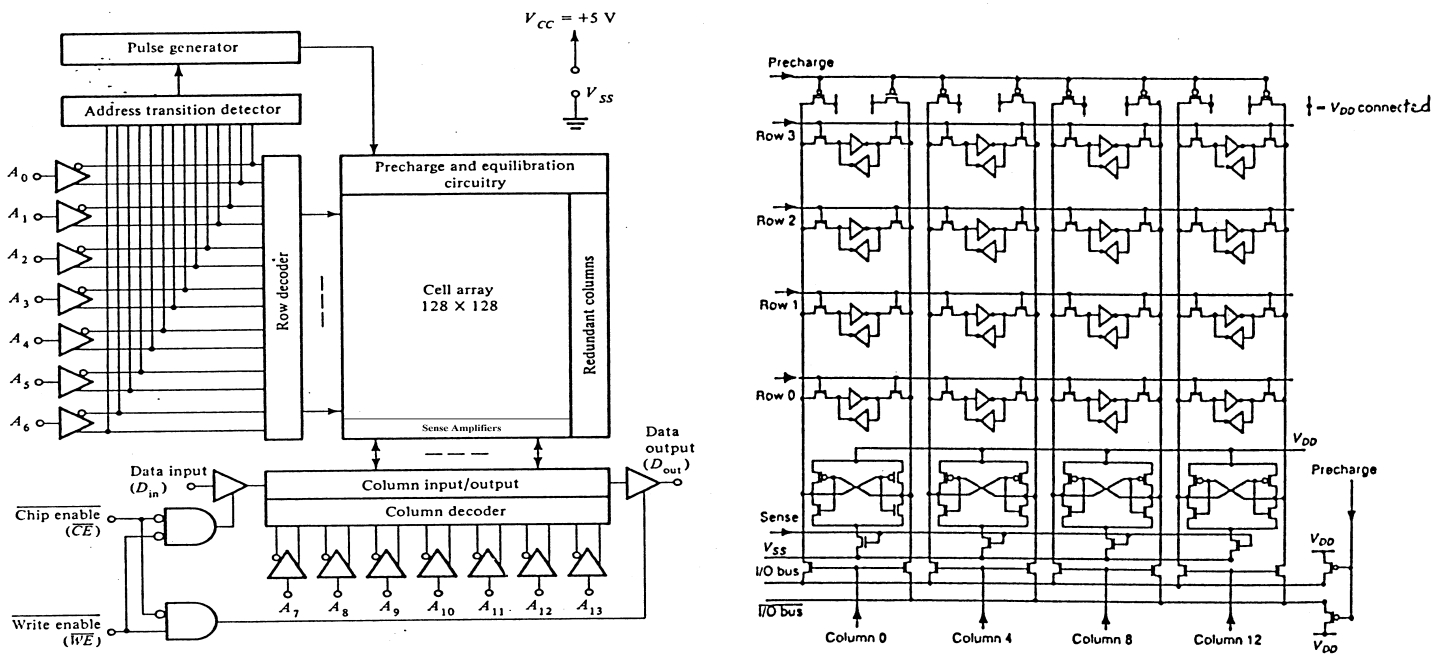

Figure 5-14   Basic Memory Array Architecture

5.5.1.1 Pre-charge Bus

Bus structures carrying data signals are generally long and connected to a large number of memory cells or subsystems, thus the bus capacitances are high and propagation of signals are slow. The effects of bus capacitance can be limited by using the pre-charge bus, thus enhancing the speed of the signal propagation in the bus.

Precharging is normally done during the inactive cycle of the clock, allowing the bus to be charged to V_{dd}, hence time is saved in the normal operation.

5.5.2 Static RAM (SRAM)

Data stored in static RAM are held by cross-coupled devices and are maintained for as long as the power is on. It has low packing density because it requires 6 transistors to form a basic 1-bit cell. The basic cell consists of two cross-coupled bistable circuits (INV X and INV Y) and two transistors for ROW select (T_5 and T_6).
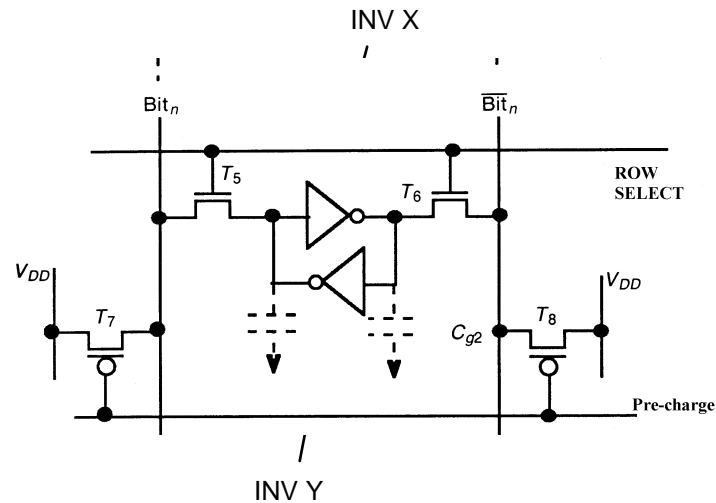
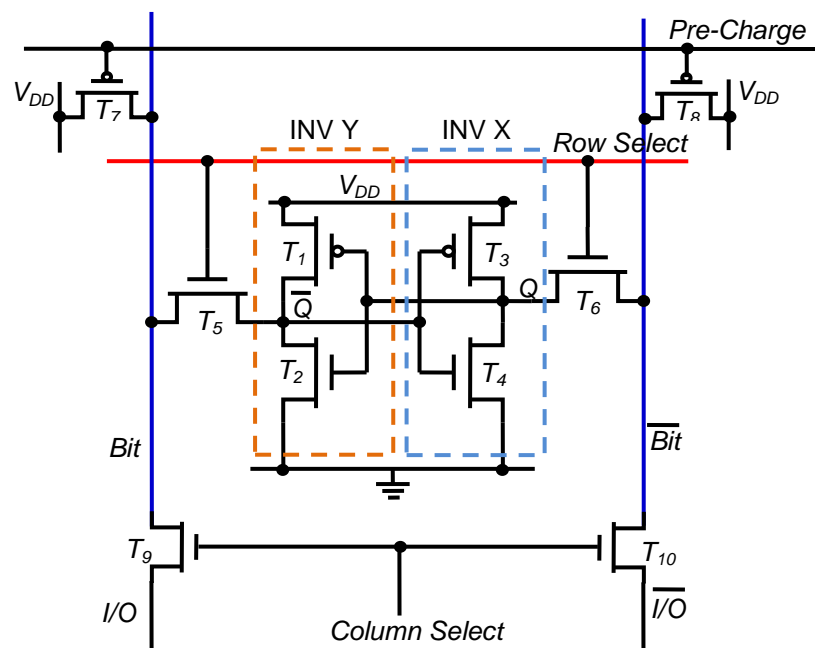Figure 5-15   6-Transistors Static Memory Cell (Logic View)

Figure 5-16   6-Transistors Static Memory Cell

(i)   Write Operation

1.   Before operation takes place, that is CLK=0, both Bit and $\overline{\text{Bit}}$ lines are precharged to "H" via T_7 and T_8.

2.   Data to be written is placed on the I/O bus and its complementary data is placed on the $\overline{\text{I/O}}$ bus.

3.   When the Column Select is Enabled, data are transferred to the Bit and $\overline{\text{Bit}}$ lines.

4.   Enabling the Row Select will cause the data on the Bit to be stored in INV X via T_5 and the complementary data on $\overline{\text{Bit}}$ to be stored in INV Y via T_6.

To write a "H" logic,

1.   Precharge Bit and $\overline{\text{Bit}}$ lines to High.

2.   Place a "H" logic on the I/O bus and a "L" logic on the $\overline{\text{I/O}}$ bus.

3.   Enable the Column Select. These logics will be presented to the Bit line $\overline{\text{Bit}}$ line respectively. A logic "L" on the $\overline{\text{Bit}}$ line causes it to discharge.

4.   Enable the Row Select. The logic state on the Bit and $\overline{\text{Bit}}$ lines will be presented to INV X and INV Y respectively.

The two inverters interlock their states and stabilized. The data remains for as long as the power is ON or when new data is wrote into it.

(ii)   Read Operation

1.   Before operation takes place, that is CLK=0, both Bit and $\overline{\text{Bit}}$ lines are precharged to "H" via T_7 and T_8.

2.   When the Row Select is Enabled, output of INV X and INV Y will be connected to the $\overline{\text{Bit}}$ and Bit lines respectively.

3.   Enabling the Column Select will cause the data on the Bit and $\overline{\text{Bit}}$ lines to be presented to the I/O and $\overline{\text{I/O}}$ bus respectively.

To read a "H" logic (previously stored in INV X),

1.   Precharge Bit and $\overline{\text{Bit}}$ lines to High.

2.   Enable the Row Select. A "L" at output of INV X will be presented to $\overline{\text{Bit}}$ line while a "H", output of INV Y, will be presented to the Bit line. The logic "L" on the output of INV X causes the $\overline{\text{Bit}}$ line to discharge.

3.   Enable the Column Select. The logic "H" on the Bit and the logic "L" on the $\overline{\text{Bit}}$ lines are impressed onto the I/O and $\overline{\text{I/O}}$ bus respectively.

5.5.2.1 Latched-Based Sense Amplifier

A sense amplifier is found at the bottom of each column of the memory array. It is used to increase the current sinking capability of the selected cell and is controlled by the Sense signal, S. Together with the sense amplifier, the pull-down transistors in the 6-T cells can be of minimum size without affecting speed of operation.
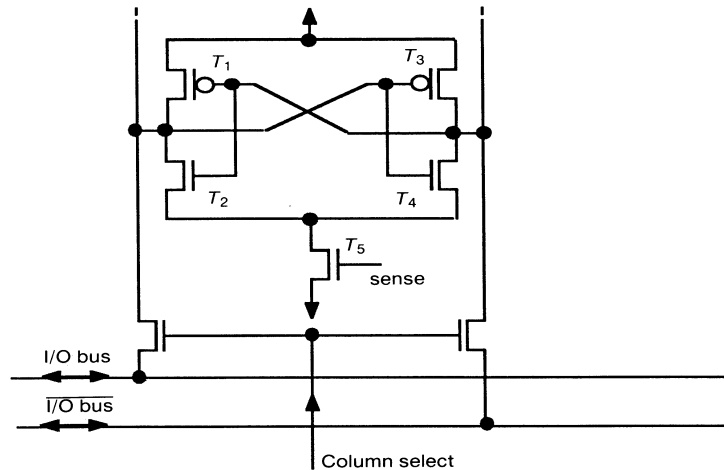

Figure 5-17   Sense Amplifier Circuit at Bottom of RAM Array Column

During read operation, when the Sense signal is inactive, the state of the Bit and $\overline{\text{Bit}}$ lines are reflected on the sense amplifier transistors T_3, T_4 and T_1, T_2 respectively. Once the Sense signal goes "H', the charges on the Bit line will discharge to V_{ss} through T_2 and T_5 if the cell is holding a logic "L". The discharging of the Bit line via T_5 provides extra current sinking capability in addition to that available in the selected memory cell for data lines. Thus, the pull-down transistors in the 6-T cells can be of minimum size without affecting the speed of operation.

5.5.3 Dynamic RAM (DRAM)

Data stored in dynamic RAM uses capacitive means (gate capacitance or capacitor) hence periodic refreshing is required. Although it requires refreshing circuitry, DRAM enjoys a high packing density since its basic cell can be formed with 1 to 4 transistors.

5.5.3.1 One Transistor DRAM Memory (1-T DRAM)

The data is stored in a capacitor, C_s, that is built within the cell structure. The transistor, T, acts to isolate the stored charge from the data line except for read or write operation. The C_L represents the large parasitic capacitance and load capacitance that is present in the bit line B.
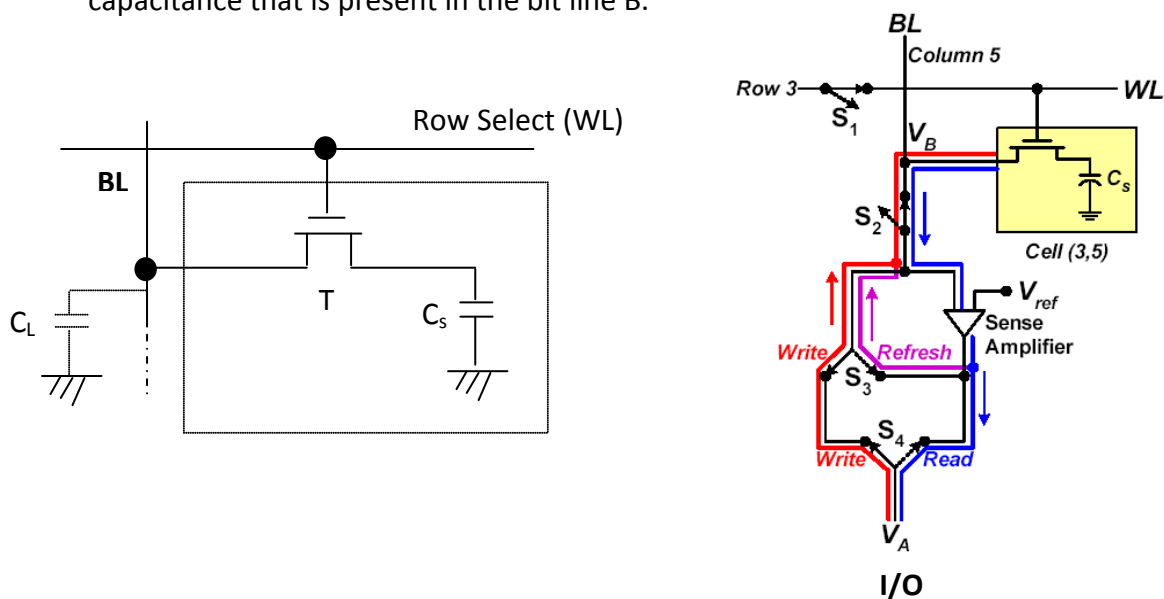

Figure 5-18   1-T Memory Cell

(i) <u>Write Operation - WEN = 1 (S3, S4)</u>

Before the start of a write operation, the BL line is pre-charged to "H", that is, C_L is pre-charged to V_{dd}.

To begin a write operation, the WEN line is set to 1, thus switch S3 and S4 are in the position as shown.

Data to be written is impressed on the I/O bus. The Column select (S2) connects the appropriate BL line to the I/O bus while the Row select (S1) connects the BL line to C_s. C_s is then charged or discharged accordingly to the value held on the BL line.

(ii)   Read Operation – WEN = 0 (S3, S4)

Before the start of a read operation, the BL line is pre-charged to "H", that is, C_L is pre-charged to V_{dd}.

To perform a read operation, the WEN line is set to 0, thus switch S3 and S4 are in the position as shown.

To read a "L" that was previously stored in C_S, when the Row Select (S1) is activated, C_S will be shorted to the BL line. This causes C_S to charge up while C_L to discharge and V_{CL} to drop significantly. The sense amplifier, which is connected to the bottom of the column, will detect this drop in V_{CL}, amplifies this voltage drop to give a "L" value on the I/O bus, and at the same time impressed it on the BL line. This causes both C_L and C_S to discharge to "L" (back to original stored value).

To read a "H" that was previously stored in C_S, when Row Select is activated, C_S will charge up slightly, thus V_{CL} drops slightly. This slight drop in V_{CL} is detected by the sense amplifier, which amplifies this signal to give a "H" on the I/O bus, and at the same time impressed it on the BL line. This causes both C_S and C_L to charge up to V_{cc}.

It can be observed that the reading operation is destructive to the charge stored, however it also refreshes the memory.

The 1-T memory cell has low noise immunity due to logic level output being dependent on the detection of voltage drop in V_{CL}. However, it provides high packing density and high speed of operation.

5.4.3.2 Three Transistors DRAM Memory

The basic memory cell of a 3-T DRAM consists of 3 transistors. The data is stored using the gate capacitance of transistor T_2 as shown in the Figure 5-19.
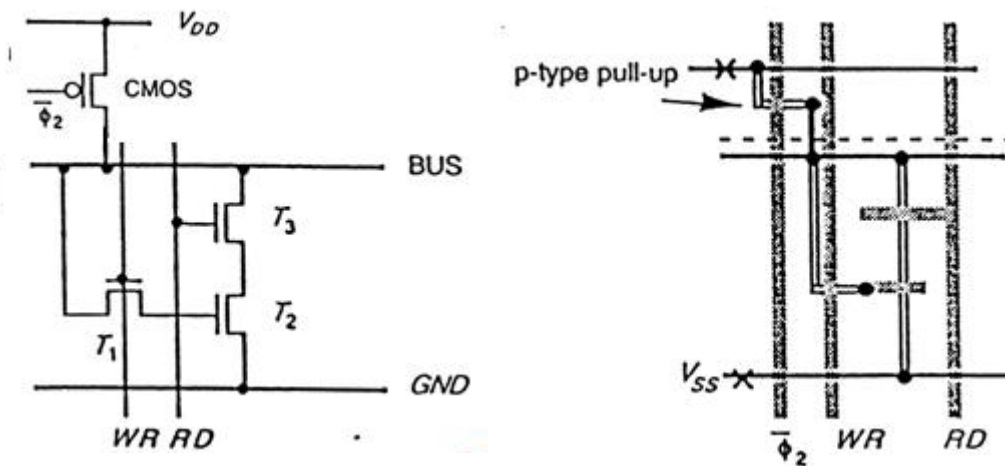

Figure 5-19   3-T DRAM cell and Stick Diagram

(i)   <u>Write Operation</u>

Bus is precharged to "H". (Data to be stored is placed on the I/O line. When the Column Select is turned ON, the value on the I/O line will be placed on the BUS line.) Setting WR = "H" and RD = "L", T_1 will be ON and T_3 will be OFF, thus the logic level on the Bus is communicated to the gate of T_2.

(ii)   <u>Read Operation</u>

Bus is precharged to "H" before setting WR = "L" and RD = "H". If the stored value is "H", both T_2 and T_3 will be "ON" thus the BUS will be pulled down to "L" via T_2 and T_3. (When Column Select is ON, the value on the BUS line will be impressed onto the I/O line.)

On the other hand, if the stored value is "L", then T_2 will be OFF and T_3 will turn ON, and the BUS will remain at "H" (its pre-charged value).

It can be observed that the complement of the stored value is being read onto the BUS. Thus, for non-inverted output, an inverter is needed before the actual output stage.

5.4.3.3 Four Transistor DRAM Memory
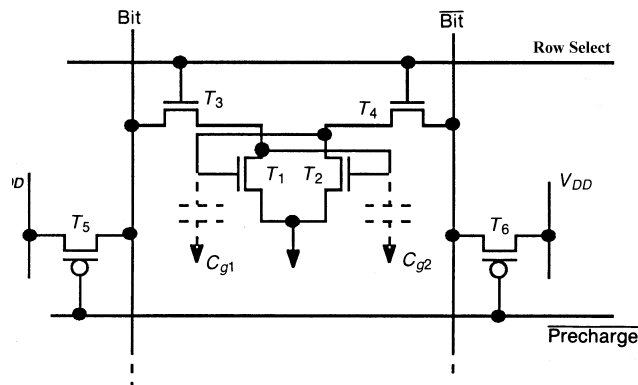
Figure 5-20 shows a 4-transistor DRAM implementation.

Figure 5-20 4-T DRAM Memory Circuit

(i)   <u>Write Operation</u>

Both Bit and $\overline{\text{Bit}}$ lines are precharged to "H" when T_5 and T_6 are "ON". To write a logic "L", the Bit line is forced to "L" by the I/O bus while the $\overline{\text{Bit}}$ line remains "H". When the Row Select turns T_3 and T_4 on, the charge at the gate capacitance, C_{g2}, will discharge to a "L" while C_{g1} is charged to a "H".

(ii)   <u>Read Operation</u>

Both Bit and $\overline{\text{Bit}}$ lines are precharged to "H" when T_5 and T_6 are "ON". To read a "L", when the Row Select is activated, the Bit line discharges to "L" through T_3 and T_1 while $\overline{\text{Bit}}$ remains at "H". Thus, a "L" is presented to the I/O bus through the Bit line.

During read operation, the sense amplifier at the bottom of the column is used to increase the current sinking capability of the selected cell

5.4.3.4 Dynamic Storage Element Comparison

DRAM enjoys high packing density. Data is stored at the gate capacitance of the transistor and requires periodic refreshing.

The 1-T DRAM has the highest packing density and operating speed. Power consumption is limited to writing and reading operations. Data is stored in capacitors and requires periodic refreshing.

The 3-T DRAM has lower packing density. Power is consumed when RD is "H" and data stored is "H". Data is stored at the gate capacitance and requires periodic refreshing.

The 4-T DRAM has the lowest packing density. Power is consumed regardless of the logic state as it supports complementary output. Data is stored at the gate capacitance and requires periodic refreshing.

Review Questions

Question 1

With regard to the Figure 5-21,
(a)   draw the stick diagram and its transistor level schematic.
(b)   state the logic function at O/P. If E = "L", what is the state of O/P ?
(c)   with reference to part (b), suggest modifications, if any, to eliminate ambiguity at the output.
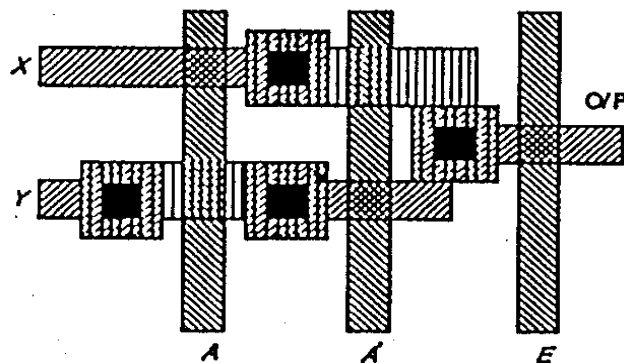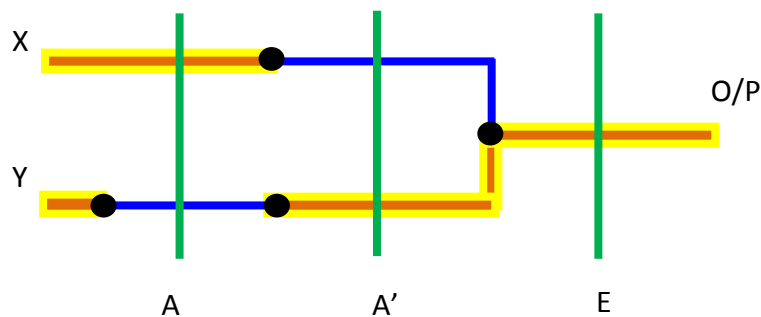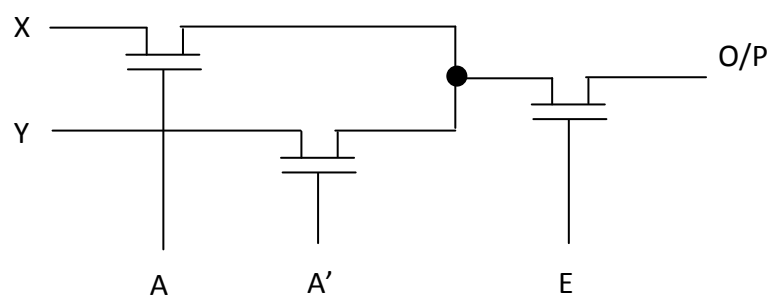(d)   draw the stick diagram of the modified circuit using CMOS technology.

Figure 5-21

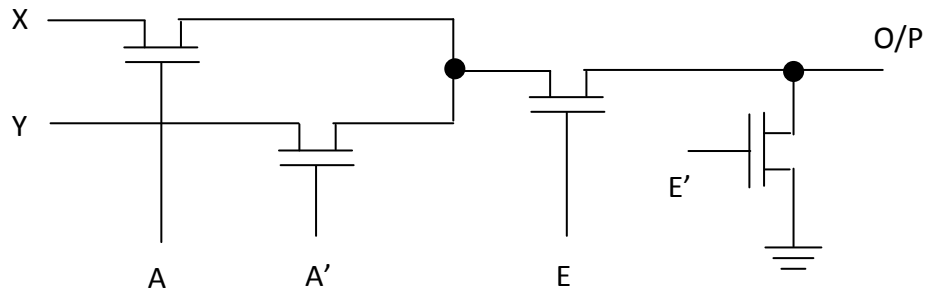## Solution to Q1

(a)   Stick Diagram

Transistor Level Schematic

(b)   O/P = (A X + A' Y) E

If E = 'L', from the schematic, O/P = unknown (floating).

(c)   Add a transistor to tie the output to ground when E = 'L'.

(d)   Modified Circuit

Question 2

Construct the colour coded stick diagram to represent the design of an integrated CMOS structure to decode the three input lines E_0, E_1 and E_2 into eight output lines Z_0, $Z_1...Z_7$, in accordance with the truth table given in Table 5-22.

Table 5-22

Inputs			Outputs							
E_2	E_1	E_0	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Solution to Q2

From the truth table, the output equations for the 3-to-8 decoder are :-

$$\overline{Z_0} = \overline{E_2}\,\overline{E_1}\,\overline{E_0} \qquad \Rightarrow \qquad Z_0 = \overline{\overline{E_2}\,\overline{E_1}\,\overline{E_0}}$$

$$\overline{Z_1} = \overline{E_2}\,\overline{E_1}\,E_0 \qquad \Rightarrow \qquad Z_1 = \overline{\overline{E_2}\,\overline{E_1}\,E_0}$$

$$\overline{Z_2} = \overline{E_2}\,E_1\,\overline{E_0} \qquad \Rightarrow \qquad Z_2 = \overline{\overline{E_2}\,E_1\,\overline{E_0}}$$

$$\overline{Z_3} = \overline{E_2}\,E_1\,E_0 \qquad \Rightarrow \qquad Z_3 = \overline{\overline{E_2}\,E_1\,E_0}$$

$$\overline{Z_4} = E_2\,\overline{E_1}\,\overline{E_0} \qquad \Rightarrow \qquad Z_4 = \overline{E_2\,\overline{E_1}\,\overline{E_0}}$$

$$\overline{Z_5} = E_2\,\overline{E_1}\,E_0 \qquad \Rightarrow \qquad Z_5 = \overline{E_2\,\overline{E_1}\,E_0}$$

$$\overline{Z_6} = E_2\,E_1\,\overline{E_0} \qquad \Rightarrow \qquad Z_6 = \overline{E_2\,E_1\,\overline{E_0}}$$

$$\overline{Z_7} = E_2\,E_1\,E_0 \qquad \Rightarrow \qquad Z_7 = \overline{E_2\,E_1\,E_0}$$

From the output equation, it is realised that each individual output can actually be implemented using a 3-input NAND gate. Hence, using CMOS technology, the stick diagram for the 3-to-8 decoder is as shown below.
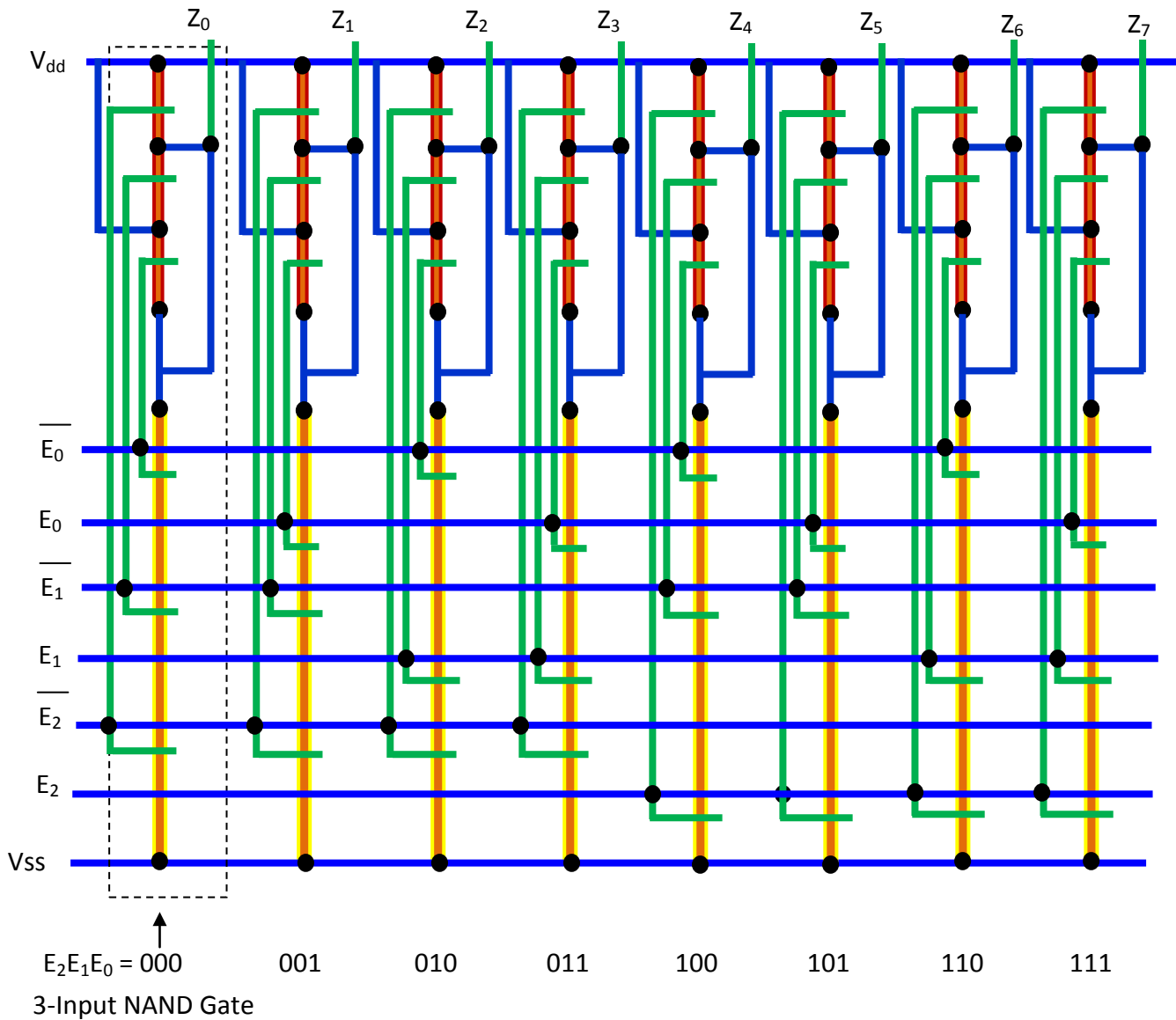
Question 3

Multiplexers and demultiplexers are common block found in digital circuits design.

(a)   A demultiplexer is a device that takes in one input and direct it to the respective output based on a set of control signals. Table 5-23 shows the truth table of a 1-to-4 demultiplexer.

Derive, using Karnaugh Maps or otherwise, the boolean equation of the outputs.

Table 5-23

Inputs		Output			
S_1	S_0	D_3	D_2	D_1	D_0
0	0	0	0	0	In
0	1	0	0	In	0
1	0	0	In	0	0
1	1	In	0	0	0

(b)   A multiplexer is a device that has more than one input and direct it to the respective output based on a set of control signals. For a 4-to-1 multiplexer, 2 select signals S_1 and S_0 are required. For each combination, the input is presented to one of 4 outputs.

The boolean equation given below is that of the output of a 1-to-4 multiplexer.
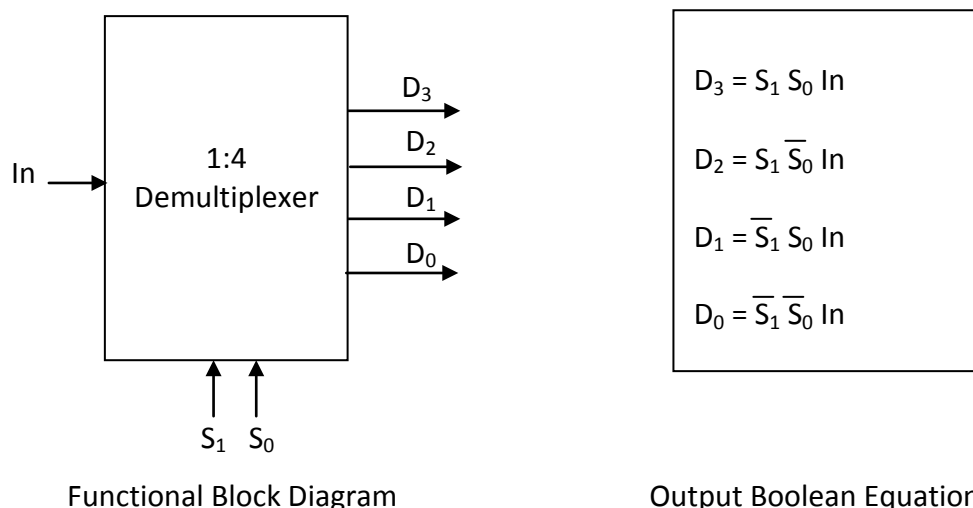
$$Z = \overline{S_1}\,\overline{S_0}I_0 + \overline{S_1}S_0I_1 + S_1\overline{S_0}I_2 + S_1S_0I_3$$

Based on the given equation, draw the transistor level circuitry of **Z** using CMOS *SWITCH* logic concept. Assume *negated* signals are readily available.
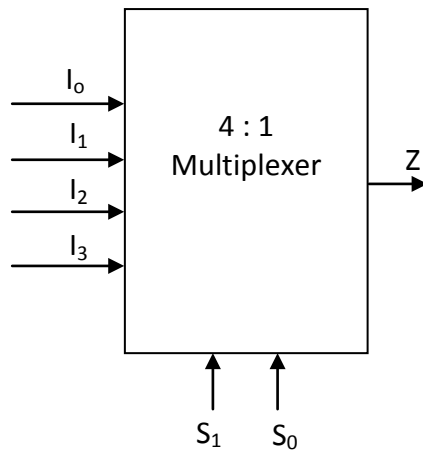
(c)   Draw the color coded stick diagram of part (b).
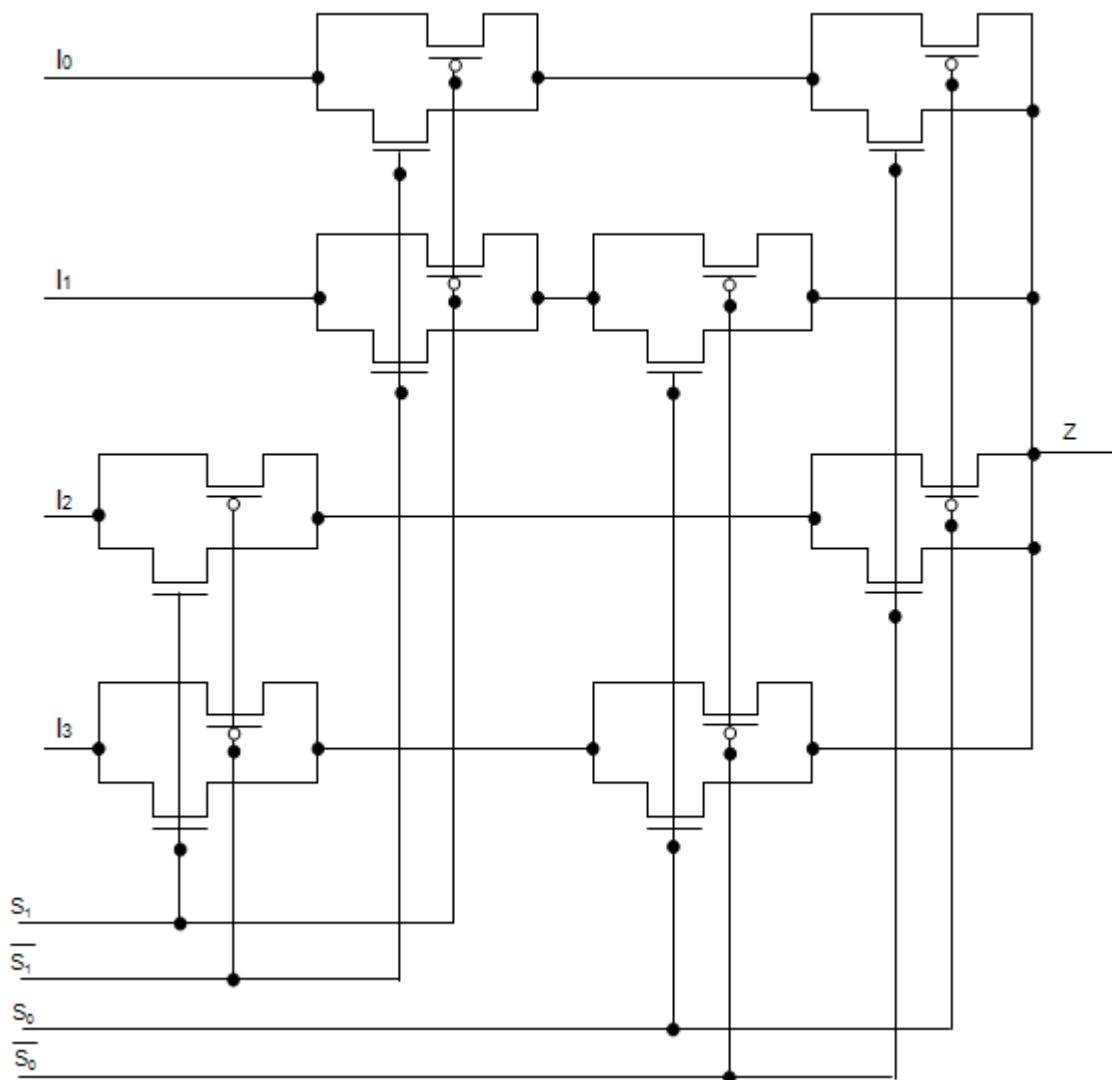
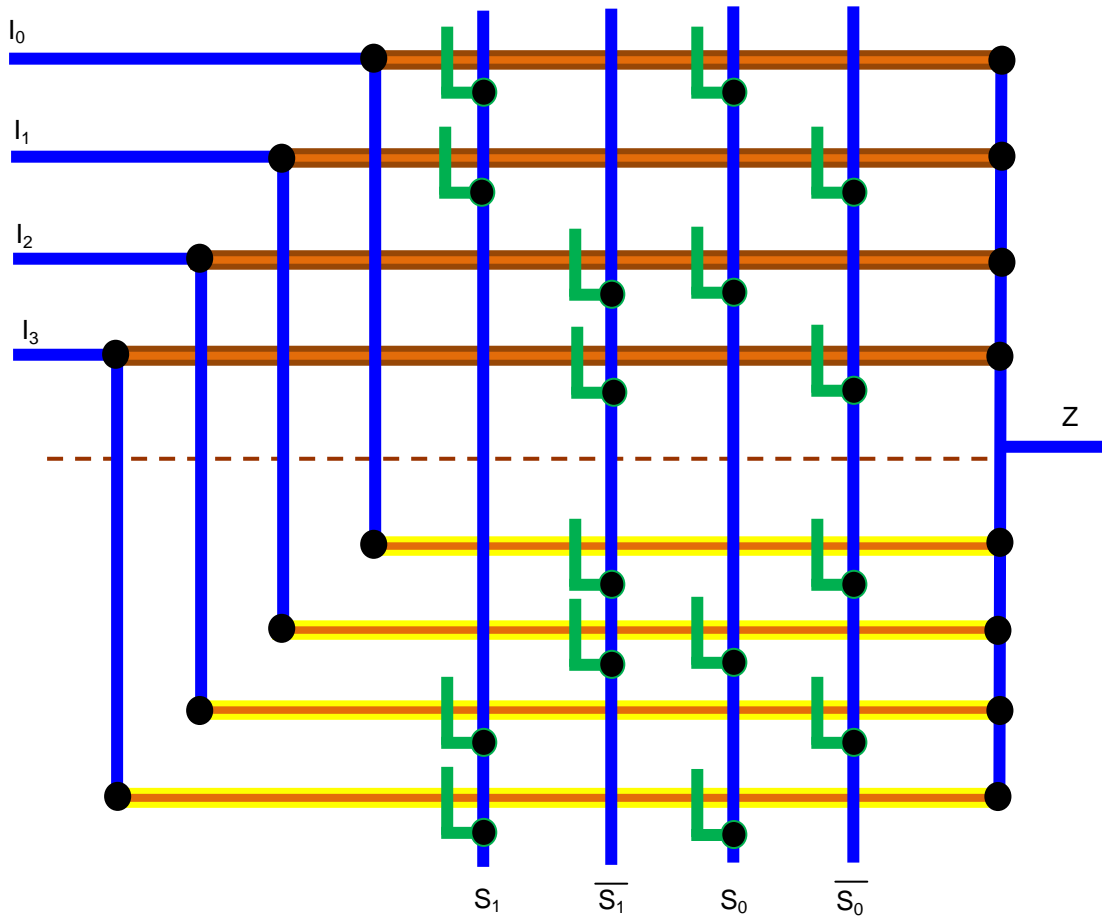**Solution to Q3**

(a)   Demultiplexer

$D_3 = S_1 S_0$ In

$D_2 = S_1 \overline{S_0}$ In

$D_1 = \overline{S_1} S_0$ In

$D_0 = \overline{S_1}\,\overline{S_0}$ In

Functional Block Diagram   Output Boolean Equations

(b) $Z = \overline{S_1}\,\overline{S_0}\,I_0 + \overline{S_1}\,S_0\,I_1 + S_1\,\overline{S_0}\,I_2 + S_1\,S_0\,I_3$

Transistor Level Schematic (Using Switch Logic)

(c)

Color Coded Stick Diagram of a 4-to-1 Multiplexer

Question 4

A priority encoder is a combinational circuit in which each input is assigned a priority with respect to the other inputs, and the output code generated any time is that associated with the highest priority input then the present. With the truth table,
(a)   work out the logic expression at the outputs, P_1 and P_0.
(b)   show the transistor level implementation of P_1 and P_0, using CMOS technology.
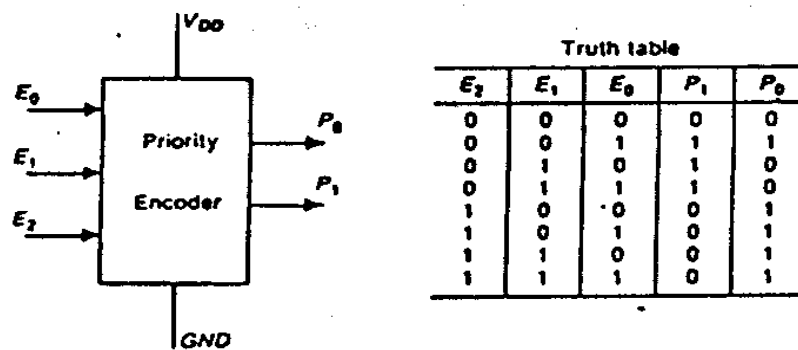(c)   construct its colour coded stick diagram.

Truth table

E_2	E_1	E_0	P_1	P_0
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

Figure 5-24

Solution to Q4

Using SOP,

$$P_1 = \overline{E_2}\,\overline{E_1}\,E_0 \; + \; \overline{E_2}\,E_1\,\overline{E_0} \; + \; \overline{E_2}\,E_1\,E_0$$

$$= \overline{E_2}\,E_0\,(\overline{E_1} + E_1) + \overline{E_2}\,E_1\,\overline{E_0}$$

$$= \overline{E_2}\,E_0 + \overline{E_2}\,E_1\,\overline{E_0}$$

$$= \overline{E_2}\,(E_0 + \overline{E_0}\,E_1)$$

Using the Boolean rule of $A + \overline{A}\,B = A + B$, thus
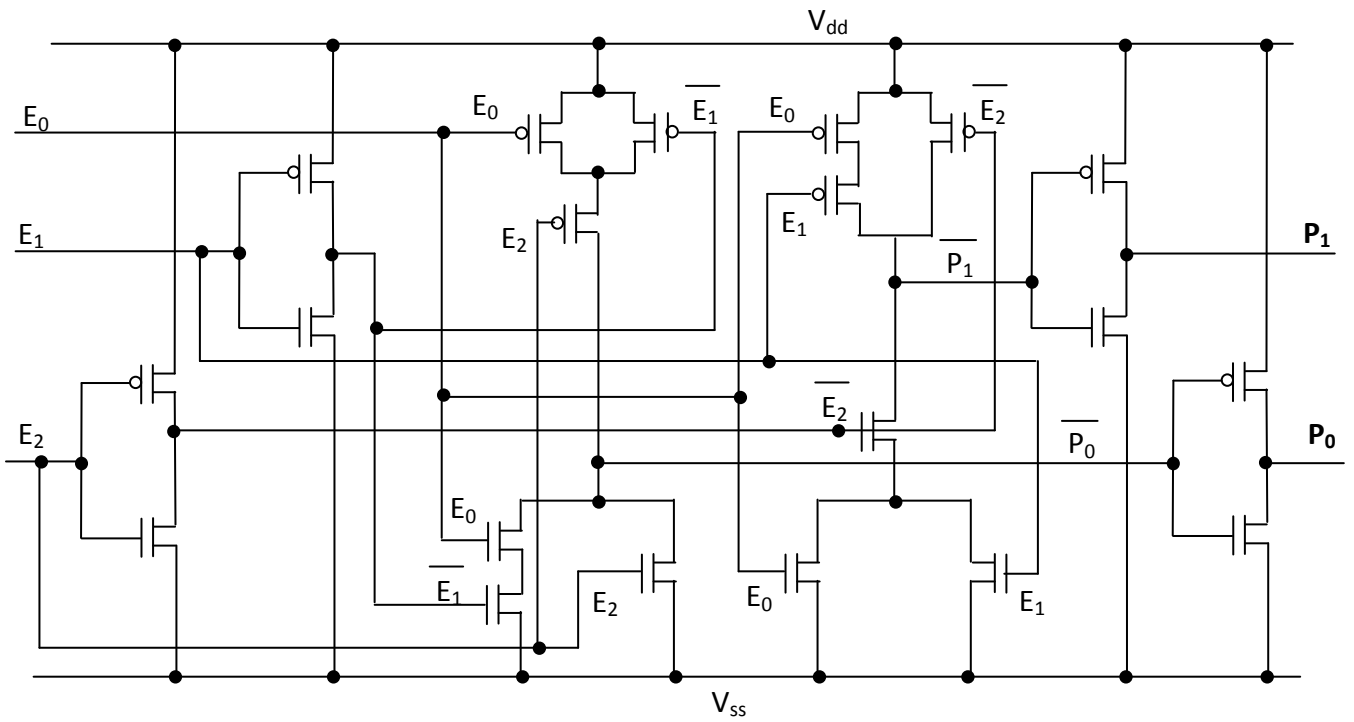
$$\mathbf{P_1 = \overline{E_2}\,(E_0 + E_1)}$$

Similarly,

$$P_0 = \overline{E_2}\,\overline{E_1}\,E_0 \; + \; E_2\,\overline{E_1}\,\overline{E_0} \; + \; \overline{E_2}\,E_1\,E_0 \; + \; E_2\,\overline{E_1}\,E_0 \; + \; E_2\,E_1\,E_0$$

$$= \overline{E_2}\,\overline{E_1}\,E_0 \; + \; E_2\,\overline{E_1}\,(E_0 + \overline{E_0}) + E_2\,E_1\,(E_0 + E_0)$$

$$= \overline{E_2}\,\overline{E_1}\,E_0 \; + \; E_2\,(E_1 + \overline{E_1})$$

$$= \overline{E_2}\,\overline{E_1}\,E_0 \; + \; E_2$$

Using the Boolean rule of $A + \overline{A}\,B = A + B$, thus
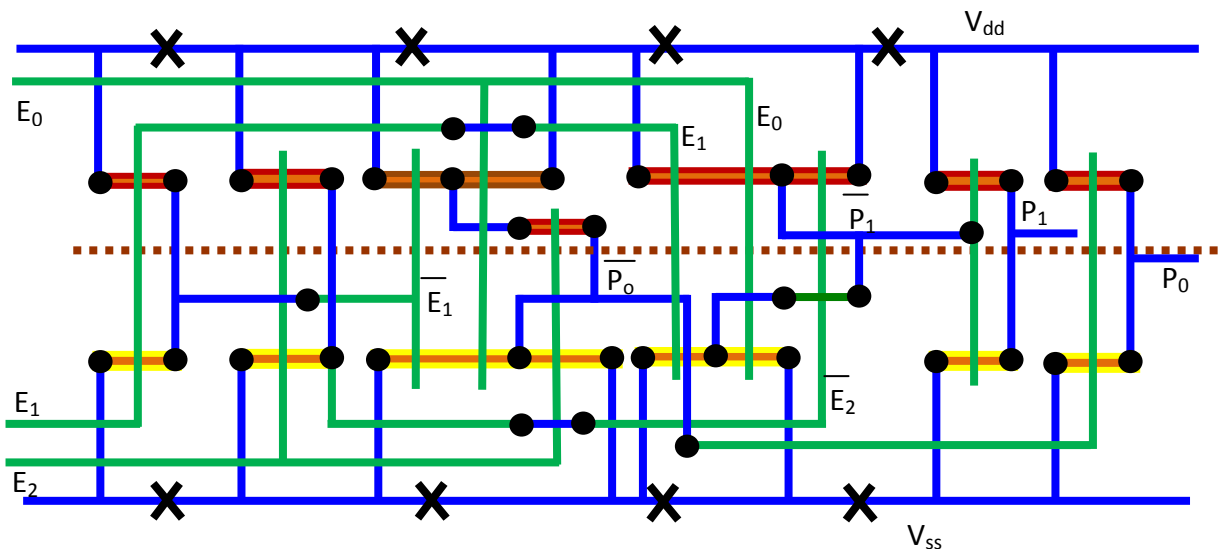
$$\mathbf{P_0 = E_2 + (\overline{E_1}\,E_0)}$$

(b)   Transistor Level Schematic

CMOS Implementation Using Complex Gate Concept

(c)   Color Coded Stick Diagram

Question 5

Table 5-25 shows the truth table of a 1-bit adder. From the truth table,

(a)   derive, using Karnaugh Maps or otherwise, the boolean equation for the carry, C_k.

(b)   using CMOS complex gate implementation, draw the transistor level circuitry of C_K:
$$C_K = (A_K \oplus B_K) + A_K + B_K$$

(c)   draw the colour-coded stick diagram of part (b).

Table 5-25

Inputs			Outputs	
A_k	B_k	C_{k-1}	S_k (Sum)	C_k (Carry)
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

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Solution to Q5

(a) $\mathbf{C_k} = A_k\,B_k\,\overline{C_{k-1}} + \overline{A_k}\,B_k\,C_{k-1} + \overline{A_k}\,B_k\,C_{k-1} + A_k\,B_k\,C_{k-1}$

$\mathbf{C_k} = A_k\,B_k\,(\overline{C_{k-1}} + C_{k-1}) + C_{k-1}\overline{(A_k\,B_k + \overline{A_k}\,B_k)}$

$\mathbf{C_k} = A_k\,B_k + \overline{(\overline{A_k}\,B_k + A_k\,\overline{B_k})}\,C_{k-1}$

$\mathbf{C_k} = A_k\,B_k + (A_k \oplus B_k)\,C_{k-1}$

(b)
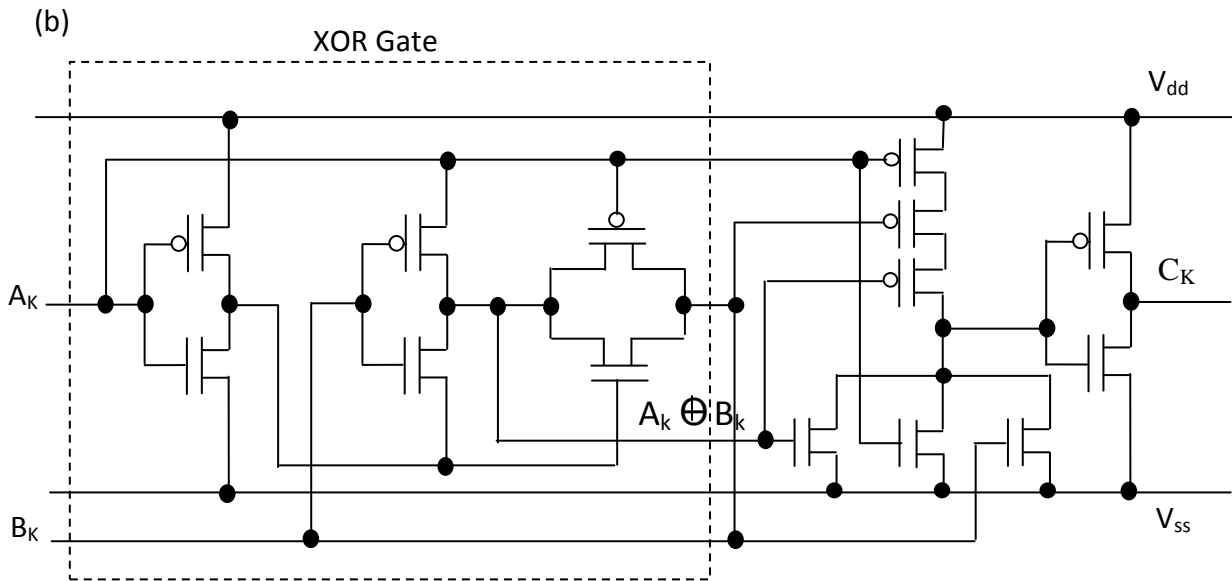
CMOS Complex Gate Implementation

(c)   Color Coded Stick Diagram
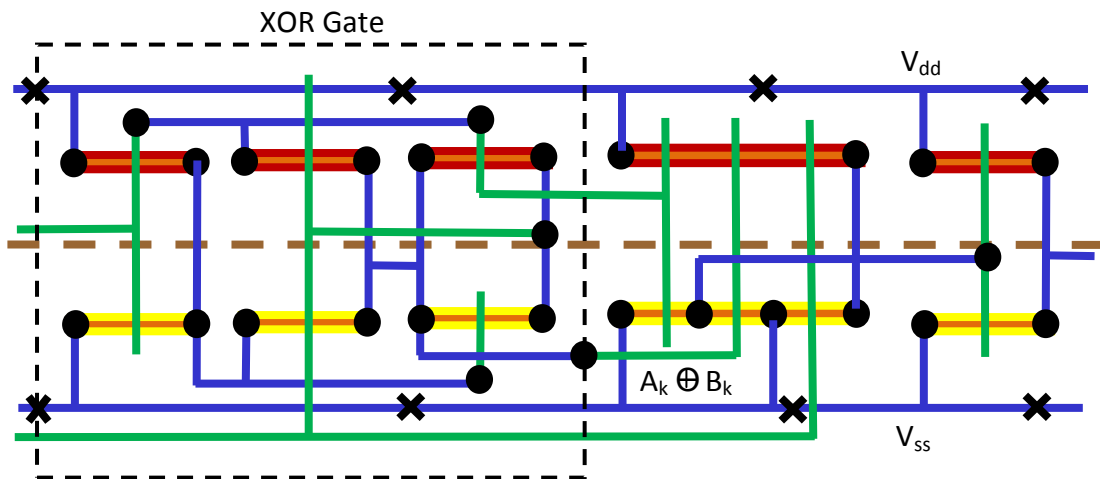
Question 6

Draw the structure of a 6-transistor Static RAM cell with the sense amplifier.
(a)   Explain its read and write operation.
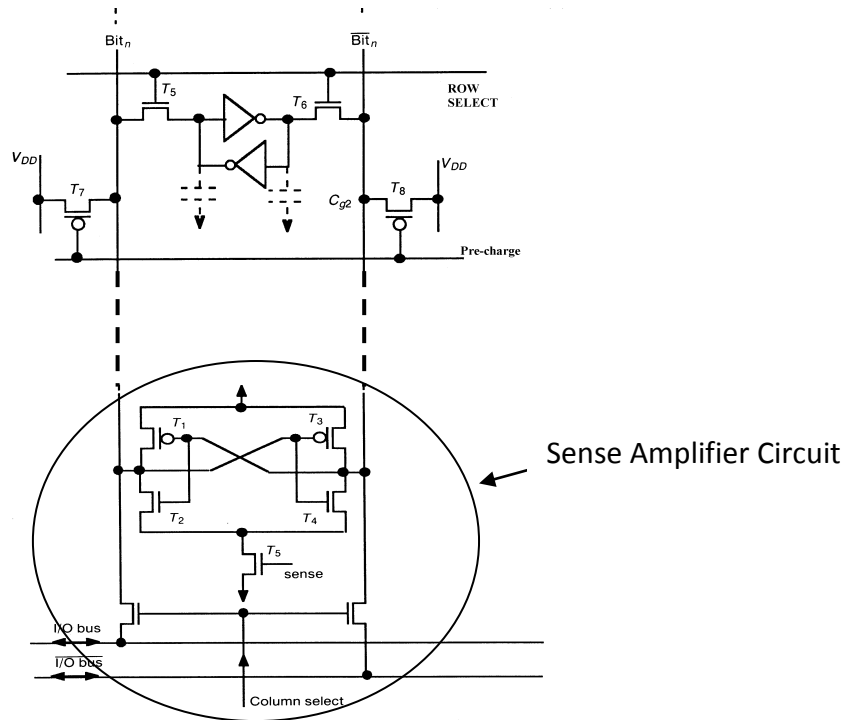(b)   Explain the need for the sense amplifier circuit.

Solution to Q6

Figure Q6

(a)(i)   Write Operation

Both Bit and $\overline{Bit}$ are precharged to "H" before operation takes place. Row Select (T_5 and T_6) and Column Select (Figure Q6) are used to select the required memory cell in the array.

To write a "H" logic, the logic is placed on the I/O bus, presented to the Bit line and a "L" logic is placed on the $\overline{I/O}$ bus, and presented to the $\overline{Bit}$ line. This causes the $\overline{Bit}$ line to discharge. The two inverters interlock their states and stabilized. The data remains for as long as the power is ON or when new data is wrote into it.

(ii)   Read Operation

Both Bit and $\overline{\text{Bit}}$ lines are precharged to "H" before operation takes place. Row select and Column select are used to select the required memory cell in the array.

If the logic level stored is "H", $\overline{\text{Bit}}$ will discharge to "L" through T_6 and the pull-down transistor in INV X while the Bit line remains "H". The data presented to the I/O Bus is thus logic "H" and that on the $\overline{\text{I/O}}$ Bus is logic "L".

(b)   Sense Amplifier

A sense amplifier is found at the bottom of each column of the memory array. It is used to increase the current sinking capability of the selected cell and is controlled by the Sense signal. Thus, the pull-down transistors in the 6-T cells can be of minimum size without affecting speed of operation.

Question 7

Draw the structure of a 1-T DRAM cell and explain the read operation if:-
(a)   it initially stores a logic level of "0"
(b)   it initially stores a logic level of "1"

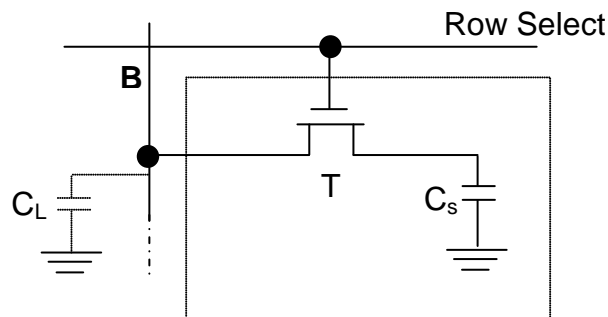**Solution to Q7**

Figure Q7

Read Operation

Before the start of a read operation, the B line is pre-charged to "H", that is, C_L is pre-charged to V_{cc}.

(a)   To read a "L" that was previously stored in C_S, when the Row Select is activated, C_S will be shorted to the B line. This causes C_S to charge up while C_L to discharge and V_{CL} to drop significantly. The sense amplifier, which is connected to the bottom of the column, will detect this drop in V_{CL}, amplifies this voltage drop to give a "L" value on the I/O bus, and at the same time impressed it on the B line. This causes both C_L and C_S to discharge to "L" (back to original stored value).

(b)   To read a "H" that was previously stored in C_S, when Row Select is activated, C_S will charges up slightly, thus V_{CL} drops slightly. This slight drop in V_{CL} is detected by the sense amplifier, which amplifies this signal to give a "H" on the I/O bus, and at the same time impressed it on the B line. This causes both C_S and C_L to charge up to V_{cc}.

It can be observed that the reading operation is destructive to the charge stored, however it also refreshes the memory.

The 1-T memory cell has low noise immunity due to logic level output being dependent on the detection of voltage drop in V_{CL}. However, it provides high packing density and high speed of operation.

Question 8

For a three transistor dynamic RAM, explain its read and write operations.

Solution to Q8
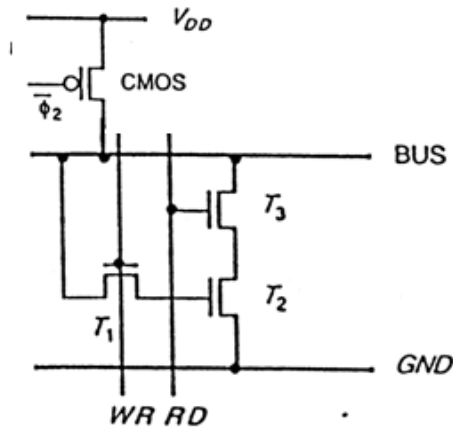

Figure Q8

(i)   Write Operation

Bus is precharged to "H" before setting WR = "H" and RD = "L". Data to be stored is impressed on the BUS.   With T_1 "ON" and T_3 OFF, the logic level on the Bus is communicated to the gate of T_2.

(ii)   Read Operation

Bus is precharged to "H" before setting WR = "L" and RD = "H". If the stored value is "H", both T_2 and T_3 will be "ON" thus the BUS will be pulled down to "L". On the other hand, if the stored value is "L", then T_2 will be OFF and T_3 will turn ON, and the BUS will remain at "H" (its pre-charged value).

It can be observed that the complement of the stored value is being read onto the BUS. Thus, for non-inverted output, an inverter is needed before the actual output stage.

Question 9

For a 4-T dynamic CMOS memory, explain its read and write operations.

Solution to Q9
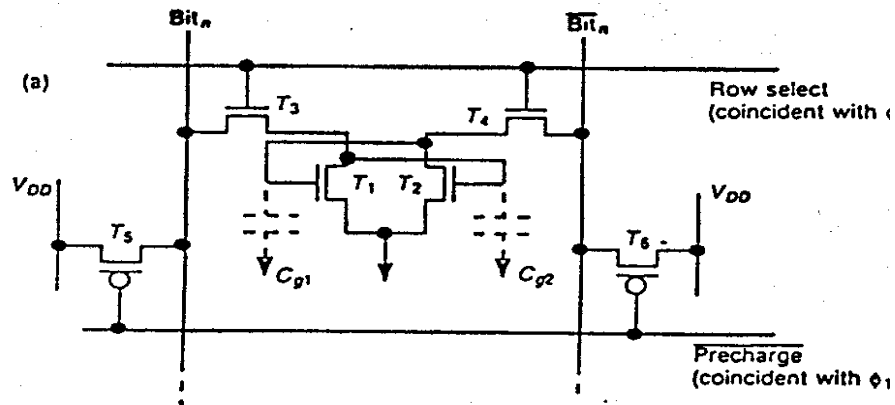
Write Operation

Both Bit and $\overline{\text{Bit}}$ lines are precharged to "H" when T_5 and T_6 are "ON". To write a logic "L", the Bit line is forced to "L" by the I/O bus while the $\overline{\text{Bit}}$ line remains "H". When the Row Select turns T_3 and T_4 on, the charge at the gate capacitance, C_{g2}, will discharge to a "L" while C_{g1} is charged to a "H".

Read Operation

Both Bit and $\overline{\text{Bit}}$ lines are precharged to "H" when T_5 and T_6 are "ON". To read a "L", when the Row Select is activated, the Bit line discharges to "L" through T_3 and T_1 while $\overline{\text{Bit}}$ remains at "H". Thus, a "L" is presented to the I/O bus through the Bit line.