CHAPTER 4

FULL CUSTOM MOS CIRCUIT AND LAYOUT DESIGN

4.1   Full Custom IC Design Flow

Complex electronic circuits made of discrete components have many interconnections, and each is a potential source of trouble. Failure of electronic equipment is usually due to a poor connection. In an integrated circuit, connections between the components are made internally during the fabrication process, and the number of external connections is thereby minimized. This is certainly a major accomplishment of the integrated circuit.   Along with the greatly increased reliability, other additional advantages that are of immense importance include :

(a)   uniqueness :   final product is unique, so potential competitors cannot readily copy the design as compared to when using standard components.

(b)   performance : performance of the product can be improved above that achievable with standard parts.

(c)   innovation :   product designer may have greater freedom to innovate, if necessary, and not being constrained by standard parts.

(d)   miniaturization : final product size can be reduced considerably as many functions can be incorporated within a single chip.

(e)   low power :   power consumption is greatly reduced.

(f)   cost :   reduction in final product cost due to saving in component cost and board size reduction.

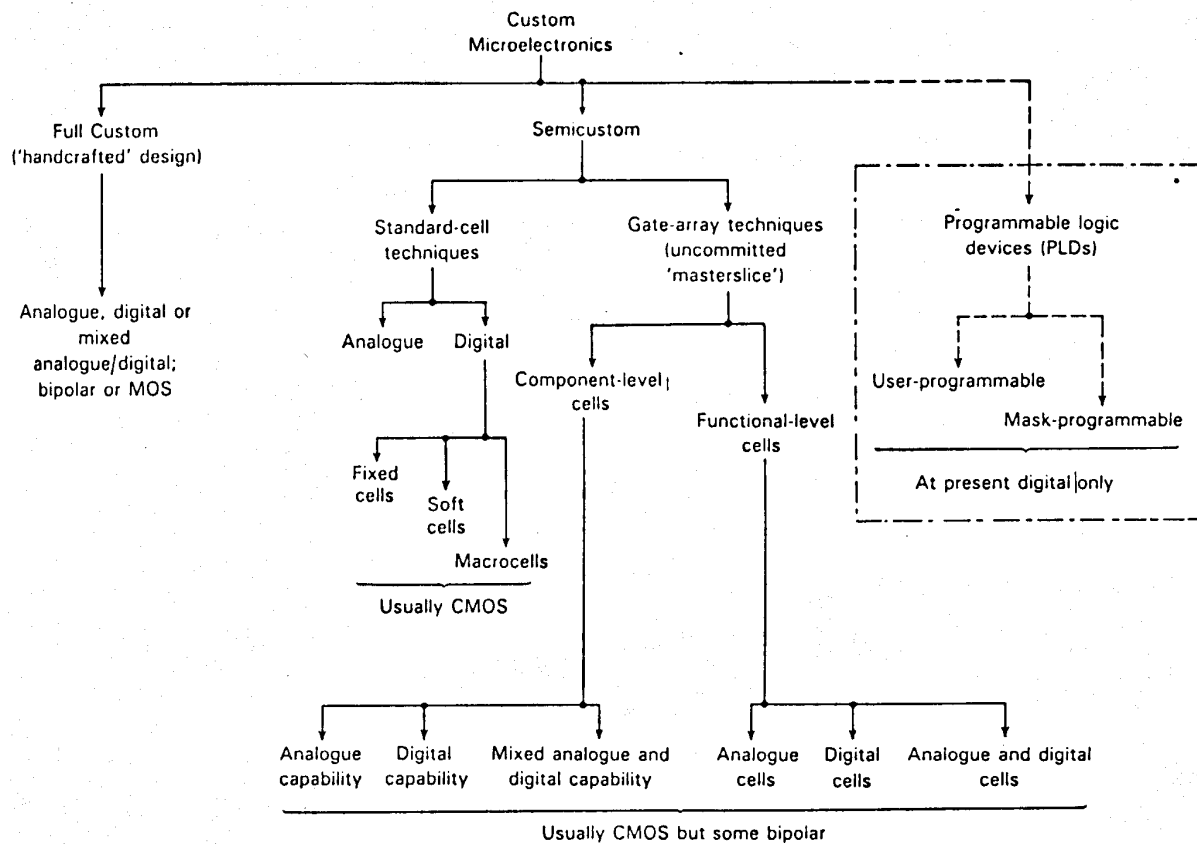## 4.1.1 Hierarchy of Custom Microelectronics ICs

Figure 4-1   Classification of Custom Microelectronics

An integrated circuit can be built using different approach depending on the amount of investment one is willing to commit. In the case of Semi-Custom approach, two major methods, the standard cells and gate array methods are available. These approaches rely on some form of pre-existing design such as standard cell-library and gate arrays prefabricated on wafers (Chapter 5) to come up with an integrated circuit.

A low cost approach is the Programmable Logic Devices (PLDs). For this approach, the required function is programmed onto the PLD IC, which can be purchased off the shell based on design requirements. This in turn reduces the time required for product completion.

On the high end, one may choose to use the Full Custom Design approach, which is highest in cost and longest in time in terms of product completion. However, it gives all the advantages mentioned previously.

4.1.2 Full Custom IC Design

When using Full Custom IC design approach, many things have to start from scratch. During the process, designers will use various configurations of transistors/gates, (complex gate, switch, dynamic gate, etc) resistors, capacitors, etc to implement the required IC specifications. Simulations are required to determine the correct logical and timing requirements of the design. The gates/transistors, etc are non-standard parts and their sizes are determined by simulation.

Mask design, which translates the schematic to geometrical data for fabrication, are also part of the process. The complete set of mask consists of designs from transistor level upwards to gate and then to block/functional level.

This approach emphasizes on getting the best possible circuit/functional performance and the smallest silicon area required to implement a circuit. Minimum silicon area implies lower cost per chip but means longer design time and efforts are needed.

4.1.3 General Design Guidelines For Full Custom Design

In order to complete an IC chip design using full custom approach, a set of general guideline needs to be followed. They are :-

(a)   define the IC requirements/specifications.

(b)   identify the various subsystems (e.g. shift register, amplifier, counter, ADC, etc) needed to form the required architecture.

(c)   ensure that there is minimum interdependence between the subsystems and determine the interconnection between them.

(d)   identify the gates/leaf cells needed within the subsystem (e.g. counter needs D-Flip Flops, NAND gate, etc).

(e)   simulate the subsystem to verify the function and decide the transistor sizes of the leaf cells/gate.

(f)   draw stick diagram (representation of mask layout design) for each leaf cell required.

(g)   convert the stick diagram of each leaf cell to mask design (MOS layers) in a CAD environment and interconnect the necessary leaf cells mask layout to form the functional block.

(h)   interconnect the mask design of various functional blocks to form the entire chip.

4.2   MOS LAYERS

There are 3 main layers used in mask layout design, namely the diffusion layer, the polysilicon layer and the metal layer.

Each of these layers is isolated from one another by either thick or thin silicon oxide. It is important to note that whenever a *polysilicon layer (gate) crosses a diffusion layer* (source and drain), *a transistor is formed*. Hence, to avoid any unwanted transistors from being formed, care should be taken to change one of these layers whenever they come together.

No device (transistor, resistor, capacitor, etc) is formed when metal crosses either a diffusion or a polysilicon layer. Layers are interconnected using contact layers.

Layer	R	C	Comments
Metal	Low	Low	Good current capability without large voltage drop. Used for power connections and long interconnections between cells.
Polysilicon	High	Moderate	High IR drop but moderately capacitive. Not suitable for long interconnection. May be used for within cells connections.
Diffusion	Moderate	High	Moderate IR drop. Used mainly to form devices but not for interconnections.

Table 4-2   MOS Layer Characteristics

4.3   STICK DIAGRAM AND DESIGN STYLES

4.3.1 Stick Diagram

Stick diagram is used as the intermediate step when translating schematic circuit to geometrical data so that orientation of the layout (e.g. input/output pins, power line, transistors, etc) can be organized before actual layout design in carried out in the CAD environment.

It uses lines or different colours to represent different mask layout layers. The orientation of a stick diagram must faithfully reflect the actual mask design.

Layer	Colour	Stick Encoding
n-diffusion	Yellow outline/Black dashed line, Brown within	
p-diffusion	Dark Brown outline, Brown within	
Polysilicon	Green	
Metal 1	Blue	
Metal 2	Red	
Implant	Yellow dotted line	
Contact - Connect Poly to Metal 1 - Connect Diffusion to Metal 1	Black Solid circle	
Via - Connect 2 metals	Black	
*N-well / P-well boundary	Brown dotted line	
*Well tie / Substrate tie	Black Cross	V_{dd} / V_{ss}

* only applicable to CMOS process

Table 4-3   Stick Diagram Encoding Table

4.3.2 Design Styles

When translating the schematic design into its stick diagram form, it is desirable to follow a set of design style.

4.3.2.1 CMOS Design Style

To draw stick diagram using CMOS design style, the following steps are recommended.

(a)   Use Metal 1 (blue), draw the V_{dd} and V_{ss} rails in parallel. Usually V_{dd} is drawn on top of V_{ss}.

(b)   Add well ties and substrate ties (represented by a cross on the supply lines).

(c)   Draw the demarcation line between the supply rails to mark the boundary between the well.

(d)   Place all PMOS devices above the demarcation line and all NMOS devices below the demarcation line.

(e)   Interconnect the inputs and outputs to meet pin orientation requirements.
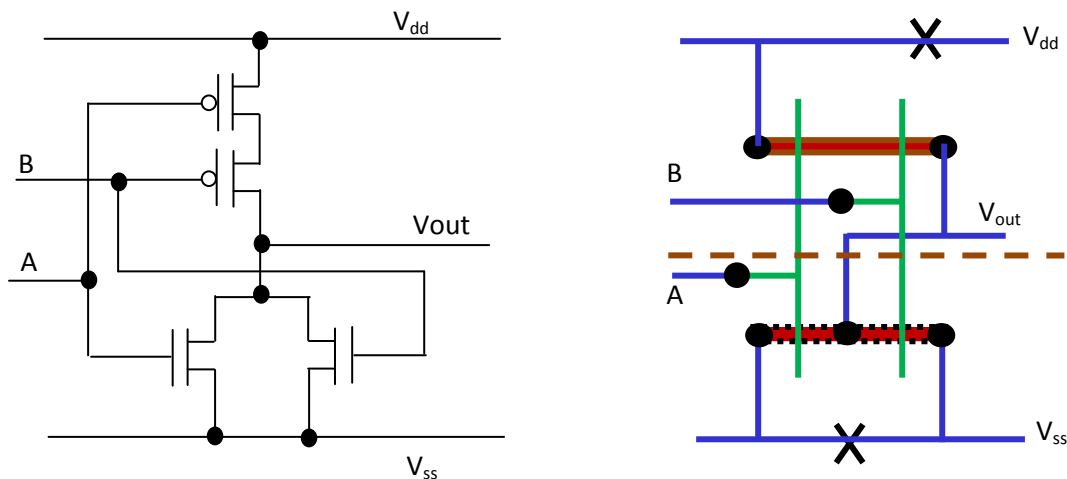   *Note : n-diffusion and p-diffusion lines cannot cross the demarcation line.*

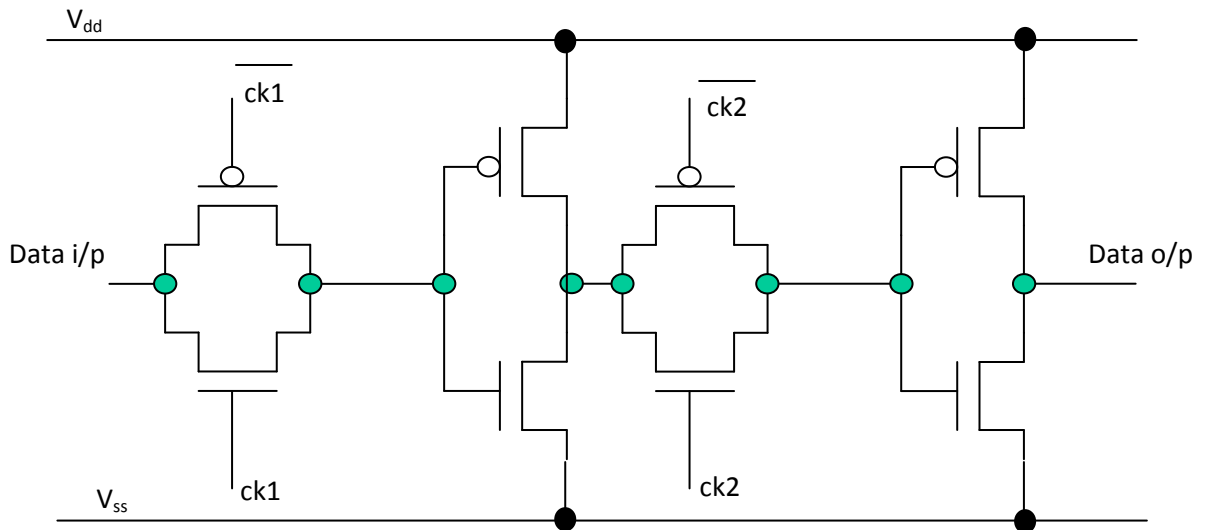Figure 4-4   CMOS NOR Gate Stick Diagram

Figure 4-5 Schematic Diagram of 1-bit Leaf Cell of Shift Register

To draw the stick diagram of the 1-bit Leaf Cell of Shift Register shown in Figure 4-5,

(a)   Using Metal 1 (blue), draw the V_{dd} and V_{ss} rails in parallel.

(b)   Add well ties and substrate ties.

(c)   Draw the demarcation line between the supply rails to mark the boundary between the well.

(d)   Place all PMOS devices above the demarcation line and all NMOS devices below the demarcation line.

(e)   make the necessary interconnections using Metal or Polysilicon layer to interconnect PMOS and NMOS across the demarcation line.
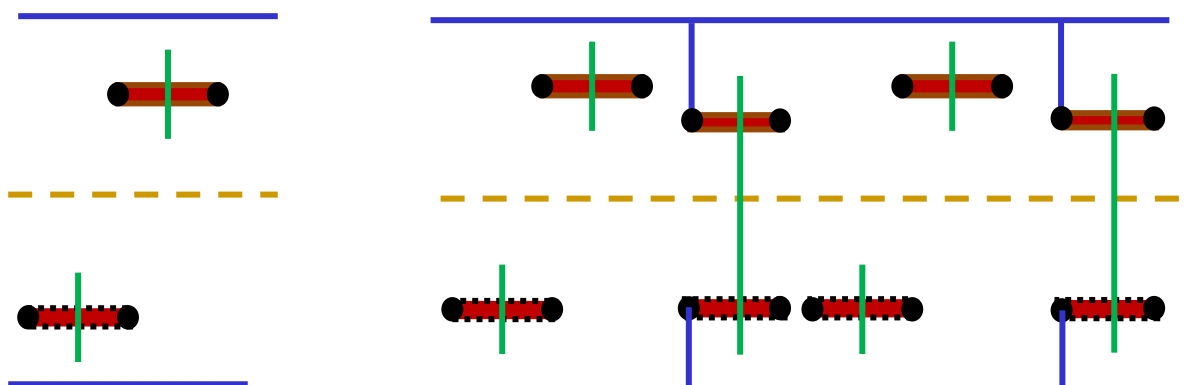
Place PMOS above demarcation line
And NMOS below demarcation line

Arrange the needed transistors with contact points

Figure 4-6   Partial CMOS Stick Diagram of 1 bit leaf cell of a Shift Register
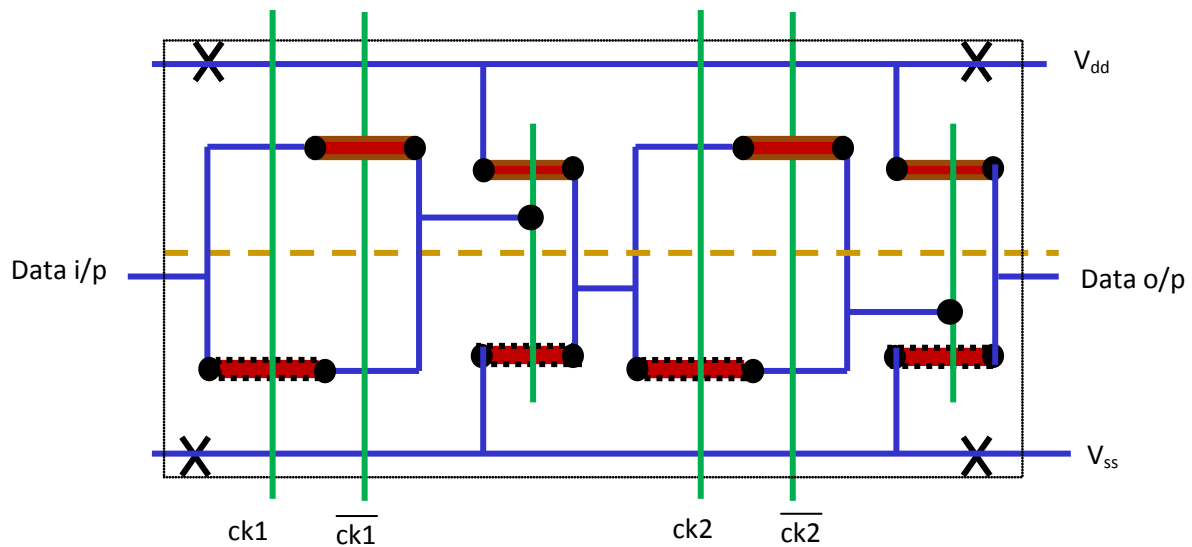
Figure 4-7   CMOS Stick Diagram of 1 bit leaf cell of a Shift Register

4.3.2.3 Mask Layout Encoding (Monochrome)

Table 4-8 gives the monochrome mask layout encoding scheme. It is an equivalent to Table 4-3.

LAYERS	MASK LAYOUT ENCODING MONOCHROME	CIF LAYER
n-diffusion (n+ active)		ND
Polysilicon		NP
Metal 1		NM
Contact cut		NC
Overglass		NG
Implant		NI
Buried contact		NB
p-diffusion (p+ active)	p+ mask	CAA or CPA
p+ mask		CPP
Metal 2		CMS
VIA		CVA
p-well		CPW
V_{DD} or V_{SS} CONTACT	V_{DD} V_{SS}	CC

FEATURE	FEATURE (MASK) (MONOCHROME)
n-type enhancement transistor	(L:W = 1:1) S D G
n-type depletion transistor	(L:W = 1:1)
p-type enhancement transistor	S D p+ mask G

Table 4-8   Feature/Layout Encoding Schemes (Monochrome)

It is possible to derive a circuit schematic from layout geometry using Feature/Layout Encoding Schemes to "reverse engineered" the design. That is, obtain the stick diagram from the layout geometry and translate the stick diagram to schematic/circuit.
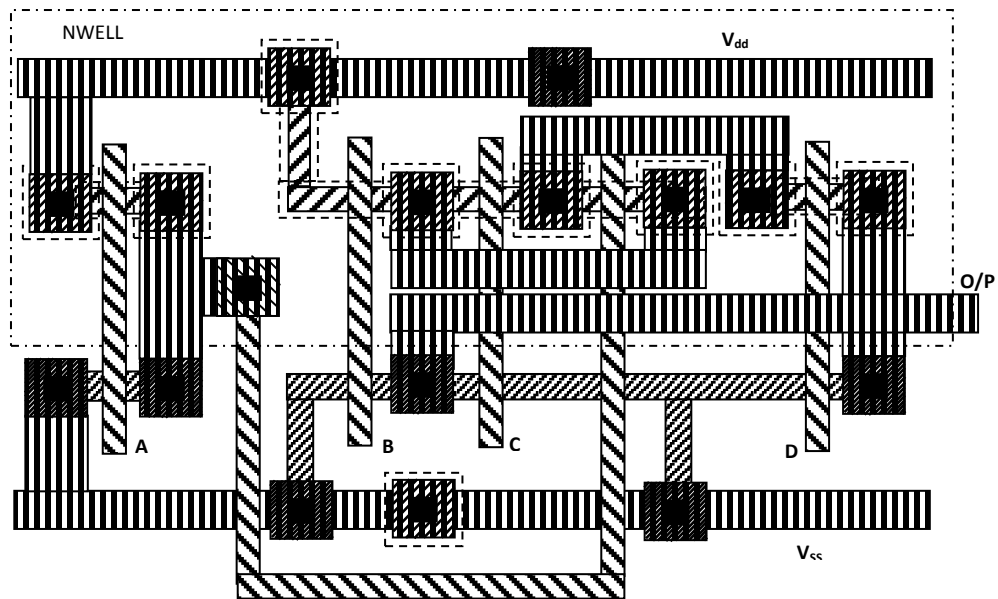

Figure 4-9   Mask Layout Design of CMOS Circuit (N-well process)
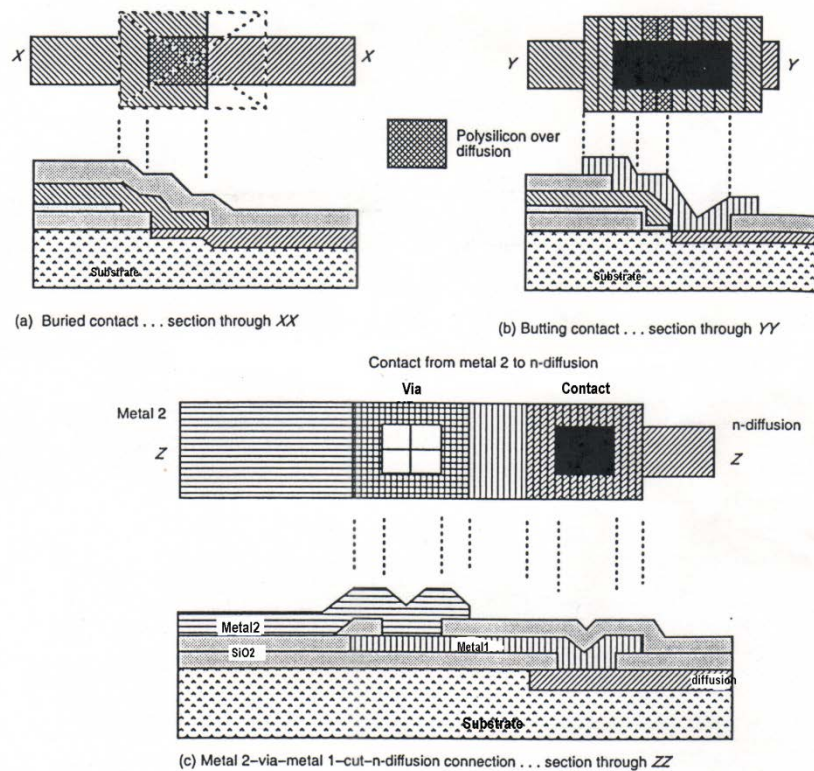

Figure 4-10   Cross-Sectional Structure of Connection Between Layers

4.4   DESIGN RULES AND LAYOUT

Design rules specify the minimum width, separation and overlaps of different layers. These rules are used to translate stick diagrams into mask geometries. It serves as the main communication link between circuit/systems designers and the process engineers engaged in manufacturing.

Lambda (λ) based design rules are based on a single parameter, λ, whose quantity is the maximum deviation of a feature from its intended position when its mask geometry is transferred to the silicon surface. It can also be viewed as the maximum tolerance in fabrication alignment for a particular process.

With λ rules, all paths in all layers are dimensioned in λ units and subsequently λ is allocated an appropriate value compatible with the feature size of the fabrication process. This concept means that the actual mask layout design takes little account of the value subsequently allocated to the feature size.   Mask layout drawn according to the λ rule are subsequently scaled in accordance to the target process technologies (e.g.   For 0.18μm process, λ=0.09μm).   However, scaling of certain layers or features is not always a linear process.

4.4.1 Design Rules Background

4.4.1.1 Well Rules

The implant for forming the N-well or P-well is usually much deeper as compared to the implant for forming the source and drain of a transistor. Hence, it is necessary to provide sufficient clearance between the N-well edges and the adjacent n+ diffusion. Similarly, sufficient clearance is required between the N-well edges and the p+ diffusion it enclosed.   The N-well resistance can be several kΩ per square, it is necessary to thoroughly ground the well. This will prevent excessive voltage drops due to well currents.

4.4.1.2 Transistor Rules

It is essential for the polysilicon to completely cross the diffusion region, otherwise the insufficient gate extension may cause the source and drain to be short-circuited if misalignment occurs during mask transfer. On the other hand, insufficient source-drain extension may cause width of the transistor to be greatly reduced or completely eliminated.
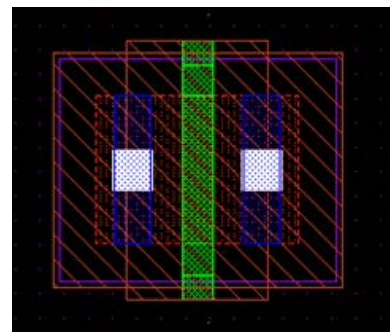

Figure 4-11   Poly extension of Diffusion

4.4.1.3 Contact Rules

Overlapping rules apply when interconnecting two layers including well-ties, substrate ties and butting contacts. Buried contacts are only supported by certain process technology.

Multiple contacts are normally found in the source and drain regions. This is to provide multiple current paths so as to avoid damage due to electro-migration. Having multiple contacts also reduces the overall contact resistance.
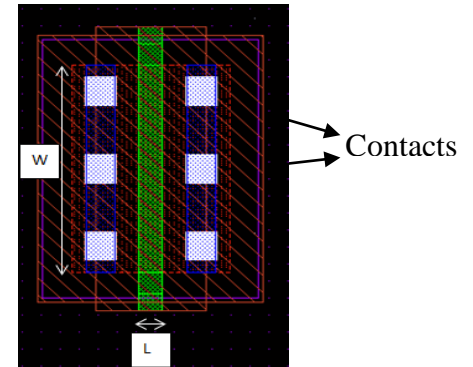

Figure 4-12   Multiple contacts in source & drain regions of transistor

4.4.1.4 Via Rules

Via may not be stacked over or sit on the boundary of polysilicon or diffusion regions as there is a variations in vertical topology at these regions.

4.5   FLOOR PLANNING

Floor planning is the process of arranging various functional blocks within a chip to minimize silicon area, maximize speed, and/or improve the overall performance.

When doing floor planning, it is always advisable to isolate sensitive analogue blocks from noisy digital functional blocks. To maximize operating speed, reduce the length of interconnections between the blocks. Always connect V_{dd} and V_{ss} power lines to the various functional blocks. Connect interconnects between blocks and from blocks to the pads.

V_{dd} pads, V_{ss} pads as well as input/output pads are usually arranged around the peripheral of the chip as defined by the specifications of the package used. The mask layout of these pads is generally available from the target process library. Modifications to these pads are usually not allowed because they are designed with protection against ESD effects
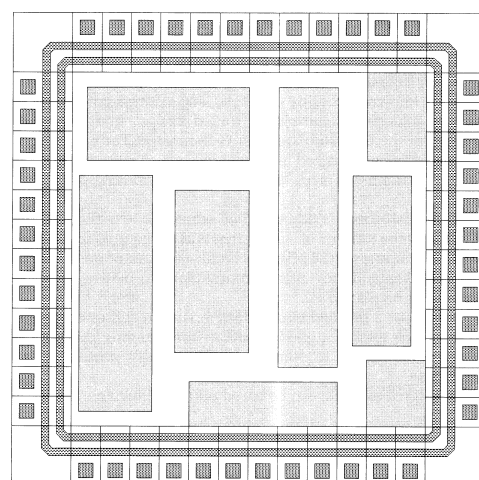

Figure 4-13   Sample Floor Plan

4.6   DESIGN VERIFICATION

The objective of design verification is to ensure that the design meets the required specifications and fabrication design rules before the masks are submitted to the factory for mass production.

Extensive CAD tools are used to perform design verification. Tools used includes :-

(i)   Simulator

The simulator helps ensure that the circuits designed perform the intended functions. It also checks that the circuit meets the timing/speed or frequency response requirements. Examples of such simulators are ModelSim, Verilog and Analog Environment.

(ii)   Design Rule Checker (DRC)

This tool verifies that the mask layout designed meets the design rules specified by the target process technology.

(iii)   Layout Versus Schematic Check (LVS)

The LVS verify that the mask layout design is the same as the intended schematic in terms of devices (transistors type, resistor, etc), size of the transistors, value of the resistors, etc as well as the interconnects. It also helps locate unconnected, partly connected or extra devices. Part of LVS check also includes the function of Electrical Rules Check.

(iv)   Electrical Rules Check (ERC)

ERC verify power connections and check for minimum conductor width for current specifications. It also locates floating nodes (gate of transistors), short circuits and as well as disabled transistors.
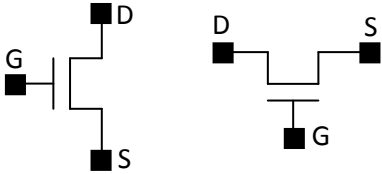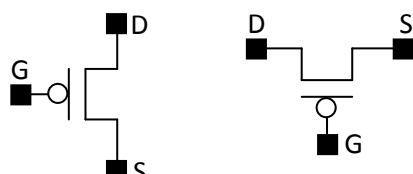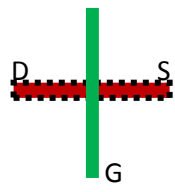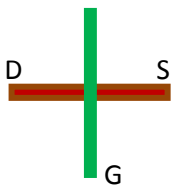
(v)   Layout Parasitic Extractor (LPE)
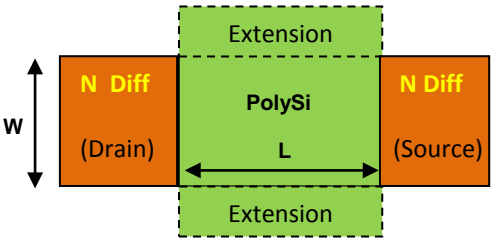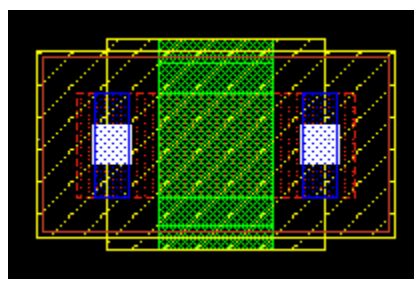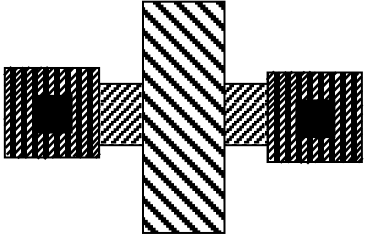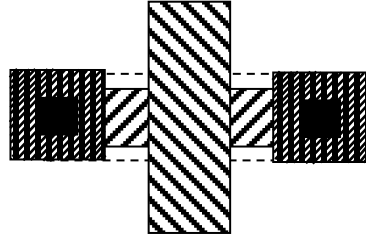
LPE extracts the parasitic resistance and capacitance value based on the completed mask layout design. This is done through calculating the resistance and capacitance values based on the geometry drawn.

(vi)   Post-Layout Simulation (BackAnnotation)

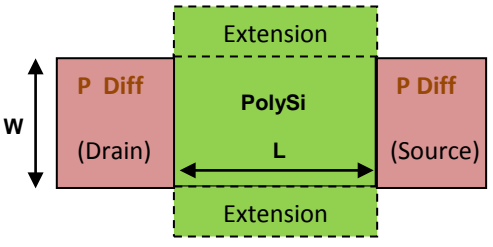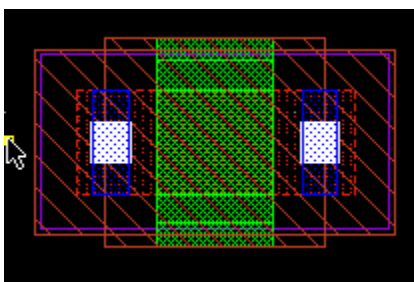Post-layout simulation gives a more accurate performance index because the extracted parasitic resistances and capacitances values are feedback into the simulator environment (values are added to the respective nodes in the circuit) and timing check is done to ensure that it still meets the specifications.

Chapter 4 – Summary

(I)   Transistor Representation

NMOS	PMOS
(a) Symbol	**(a) Symbol**
(NMOS symbol diagram: D, G, S and D, S, G)	*(PMOS symbol diagram: D, G, S and D, S, G)*
(b) Stick Diagram	**(b) Stick Diagram**
(NMOS stick diagram: D, S, G)	*(PMOS stick diagram: D, S, G)*
(c) Layout (Colour)	**(c) Layout (Colour)**
N Diff (Drain), PolySi, N Diff (Source), Extension, W, L	*P Diff (Drain), PolySi, P Diff (Source), Extension, W, L*
(d) Layout (Monochrome)	**(d) Layout (Monochrome)**

(II)   Circuit Representation - CMOS Inverter

(a) Symbol	(b) Transistor Level Schematic

(c) Stick Diagram	(d) Layout (Colour)

(d)   Layout (Monochrome)
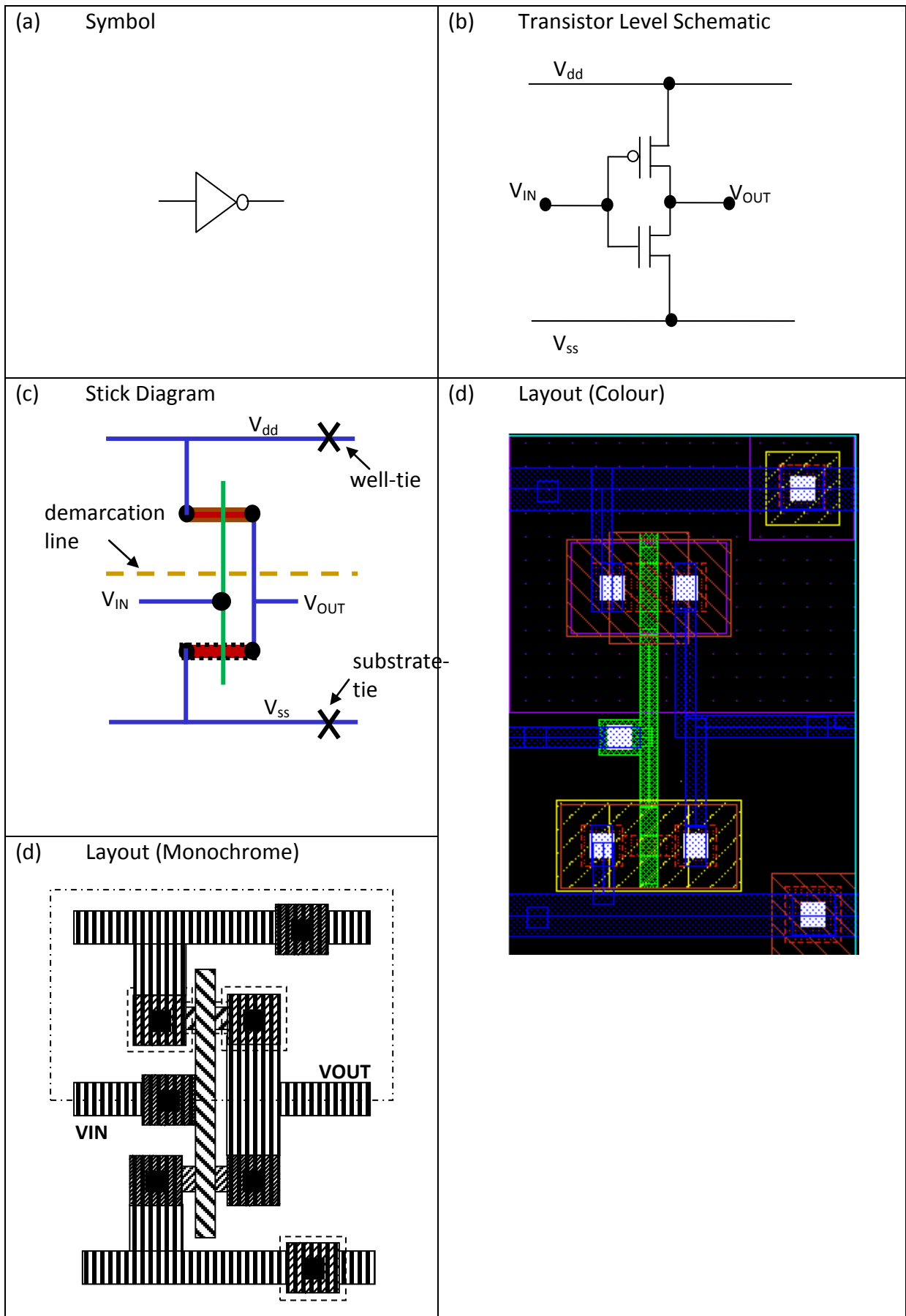
(III)   Layout & Cross-Section View of CMOS Inverter

Stick Diagram

NMOS

| N Diff (Drain) | PolySi L | N Diff (Source) |

Extension

Extension

W

| P Diff (Drain) | PolySi L | P Diff (Source) |

Extension

Extension

Stick Diagram

P MOS
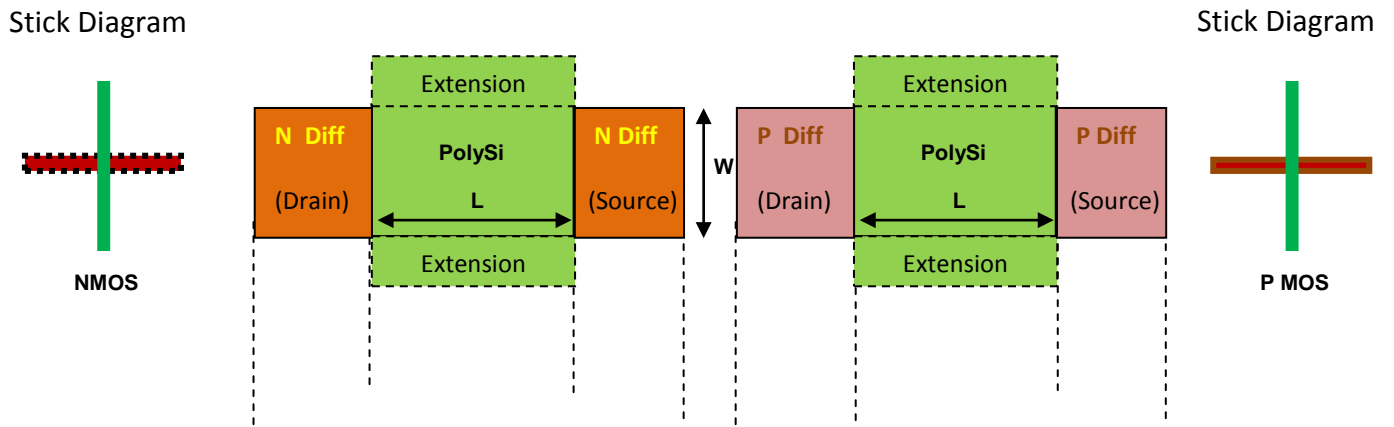
Plan View / Layout View of N-Well CMOS Inverter

Al (Metal)

(Gate)

W

L

p+   n+   p-substrate   n+   p+   n-well   p+   n+

substrate tie   Source   Drain   Drain   Source   n-well tie
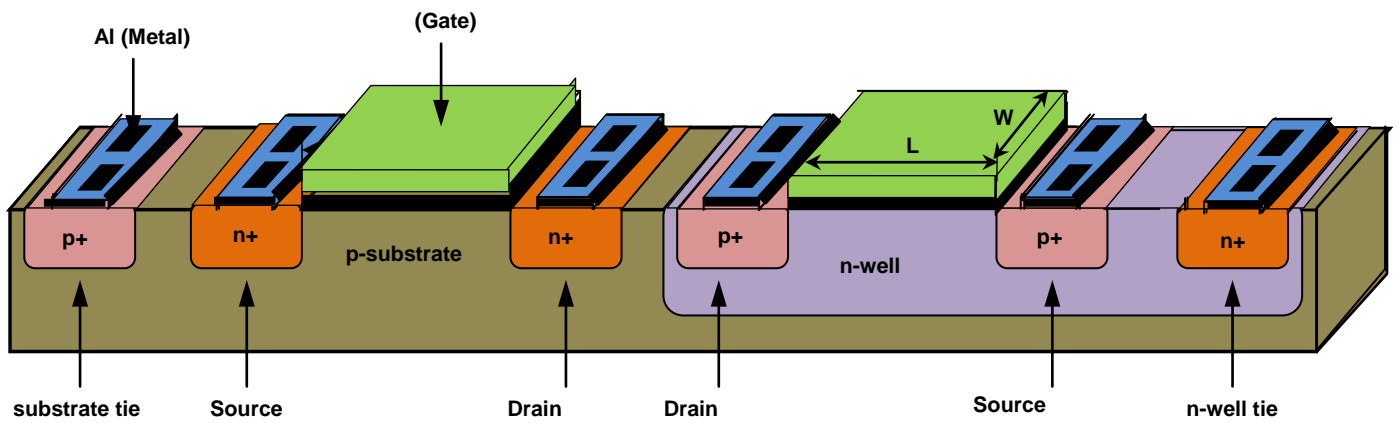
Cross-sectional structure of N-Well CMOS Inverter

Review Questions

Question 1

List the key advantages of using full custom IC design as compared to standard component implementation.

Solution to 1

Along with the greatly increased reliability, other additional features that are of immense importance include :

(a)   uniqueness :   final product is unique, so potential competitors cannot readily copy the design as compared to when using standard components.

(b)   performance :   performance of the product can be improved above that achievable with standard parts.

(c)   innovation :   product designer may have greater freedom to innovate, if necessary, and not being constrained by standard parts.

(d)   miniaturization : final product size can be reduced considerably as many functions can be incorporated within a single chip.

(e)   low power :   power consumption is greatly reduced.

(f)   cost :   reduction in final product cost due to saving in component cost and board size reduction (based on economy of scale).

Question 2

(a) Name the 3 basic MOS layers and briefly state their characteristics.
(b) State the implication, if any, when a diffusion layer crosses a polysilicon layer.
(c) State the implication, if any, when a polysilicon layer crosses a metal layer.

Solution to Q2

(a) The 3 basic MOS layers are :-

Metal : It has low resistive and capacitive effect. It has good current carrying capability without large voltage drop and is commonly used for power connections and long interconnections between cells.

Polysilicon: It has high resistive but moderate capacitive effect. The combined RC product is moderate but the IR drop is high, hence it is not suitable for long interconnection but may be used for within cells connections.

Diffusion : It has moderate resistive but high capacitive effect. Its IR drop is moderate and is highly capacitive thus greatly affecting timing. Thus, it is used mainly to form devices but not for interconnections.

(b) If a diffusion layer crosses a polysilicon layer, a transistor is formed.

(c) If a polysilicon layer crosses a metal layer, there is no implication as they are on different layer and also no feature is formed.

Question 3

Justify the following design rules :
(a) 2λ poly to poly spacing.
(b)   no spacing required between diffusion and metal layers.
(c) 2λ overhanging of polysilicon at transistor gate.
(d)   substrate and well-ties are required for CMOS technology.

Solution to Q3

(a) 2λ poly to poly spacing is required to avoid short-circuiting between two unrelated tracks.

(b)   No spacing is required between diffusion and metal layers because they are on different layers isolated from each other by layers of oxides.

(c) 2λ overhanging of polysilicon at transistor gate is prevent the source and drain terminals of a transistor from forming a short-circuit.

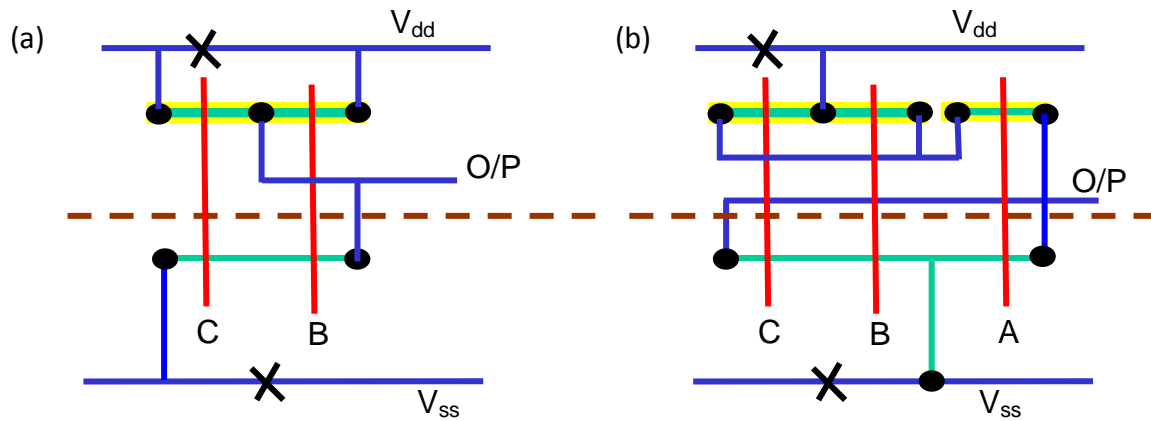(d)   substrate and well-ties are required for CMOS technology to minimize the chance of latch-up.

Question 4

Draw the stick diagram, based on CMOS technology, of the following functions:-

(a)   two-input NAND gate

(b) $Z = \overline{A + BC}$

Solution to Q4

Question 5

For the layout shown in Figure 4-12,
(a)   draw the corresponding colour-coded stick diagram.
(b)   draw the transistor level schematic.
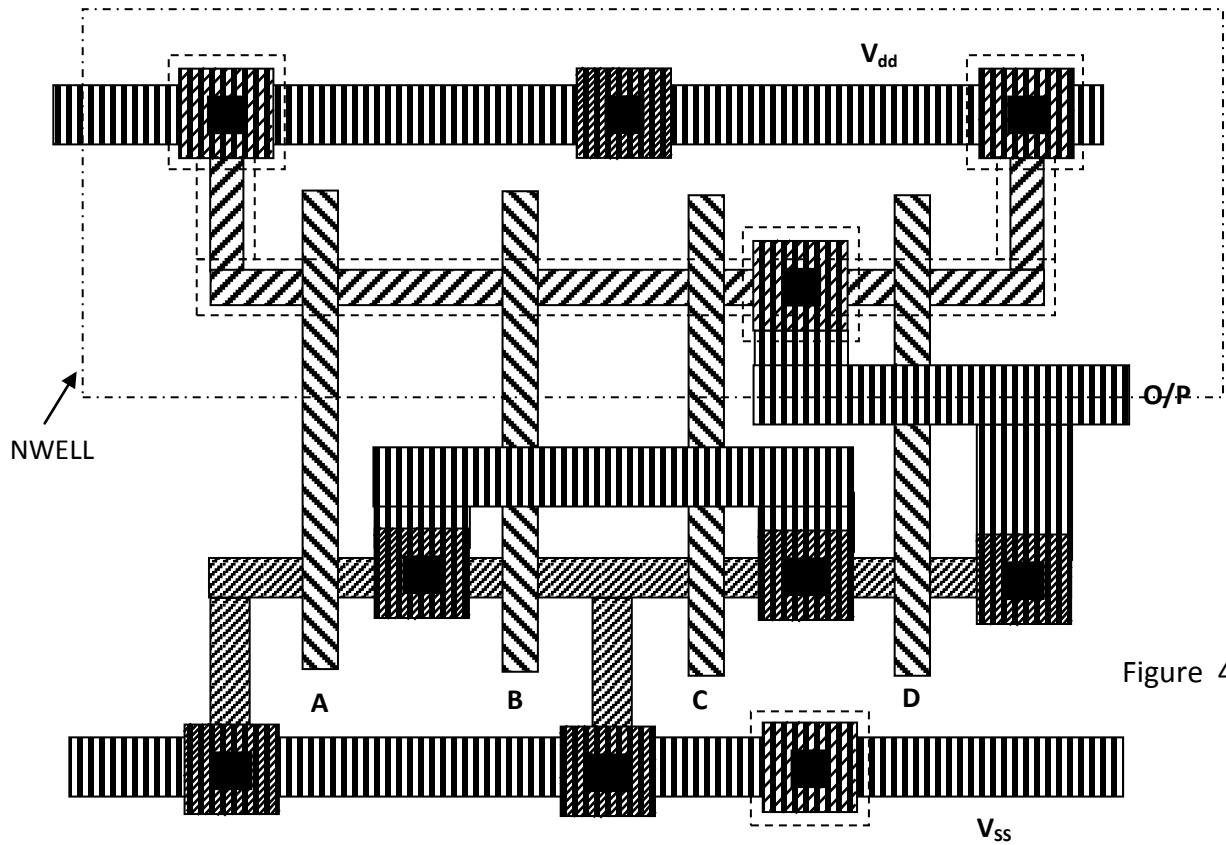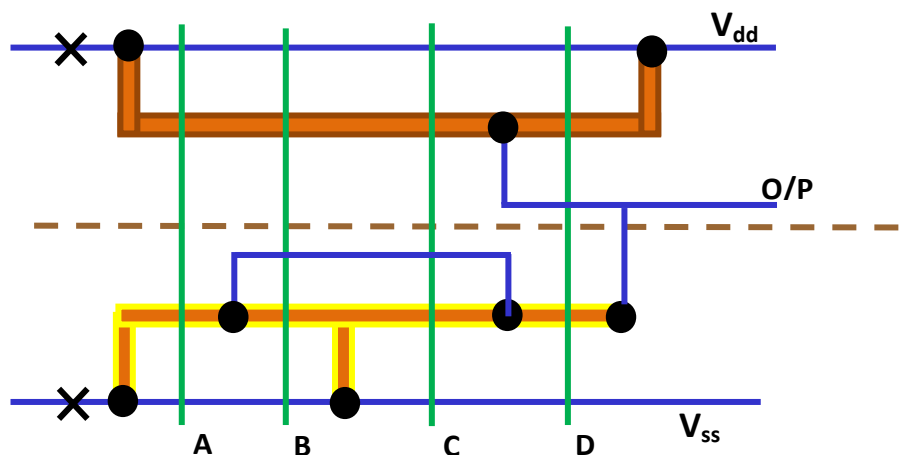(c)   state the boolean expression.
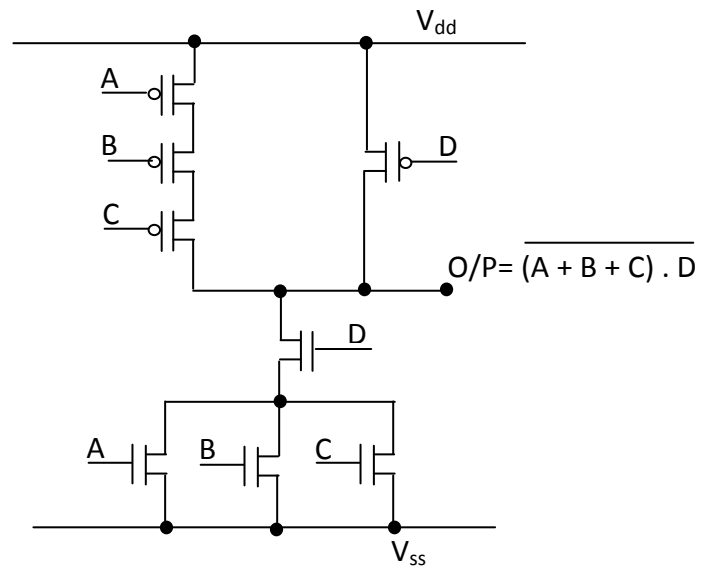

NWELL

Figure 4-12

Solution to Q5

(a)   Stick Diagram

(b)   Transistor level schematic

$$O/P = \overline{(A + B + C) \cdot D}$$

(c) $O/P = \overline{(A + B + C) \cdot D}$

Question 6

From the mask layout shown in Figure 4-13,
(a)   Draw the corresponding colour-coded stick.
(b)   Draw the corresponding transistor level schematic and state the boolean expression for *O/P*.
(c)   Name and state the purpose of Part (I) and Part (II) as indicated on the layout.
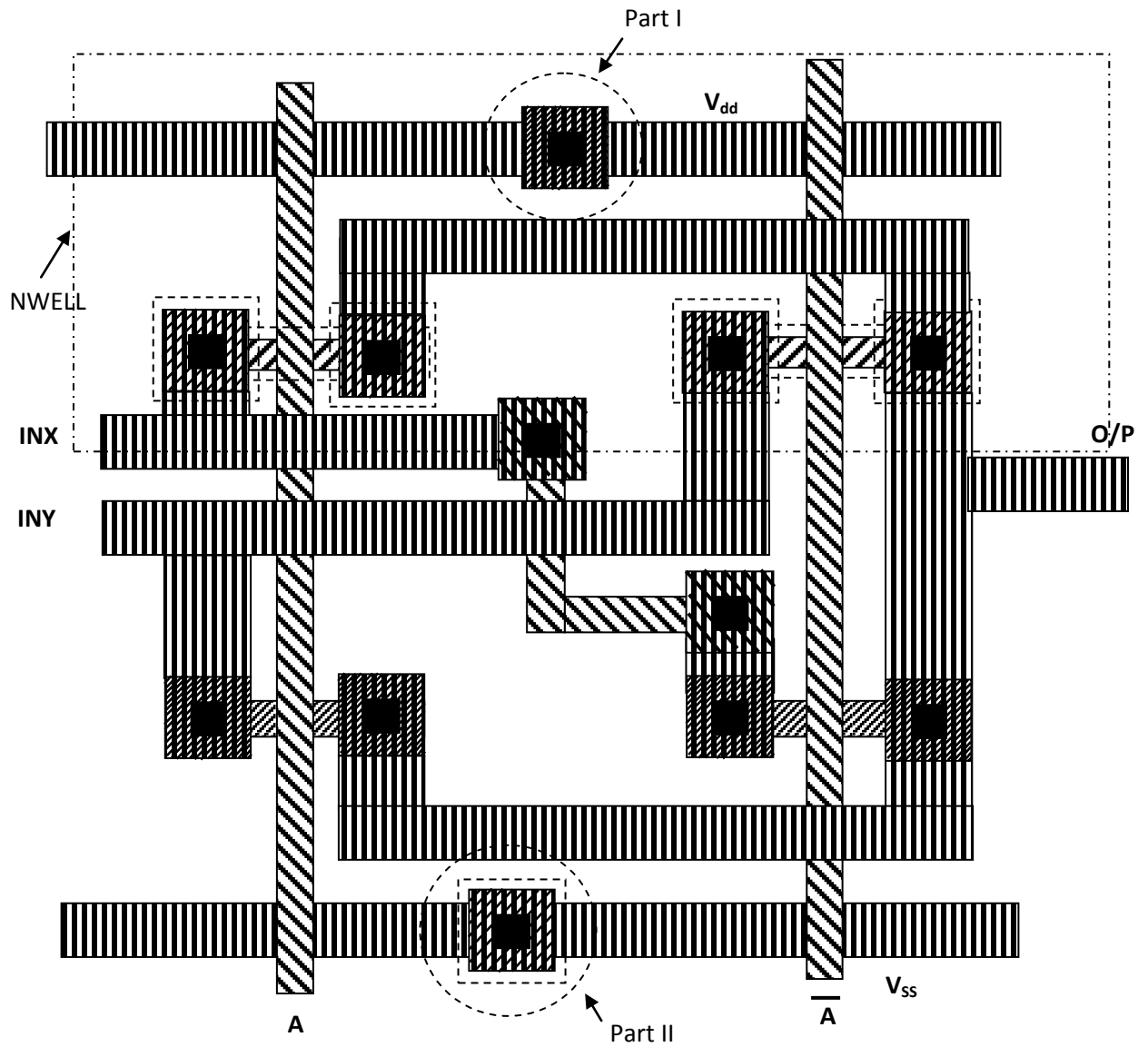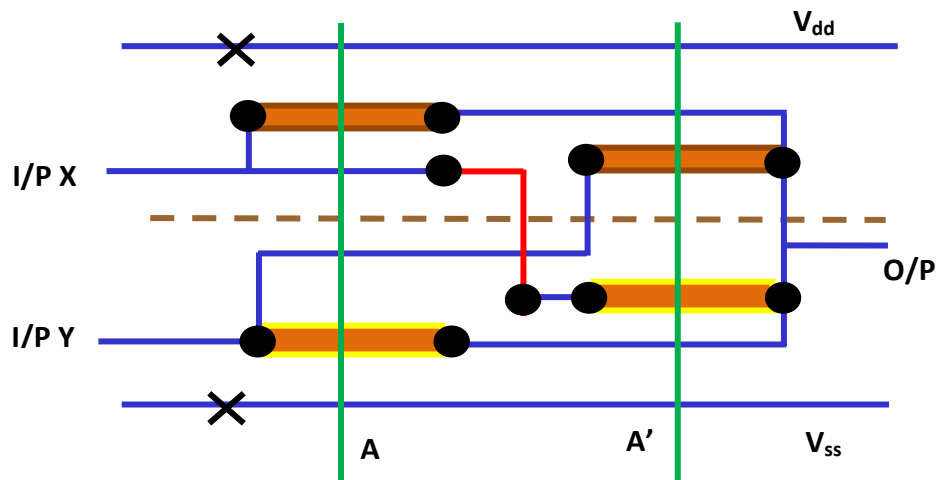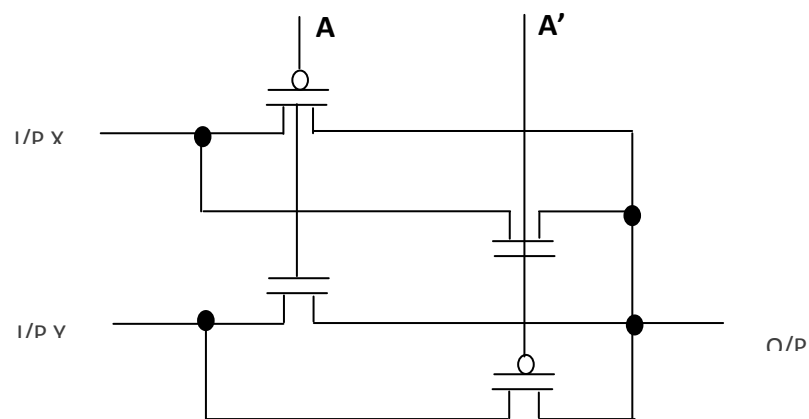(d)   State and briefly explain the choice of diffusion type for Part (I).

Figure 4-13

Solution to Q6

(a)   Stick Diagram

(a)   Transistor Level Schematic

$$O/P = \overline{A}\ INX\ +\ A\ INY$$

(c)   Part (I) is a well-tie and Part (II) is a substrate-tie.
These are necessary to reduce possible latch-up effect in CMOS circuits.

(d)   N-type diffusion is used to form Part(I). This is the choice as it is meant as a contact to connect the n-well to the supply, V_{dd}.

Question 7

Explain briefly the need for the followings CAD tools used in Integrated Circuit design.
(a)   Logic Simulation
(b)   Design Rule Check
(c)   Layout versus Schematic Check
(d)   Post Layout Simulation, also known as Back-Annotation

Solution to Q7

(a)   <u>Logic Simulation</u>
        The simulator helps ensure that the circuits designed perform the intended functions. It also checks that the circuit meets the timing/speed or frequency response requirements. Examples of such simulators are Quicksim, Verilog and Analog Artist.

(b)   <u>Design Rule Check (DRC)</u>
        This tool verifies that the mask layout designed meets the design rules specified by the target process technology.

(c)   <u>Layout Versus Schematic Check (LVS)</u>
        The LVS verify that the mask layout design is the same as the intended schematic in terms of devices (transistors type, resistor, etc), size of the transistors, value of the resistors, etc as well as the interconnects. It also helps locate unconnected, partly connected or extra devices. Part of LVS check also includes the function of Electrical Rules Check.

(d)   <u>Post-Layout Simulation</u>
        Post-layout simulation gives a more accurate performance index because the extracted parasitic resistances and capacitances values are feedback into the simulator environment (values are added to the respective nodes in the circuit) and timing check is done to ensure that it still meets the specifications.