CHAPTER 2

INTEGRATED CIRCUIT DESIGN OVERVIEW

2.1 Review of Semiconductor Physics
2.2 Comparison of IC and Discrete Components
2.3 IC Classification and Evolution

REVIEW OF SEMICONDUCTOR PHYSICS

2.1.1 Atom

An atom is made up of a central nucleus (protons + neutrons) with electrons revolving around its orbit.

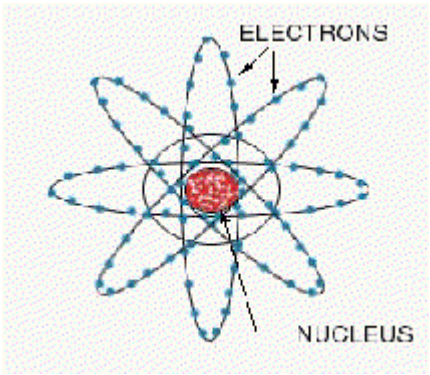


Figure 2-1 Atomic Structure

2.1.2 Atomic Bonding

Atoms may be bonded in different manner thus giving rise to different property. There are basically three types of bonding methods, namely,

(i) Metallic bonding

The valence electrons can be detached easily from the atom, giving rise to large number of free electrons; hence, solid with this bonding structure behaves like conductors.

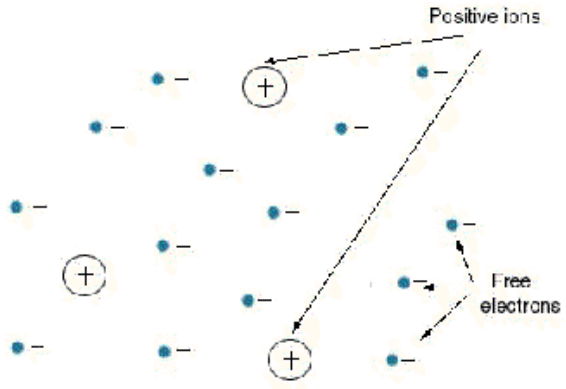


Figure 2-2 Metallic Bonds

(ii) Covalent bonding

Each atom is surrounded by four nearest neighbours, and the valence electrons on the outer-shell are shared to form a stable structure. This structure gives rise to semiconductor.

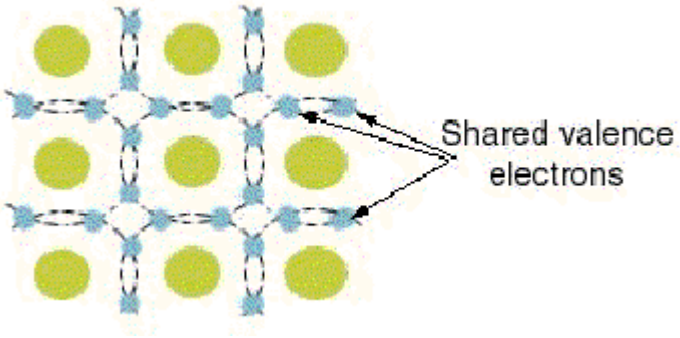


Figure 2-3 Covalent Bonds

(iii) Ionic bonding

Valence electrons are strongly attached to their atoms, they cannot break off easily, and thus material with this type of bonding behaves like an insulator.

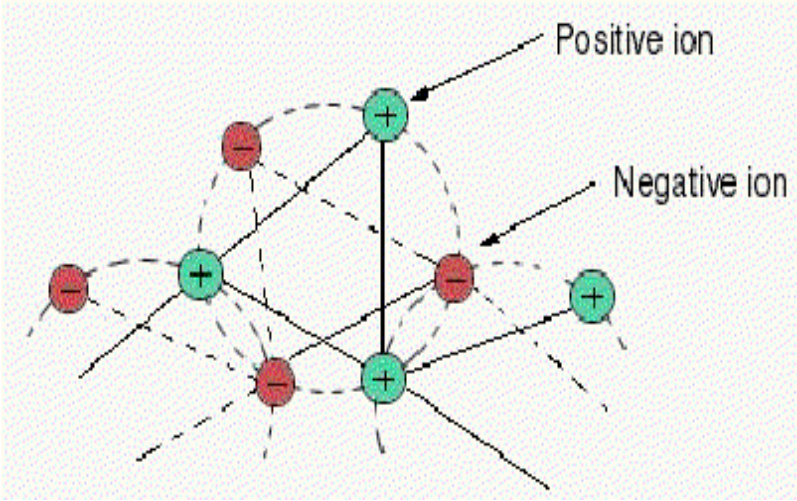


Figure 2-4 Ionic Bonds

2.1.3 Physics of Semiconductor

Semiconductors are a group of materials having electrical conductivities intermediate between metals and insulators. The conductivity of these materials can be varied over orders of magnitude by changes in temperature, optical excitation, and/or impurity content.

Silicon (Si) is a very popular semiconductor used for the fabrication of majority of the rectifiers, transistors and integrated circuits and is the material of interest in this course.

2.1.3.1 Intrinsic Semiconductor

Intrinsic semiconductor is a perfect semiconductor crystal with no impurities or lattice defects. Since there are no free electrons to help in conduction, it behaves like an insulator at very low temperature (0°K or -273°C).

At room temperature, some electrons gain sufficient energy to break away from its parent atom. With these free electrons, the material is now capable of conducting electricity to a certain extend.

This thermal breaking of covalent bonds creates vacancies called holes. Hence, the holes and free electrons are equal in numbers, this is also known as an electron-hole pair generation. The reverse process also occurs; that is, recombination of hole and free electron takes place when a free electron moves into a vacancy in a covalent bond.

The electrons and holes concentration generated under this condition are denoted as n_o and p_o respectively and $n_o = p_o$. As these are intrinsic carriers, they are also commonly referred to as n_i where $n_i = p_o = n_o$.

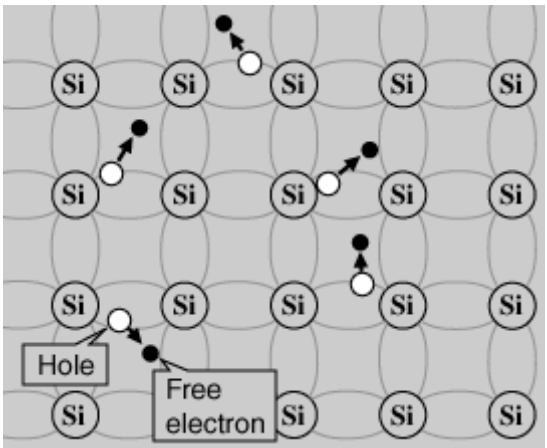


Figure 2-5 Intrinsic Semiconductor (Si)

2.1.3.2 Extrinsic Semiconductor

These are semiconductors doped with certain degree of impurities such that the equilibrium carrier concentrations n_o and p_o are different from n_i. There are two major type of extrinsic semiconductor, namely n-type and p-type.

(i) n-type semiconductor

An N-type semiconductor has donor impurities, N_d. These are elements with FIVE valence electrons per atom, such as phosphorus (P), arsenic (As), antimony (Sb). Each donor fits into the crystal structure, replacing a silicon atom, but there is one electron remaining after the covalent bonds are filled. At room temperature, it acquires enough thermal energy to break away and become free electron. The donor atom left behind is now ionized with a positive charge. Type V (5) dopants have electrons as majority carriers and holes as minority carriers.

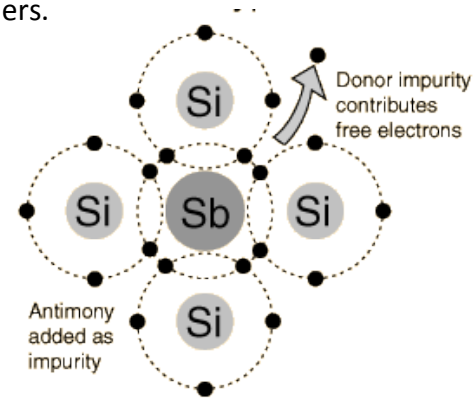


Figure 2-6 N-type Semiconductor (Si)

(ii) p-type semiconductor

A P-type semiconductor has acceptor impurities, N_a. These are elements with THREE valence electrons per atom, such as, boron (B), indium (In), gallium (Ga) and aluminum (Al). Each acceptor has one valence electron less than required to complete the covalent bonds. At operating temperature, electrons from covalent bonds fill the vacancies of the acceptors, and the acceptors are ionized and have a negative charge. Type III (3) dopants have holes as majority carriers and electrons as minority carriers.

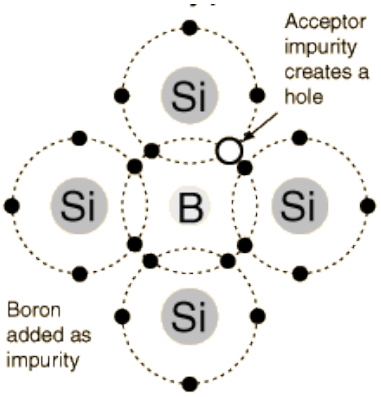


Figure 2-7 P-type Semiconductor (Si)

2.1.4 The pn Junction

pn junction exists between many integrated-circuit elements and its underlying substrate. It constitutes voltage-dependent parasitic capacitance which in turn determines the breakdown voltage and output resistance of the active devices.

There are many techniques to form a pn junction. Different techniques result in different characteristics. Two common techniques used are :-

(i) *step* pn junction
- uniform p and n doping on each side of a junction.

(ii) *graded* pn junction
- the p and n side has concentration which varies with distance on either side of the junction.

2.1.4.1 Step pn Junction

Step pn junction may be visualized as separate regions of p- and n- semiconductor being brought together to form the junction. Upon joining the two regions, diffusion of carriers take place because of the large carrier concentration gradients at the junction.

When a p-n junction is formed, some of the free electrons in the n-region diffuse across the junction and combine with holes to form negative ions (N_a^-). In so doing they leave behind positive ions (N_d^+) at the donor impurity sites. These charges cause an electric field **E** to be established and it opposes the diffusion current. The electric field will build up to a point where the net current is zero. This point is also known as the equilibrium point.

Source : http://hyperphysics.phy-astr.gsu.edu/hbasees/Solids/pnjun.html#c1

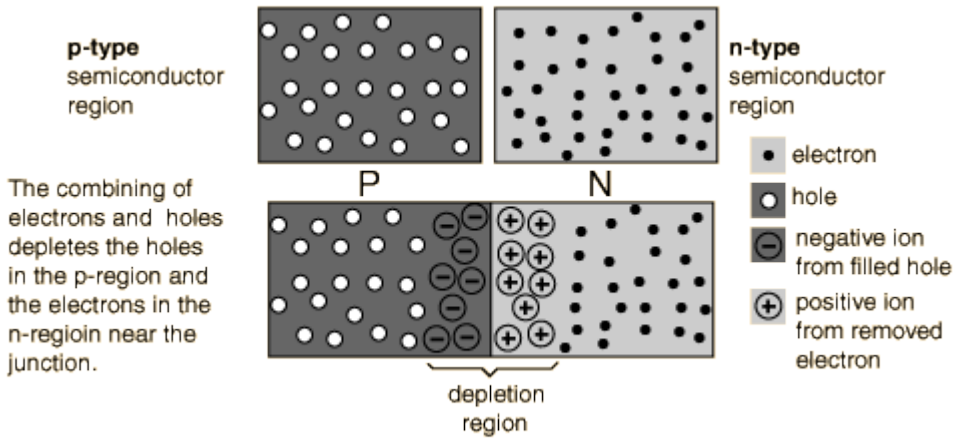
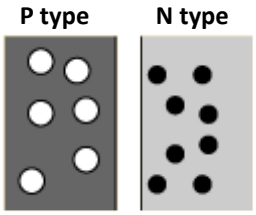


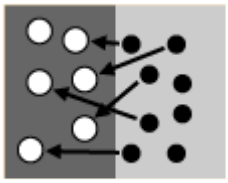
Figure 2-8 Step PN Junction

2.1.4.2 PN Junction Details

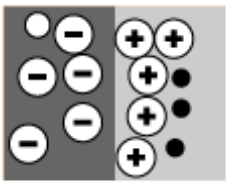
When p-type and n-type materials are placed in contact with each other, electrons diffuse across to combine with holes, creating a "depletion region".



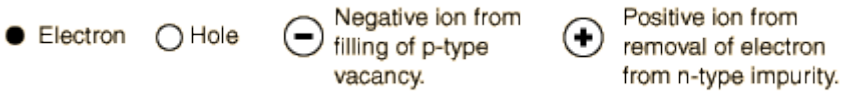
In the p-type region there are holes from the acceptor impurities and in the n-type region there are extra electrons.



When a p-n junction is formed, some of the electrons from the n-region which have reached the conduction band are free to diffuse across the junction and combine with holes.



Electron **filling a hole** in an atom on the p-side makes it a **negative ion**.
Electron **leaving** an atom leaves behind **a positive ion** on the n-side.
A space charge builds up, creating a depletion region which inhibits any further electron transfer.



The equilibrium potential difference, V_o, across the region is given by :-

$$V_o = V_n - V_p$$

or

$$V_o = V_T \ln (N_a N_d / n_i^2)$$

where

V_o = electrostatic potential or built up potential (at equilibrium)

V_n = potential in the neutral n material

V_p = potential in the neutral p material

V_T = (kT)/q which is approximately = 26mV at 300 K for silicon

n_i = intrinsic carrier concentration = 1.5 x 10^{10} cm^{-3} at 300 K for silicon

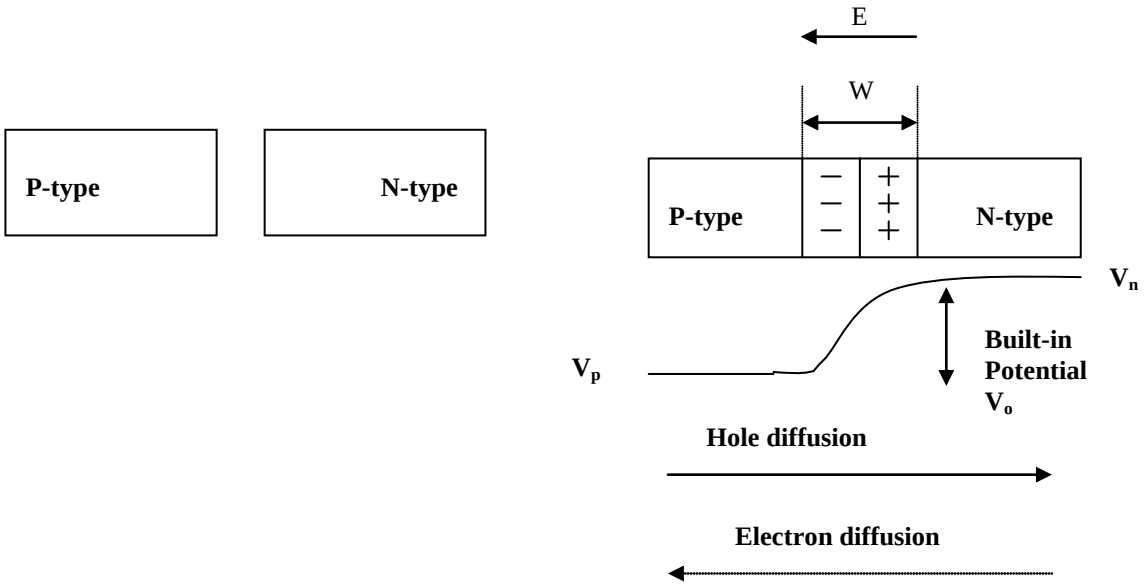


Figure 2-9 Step pn Junction

The region, W, is called the depletion region/transition region (depleted of carriers). The width of this depletion region is a function of doping concentration.

$$W = [\frac{2\varepsilon_o \varepsilon_r V_o}{q} (\frac{N_a + N_d}{N_a N_d})]^{½} \qquad m$$

where

q = electron unit charge = 1.6x10^{-19} C

$\varepsilon = \varepsilon_o \varepsilon_r$ = permittivity of free space * relative permittivity of material (Si)

= 8.85x10^{-14} x 11.8 F/cm

2.1.4.3 Biasing of pn Junction

(i) Equilibrium

When no external voltage is applied to a pn junction, it is said to be at equilibrium. In addition, there is no current flowing across the junction.

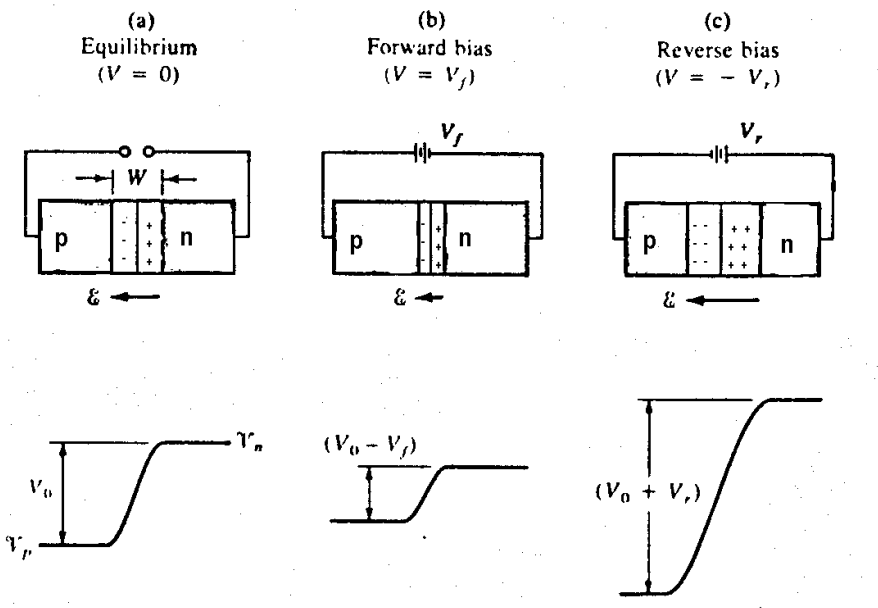


Figure 2-10 P-N under voltage bias

(ii) Forward Bias (V > 0)

With an applied voltage of V > 0V, the electrical field across the depletion is reduced to (V_o-V). Therefore, when $V \geq V_o$, current starts to flow across the junction because the bias voltage has overcame the built-in potential.

(iii) Reverse Bias (V < 0)

The electrostatic potential barrier at the junction is widen to (V_o+V), this practically prevents the diffusion current flow. Under reverse biased condition, the electric field across the depletion region is increased and so is the width of the depletion region.

2.1.4.4 Integrated Circuit Implementation of P-N junction

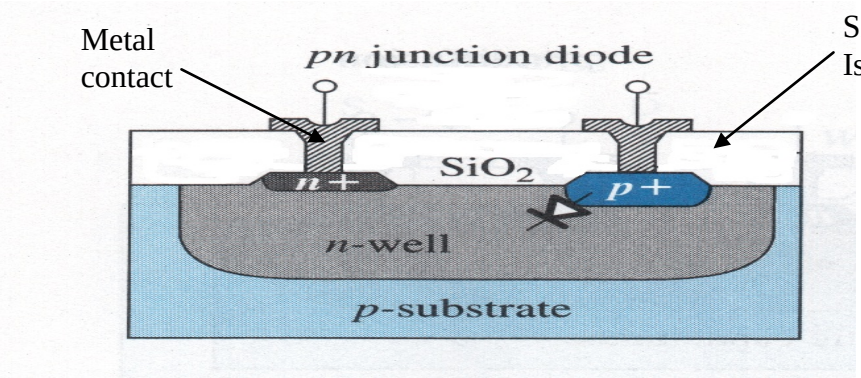


Figure 2-11 Cross-sectional structure of PN junction in Si Wafer

p-substrate

Si wafer doped with type III impurities; it provides mechanical support/bulk for the device

n-well

Si doped with type V impurities (n-type semiconductor); it serves as the cathode (-ve terminal of the diode)

n+ region

Si doped heavily with type V impurities; it provides the contact region for the n-well to other devices

p+ region

Si doped heavily with type III impurities (p-type semiconductor); it provides the anode of the diode (+ve terminal) and serves as contact region to other devices

2.2 COMPARISON OF IC AND DISCRETE COMPONENTS

Advantages of ICs over discrete components :-

(i) higher reliability - no solder joints, wires, plugs, etc.

(ii) low power consumption - parasitic greatly reduced.

(iii) higher speed - shorter paths and lower parasitic capacitance.

(iv) smaller physical size and weight reduction hence smaller number of subsystems needed.

(v) lower cost due to high production volume thus enabling automation.

2.3 IC CLASSIFICATION AND EVOLUTION

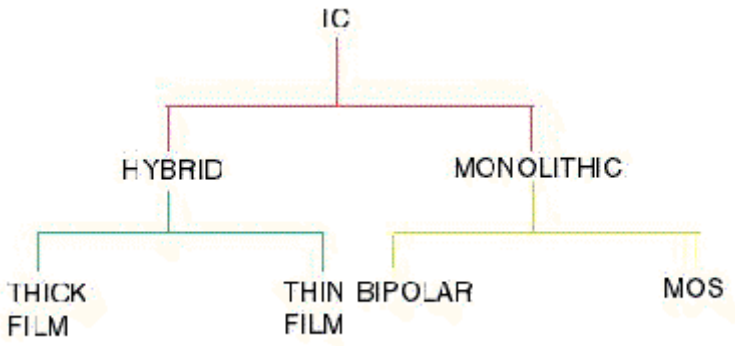


Figure 2-12 IC Classification by Processing Technology

2.3.1 Hybrid Technology

This technology place devices and circuits of different technologies on a common substrate and interconnecting them to perform useful functions

It can be subdivided into two fabrication technologies, namely :-

(i) Thin Film
This fabrication technology gives rise to circuits with precision resistor tolerance, reliable high frequency operation and long term stability.

(ii) Thick Film
This fabrication technology gives rise to circuits with greater current carrying capacity, higher reliability in severe environment and requires lower capital investment in terms of design and production cost.

2.3.2 Monolithic technology

It is also known as planar technology where all components are placed on a single semiconductor substrate.

It can be subdivided into two fabrication technologies, namely :-

(i) Bipolar Technology
Current movement involves both the majority and minority carriers.

(ii) MOS Technology
Current movement involves only the majority carriers.

2.3.3 IC Evolution

1823 - Si was discovered
1948 - Transistor was invented
1959 - Planar transistor (IC) was developed

Year	Level Of Integration	Transistors per chip	Typical Products
1959 – 1961	Discrete Components	1	Transistors, diodes
1961 – 1966	Small Scale Integration (SSI)	2 - 50	Logic gates, Flip Flops
1966 – 1971	Medium Scale Integration (MSI)	50 – 5,000	Counters, Multiplexers, Adders
1971 – 1980	Large Scale Integration (LSI)	5,000 – 100,000	8-bit micro-processors, ROM,RAM
1980 – 1985	Very Large Scale Integration (VLSI)	100,000 – 10,000,000	16 and 32 bit micro-processors
1985 – 1990	Ultra Large Scale Integration (ULSI)	10,000,000 – 1,000,000,000	Special processors, Real time image processing
1990 –	Super Large Scale Integration (SLSI)	>1,000,000,000	Pentium III, System on Chip

Table 2-13 Microelectronics Evolution

Over the years, IC chips sizes has shrunk dramatically, from 50um in the 1960s to 0.18um at the beginning of the new millennium, and there is no stop sign in sight. By reducing the minimum feature size, smaller devices can be made, thus more powerful chip with the same die size.

	1995	1998	2000	2002	2005	2008
Min feature size (um)	0.35	0.25	0.18	0.13	0.10	0.07
DRAM (Bits/Chip)	64M	256M	1G	4G	16G	64G
Microprocessor (Transistors/cm^2)	4M	7M	13M	25M	50M	90M
ASIC (Transistors/cm^2)	2M	4M	7M	13M	25M	40M
Wafer Size (mm)	200	200	200 – 300	300	300	300 – 400

Source : Semiconductor Industry Association (SIA)

Table 2-14 Overall Road Map for Semiconductor Industry

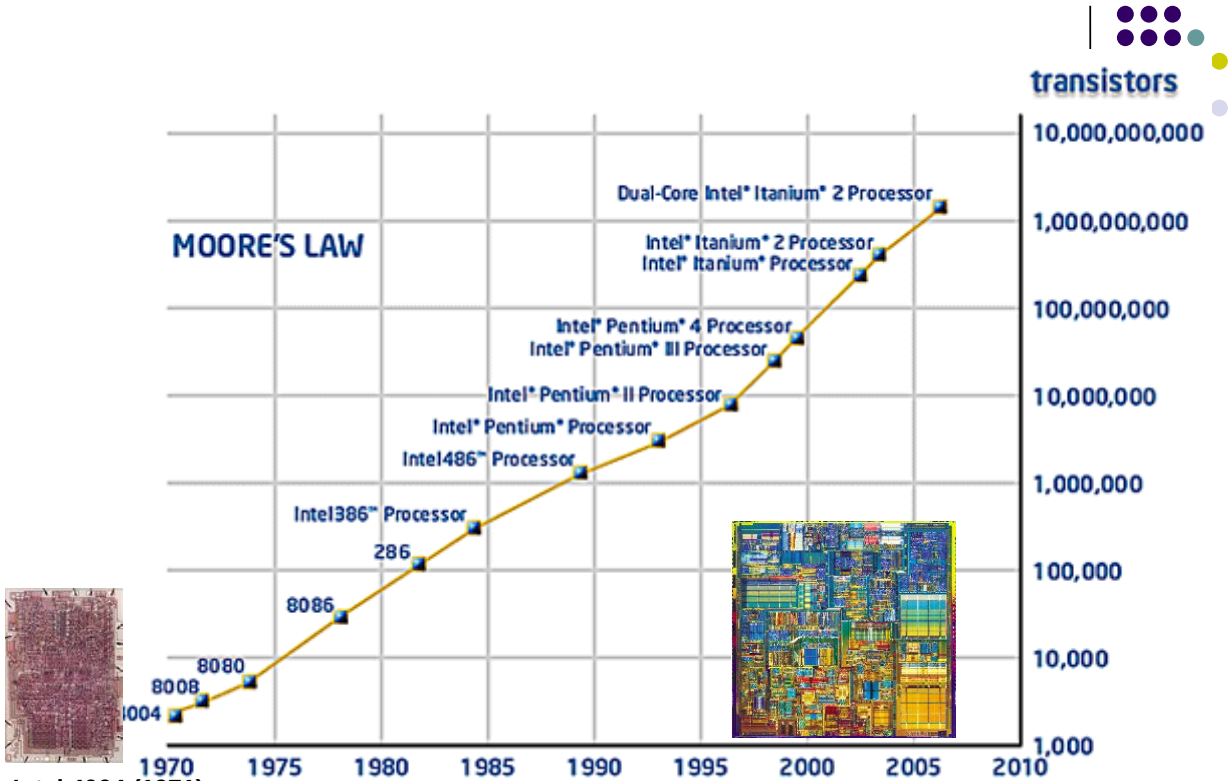


Figure 2-15 Moore's Law

2.3.4 Technology and Speed/Power Performances

Different technology is used to meet different speed and power requirements.

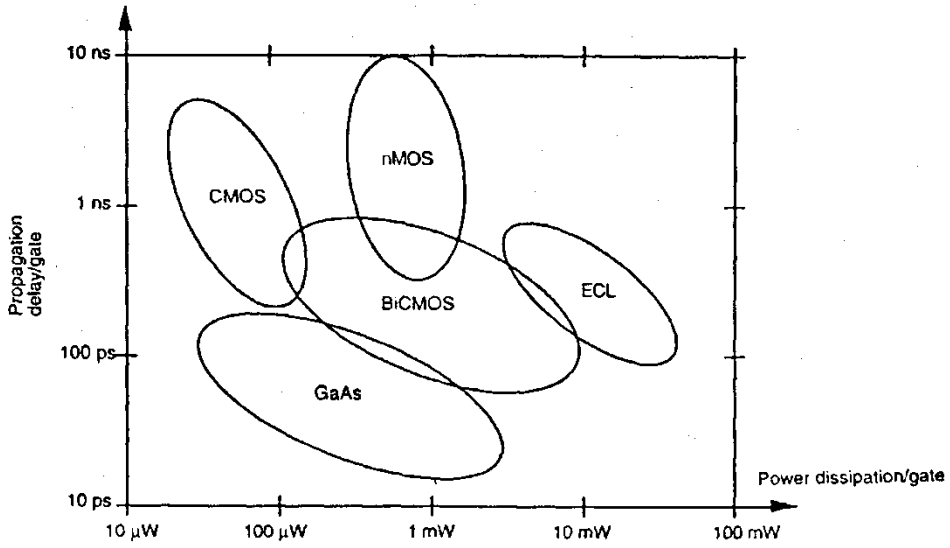


Figure 2-16 Speed/Power Performance of Various Technologies

CMOS is now the dominant technology in IC manufacturing. It employs both PMOS and NMOS transistors to form logic elements. The advantage of CMOS is that its logic elements draw significant current only during the transition from one state to another and very little current between transitions - hence power is conserved. However, it has a known deficiency of limited load driving capabilities (due to limited current sourcing and sinking abilities of PMOS and NMOS transistors. Hence, it is largely used in forming logic circuits.

Bipolar technology, such as ECL, has higher gain, better noise and better high frequency characteristics. It is largely used to form critical high speed parts of a system. However, it requires larger area per transistor and the power dissipation is also higher compared to CMOS.

BiCMOS technology provides an efficient way of speeding up VLSI circuits. It is a combination of Bipolar and CMOS technology. Bipolar transistors are used to form the I/O and driver circuits while the MOS transistors were used to form the logic part of the circuits, thus overcoming the deficiency of limited load driving capabilities of CMOS technology.

Gallium Arsenide (GaAs) is an alternate substrate over Silicon (Si). Due to it being more rare and difficult to obtain than silicon, arsenic being very toxic and GaAs lacks the silicon's ability to use its oxide formed as a mask to protect the silicon, Si remained the dominant material for semiconductors.

Review Questions

Question 1

With respect to intrinsic silicon, briefly explain :-

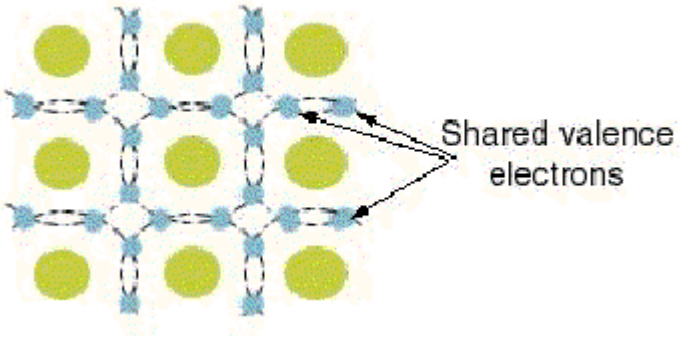
(a) its atomic bonding structure.

(b) its atomic characteristics at room temperature (electron-hole generation).

(c) how n-type and p-type semi-conductor are obtained.

Solution to Q1

(a) Intrinsic silicon is a perfect semiconductor crystal with no impurities or lattice defects. It behaves like an insulator at very low temperature (0°K or -273°C) since there are no free electrons to help in conduction. It is formed by covalent bonding.



Atomic Structure of Intrinsic Silicon

(b) At room temperature, electrons gain sufficient energy to break away from its parent atom. With these free electrons, the material is now capable of conducting electricity to a certain extend.

This thermal breaking of covalent bonds creates vacancies called holes. Hence, the holes and free electrons are equal in numbers, this is also known as an electron-hole pairs generation. The reverse process also occurs; that is, recombination of hole and free electron takes place when a free electron moves into a vacancy in a covalent bond. Whenever an electron breaks free, it leaves behind a hole.

The electrons and holes concentration generated under this condition are denoted as n_o and p_o respectively and $n_o = p_o$. As these are intrinsic carriers, they are also commonly referred to as n_i where $n_i = p_o = n_o$.

(c) n-type semiconductor

An N-type semiconductor has donor impurities, N_d. These are elements with five valence electrons per atom, such as phosphorus (P), arsenic (As), antimony (Sb). Each donor fits into the crystal structure, replacing a silicon atom, but there is one electron remaining after the covalent bonds are filled. At room temperature, it acquires enough thermal energy to break away and become free electron. The donor atom left behind is now ionized with a positive charge.

Type V dopants have electrons as majority carriers and holes as minority carriers.

p-type semiconductor

A P-type semiconductor has acceptor impurities, N_a. These are elements with three valence electrons per atom, such as, boron (B), indium (In), gallium (Ga) and aluminum (Al). Each acceptor has one valence electron less than required to complete the covalent bonds. At operating temperature, electrons from covalent bonds fill the vacancies of the acceptors, and the acceptors are ionized and have a negative charge.

Type III dopants have holes as majority carriers and electrons as minority carriers.

Question 2

(a) Aluminum is added to an n-type silicon sample with concentration $N_d = 10^{16}$ cm^{-3}, to form an abrupt junction. If the acceptor added has a concentration of $N_a = 4 \times 10^{18}$ cm^{-3}, calculate the built-in potential (V_o) and depletion region width (W) for this junction at equilibrium (300K).

Given :

$n_i = 1.5 \times 10^{10}$ cm^{-3}

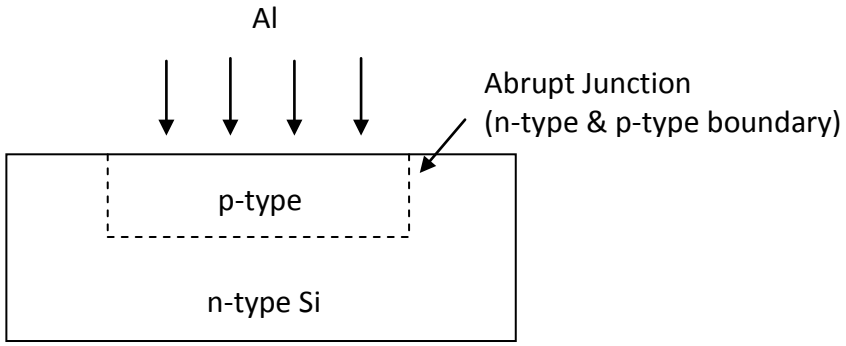
$V_T = 26$ mV

$\varepsilon = \varepsilon_o \varepsilon_r = 8.85 \times 10^{-14} \times 11.8$ F/cm

(b) What is the purpose of the depletion layer in a pn junction ?

Solution to Q2

(a)



(i) Built-In Potential (V_o)

$V_o = V_T \ln (N_a N_d / n_i^2)$

$$= 26x10^{-3} \ln \frac{(4 \times 10^{18})(1 \times 10^{16})}{(1.5 \times 10^{10})^2}$$

= **0.853 V**

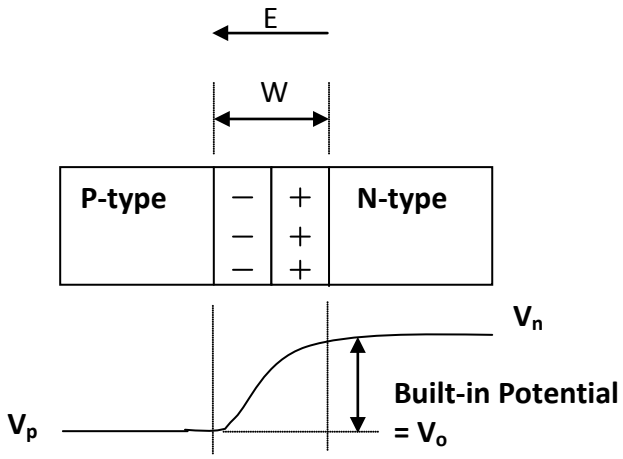
(ii) Depletion Width

$$W = [\frac{2\varepsilon_o \varepsilon_r V_o}{q} (\frac{N_a + N_d}{N_a N_d})]^{½} \quad m$$

$$W = [\frac{2\,(8.85x10^{-14})x11.8\ x\ 0.853}{1.6x10^{-19}} (\frac{4x10^{18} + 1x10^{16}}{(4x10^{18})(1x10^{16})})]^{1/2} \quad m$$

= **3.34×10^{-5} cm**

(b) Depletion region prevents carriers from crossing between the p and n region in the pn junction. It also provides the electric field that constitutes the built-in voltage, V_o.



Question 3

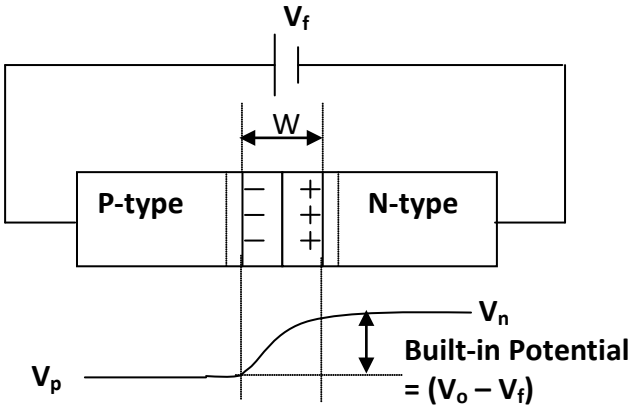
Explain what will happen to depletion region of a pn junction when it is :-

(a) forward biased.

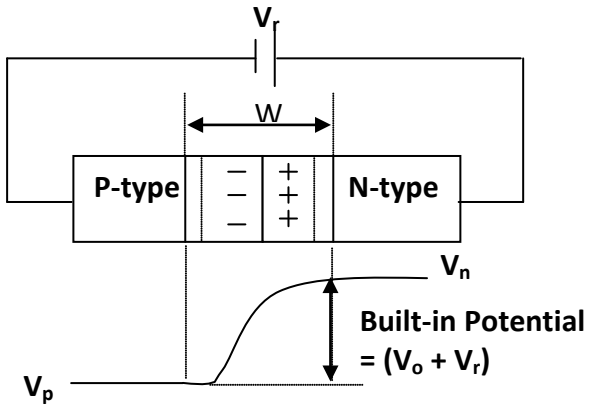
(b) reverse biased.

Solution to Q3

(a) Forward biasing is achieved by applying a '+ve' voltage to the p-side and a '-ve' voltage to the n-side of the pn-junction. This causes the built-in potential to reduce below the V_o at equilibrium and hence the depletion width to decrease. When $V_f \geq V_o$, current flows from the p-side to the n-side.

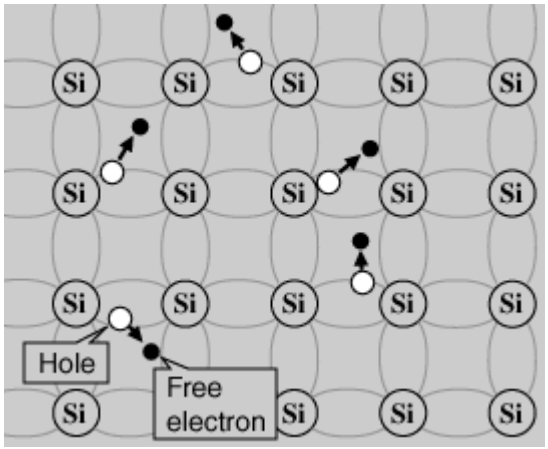
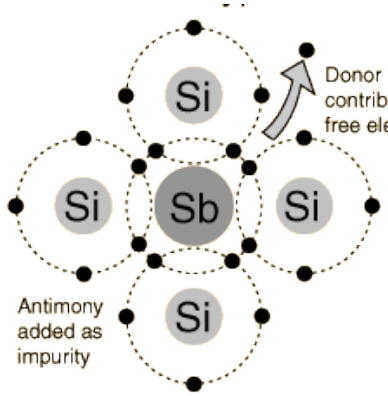
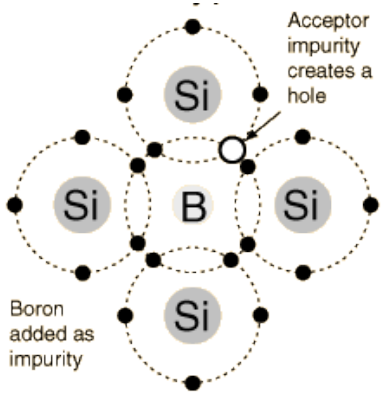


(b) Reverse biasing is achieved by applying a '-ve' voltage to the p-side and a '+ve' voltage to the n-side of the pn-junction. This causes the built-in potential to increase beyond its V_o at equilibrium and hence the depletion width also increases. Current flow cross the junction is prohibited.



Chapter 2 – Summary

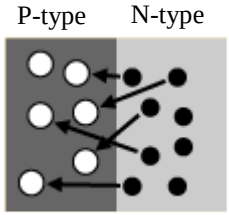
2.1.3 Physics of Semiconductor

Pg 4 **Intrinsic**	Pg 5 **N-Type**	Pg 6 **P-Type**
		
Pure silicon atoms	Silicon atoms + type-V dopants eg phosphorus (P), arsenic (As), antimony (Sb)	Silicon atoms + type-III dopants eg boron (B), indium (In) and aluminum (Al)
	Each donor replaces a silicon atom	Each acceptor replaces a silicon atom
At room temperature, $n_i = p_o = n_o$	At room temperature, the extra electrons break free resulting in excess electrons (majority carriers)	At room temperature, there are excess holes (majority carriers). Electrons from other covalent bonds move in to fill the vacancies.
Poor Conductor	Conductor	Conductor

2.1.4 The pn Junction in NMOS

Pg 7

PN Junction



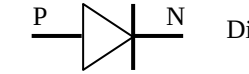
● Electron ○ Hole

⊖ Negative ion from filling of p-type vacancy.

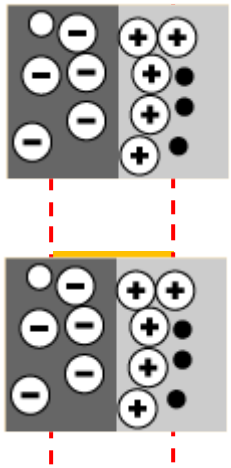
⊕ Positive ion from removal of electron from n-type impurity.

Electron **filling a hole** in an atom on the p-side makes it a **negative ion**.

Electron **leaving** an atom leaves behind **a positive ion** on the n-side.



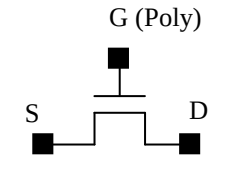
Diode

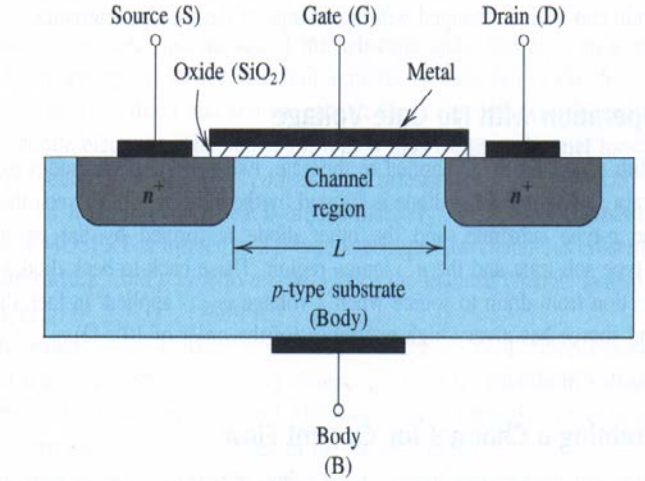


A space charge builds up, creating a depletion region (insulation) which inhibits any further electron transfer.

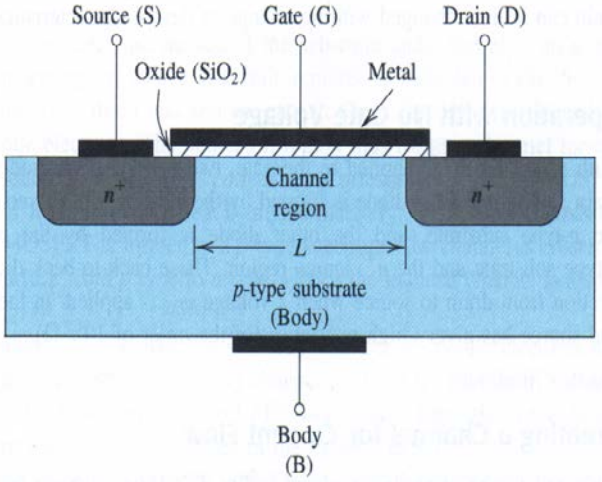
N and P regions are isolated from each other (open circuit). No further flow of carriers can take place

PN Junction in N-Transistor





N and P region are isolated from each other by the depletion region. Hence, the source and drain can be built on the same substrate without literally being short-circuited.

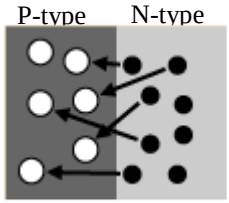


NMOS Enhancement Transistor

2.1.4 The pn Junction in PMOS

Pg 7

PN Junction



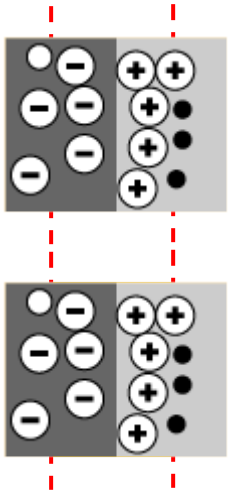
● Electron ○ Hole

⊖ Negative ion from filling of p-type vacancy.

⊕ Positive ion from removal of electron from n-type impurity.

Electron **filling a hole** in an atom on the p-side makes it a **negative ion**.

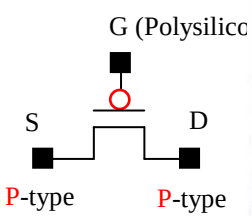
Electron **leaving** an atom leaves behind **a positive ion** on the n-side.



A space charge builds up, creating a depletion region (insulation) which inhibits any further electron transfer.

N and P regions are isolated from each other (open circuit). No further flow of carriers can take place

PN Junction in P-Transistor



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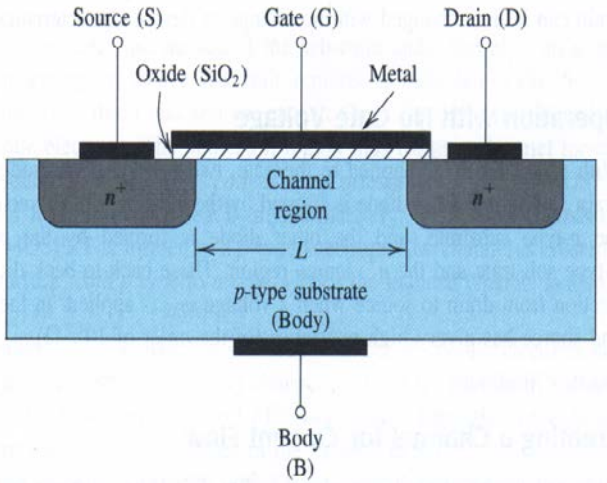

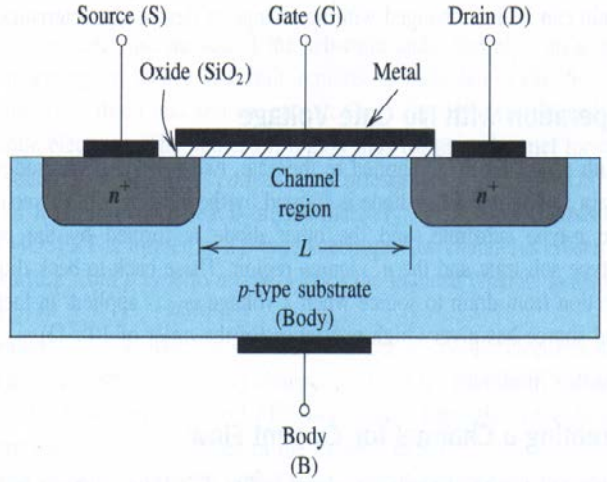

PMOS Enhancement Transistor