14s1

Solution to Question 1

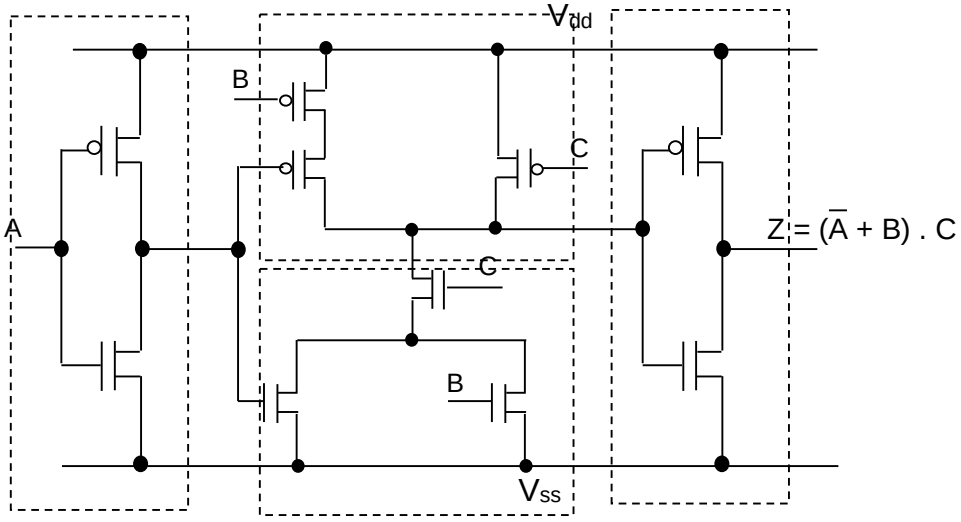
(i) resistance of wire = 23.25 R_{sM} Ω

(ii) capacitance of wire = relative area * relative capacitance * □Cg
= 8.7 □C_g F

(iii) Time taken = RC
= 20.25 R_{sM} * 7.8 □C_g
= 157.95 $\frac{R_{sn}}{R_{sn}}$ R_{sM} □C_g
= 157.95 (R_{sM}/R_{sn}) τ

Solution to Question 2

(b)



Solution to Question 3

(a) $G = \overline{(A\,C + B\,D)} \,.\, F$

(b) C_E = **6□C_g**

(i) Gate 1 : A = B = 1, C = D = 0
R = 0.625 R_{sn}
$T_{(OFF)}$ = RC
= 0.625 R_{sn} x 6□C_g
=3.75 τ

(ii) Gate 2 : V_E = "H", F = 1

$R = R_{sn}$

$T_{(ON)} = R_{sn} \times 3 \square C_g$
$= 3\tau$

Total delay = 6.75τ

Solution to Question 5

(c) (ii) The circuit is an 8-bit up-down counter with clear and pre-load feature.

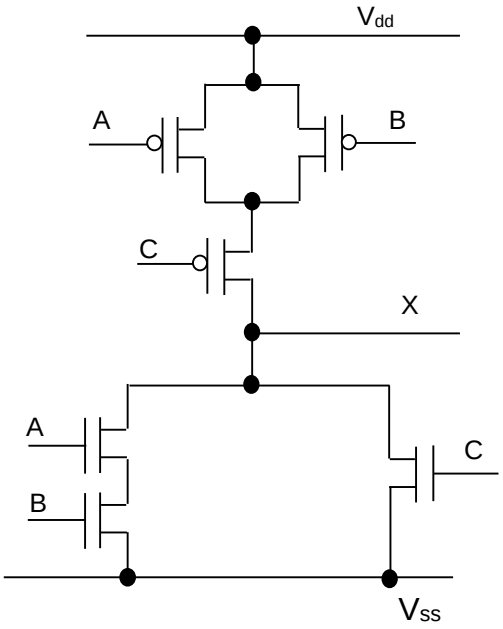
- When **clear** is low (0), counter is reset and **cnt** (**oData**) will be set to 0.
- When **clear** is high (1), counter can be initialized with the value from **data** or counting can proceed by setting load=0.
- Up or down counting depends on the signal at **up_down**.
    - If up_down=1, cnt (oData) will increment on the positive edge of clk
    - If up_down=0, cnt (oData) will decrement on the positive edge of clk

(iii) The module is a sequential circuit as the events are clock triggered as seen in the always @(posedge clk) statement.

14S2

Solution to Question 1

(b)(ii) Transistor Level Schematic

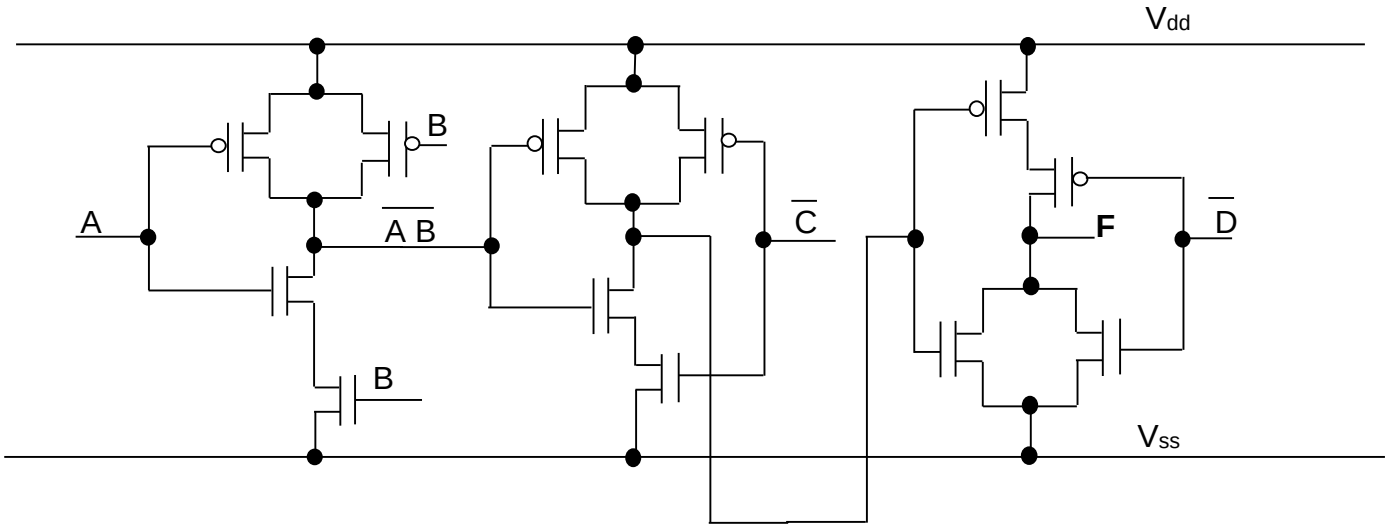


$X = \overline{A.B + C}$

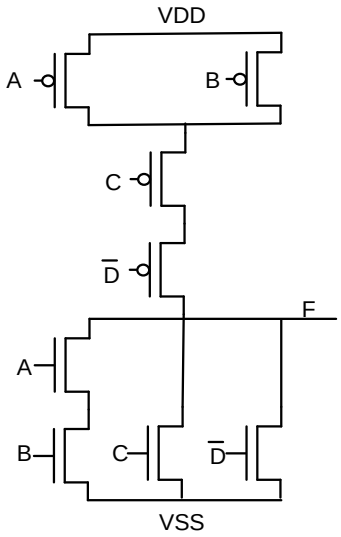
Solution to Question 3

(a) (i) $F = \overline{\overline{\overline{(\overline{AB}.\overline{C})} + \overline{D}}} = \overline{AB + C + \overline{D}}$

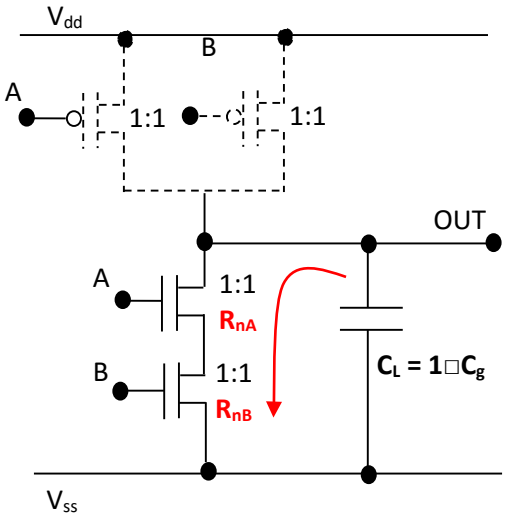
(ii) Function Implemented Using Standard Gates Concept



(iii)

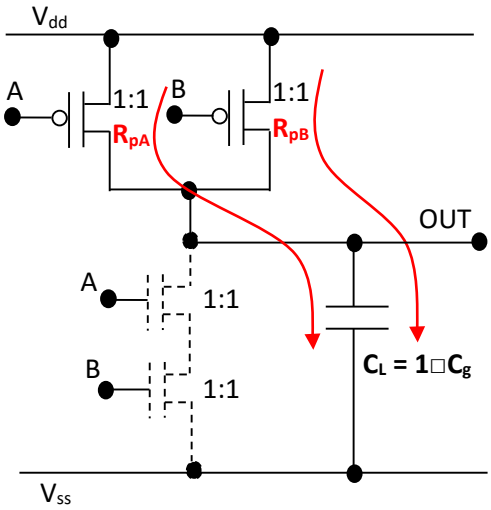


(b)(i)



tpHL = $2R_{sn}(1/1) * C_L$
= $2R_{sn} * 1\square C_g$
= 2τ

(b)(ii)



Time taken = tpLH
= $(R_{pA} // R_{pB}) * C_L$

= $\frac{1}{2}R_{sp}(1/1)* C_L$
= $\frac{1}{2}$ $(2.5R_{sn}) * 1\square C_g$
= 1.25τ

Solution to Question 4

(a)

(i) resistance of wire = 10 R_{spoly} Ω

(ii) capacitance of wire =15 □C_g F

(iii) Time taken = 10 R_{spoly} * 15 □C_g

$$= 150 \frac{R_{sn}}{R_{sn}} R_{spoly} \square C_g$$

$$= 150 \frac{R_{spoly}}{R_{sn}} \tau$$

solution to Question 5

(c) (ii) The circuit is a 4-bit up-down counter with synchronous clear feature.

- As **clr** is not in the sensitivity list, the counter will not reset instantaneously but have to wait for the positive edge of the clk to be present.

(iii) When the positive edge of the clock occurs,

- If **clr** is high (1), then counter will be initialized to zero.
- If **clr** is low (0), the up_down signal will be assessed.
  - If up_down=1, tmp will increment by 1
  - If up_down=1, tmp will decrement by 1

  The tmp value is then re-assigned to the output, q.

15S1

Solution to Question 1

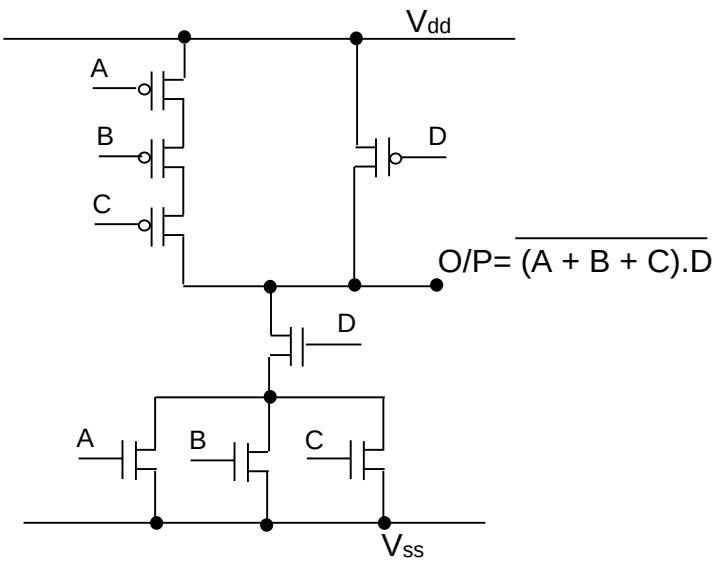
(i) resistance of wire = 14.75 R_{sM} Ω

(ii) capacitance of wire = relative area * relative capacitance * □Cg
= 4.1 □C_g F

(iii) Time taken = RC
= 14.75 R_{sM} * 4.1 □C_g
= 60.475 $\frac{R_{sn}}{R_{sn}}$ R_{sM} □C_g
= 60.475 (R_{sM}/R_{sn}) τ

Solution to Question 2

(e)



Solution to Question 3

(a) $G = \overline{(A\,C + B\,D)} \,.\, F$

(b) C_E = **6□C_g**

(i) Gate 1 : A = B = 1, C = D = 0
R = = 0.625 R_{sn}
$T_{(OFF)}$ = RC
= 0.625 R_{sn} x 6□C_g
=3.75 τ

(ii) Gate 2 : V_E = "H", F = 1

R = R_{sn}

$T(_{ON}) = R_{sn} \times 3 \square C_g$

$= 3\ \tau$

Total delay $=6.75\ \tau$

Solution to Question 5

(ii) The Rst signal is a synchronous signal. For reset to occur, the Rst has to be at logic 1 when the posedge of Clock occurs.

The purpose of this signal is to bring the circuit to a known state prior to the execution of the intended function.

(iii) The codes describe a 4-bit right-shift register (sequential circuit). When the Rst is at logic 1 and a posedge Clock occurs, the output (Q) is reset to 0; else the bits on the output will shift from MSB to LSB with the MSB taking the value of Data eventually.