Nanyang Polytechnic

School of Engineering

Diploma in Electronics Computer & Communications Engineering
(EGDF01)

EXPERIMENT NO	:	Lab 08 (Duration : 2 hours)
EXPERIMENT TITLE	:	Place and Route of Counter using Cadence Encounter
OBJECTIVE	:	To perform place and route of Counter

Exercise 1

To do place and route of the counter synthesized in Lab7 using Cadence software - Encounter.

1. Open a new Terminal
   Type :
   cd
   cd term2
   source cshrc

2. Change directory
   Type :
   cd EN
   encounter to launch the software. You should see Figure Lab8-1.

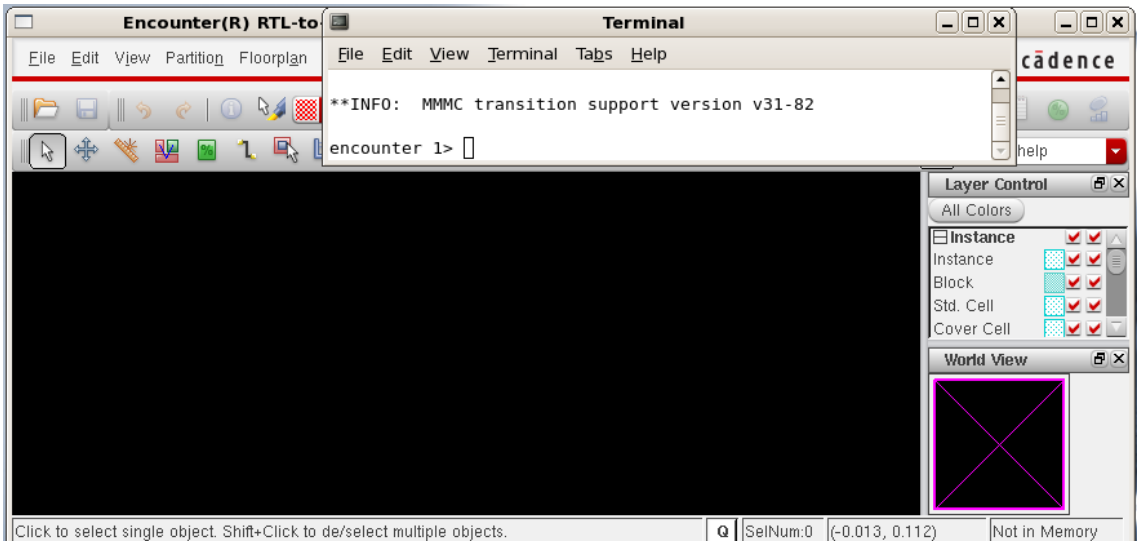

Figure Lab8-1 Encounter-shell Prompt

3. In Encounter GUI, **File→Import Design**.
As shown in Figure Lab8-2, click **Load**, select **counter.globals** and click **Open**.

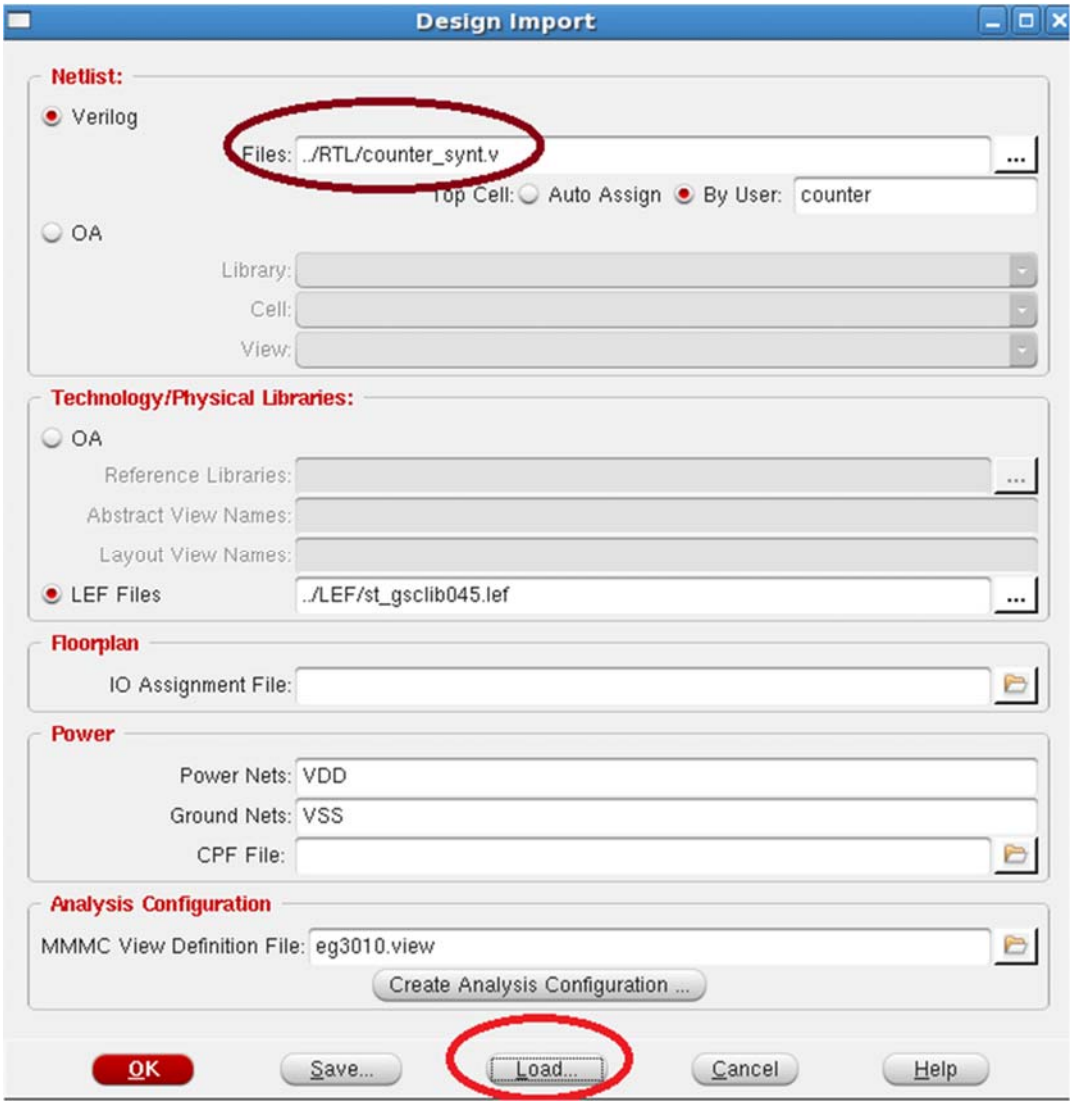

Figure Lab8-2 Import Design

4. Click on the icon (red cycle) as shown in Figure Lab8-3 and hit **f** to see the full view.

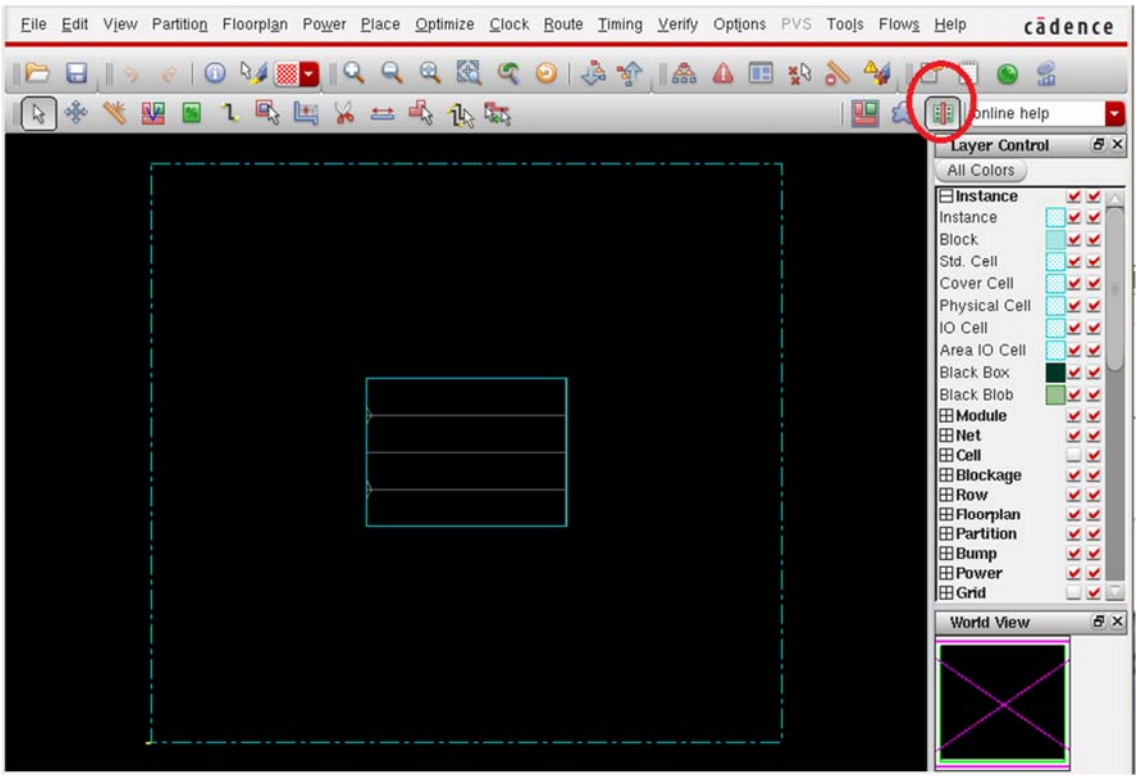

Figure Lab8-3 Ready for Floorplanning

5. Floorplanning:
Floor plan→Specify Floorplan. Key in the parameters as shown in Figure Lab8-4 and click **OK**.

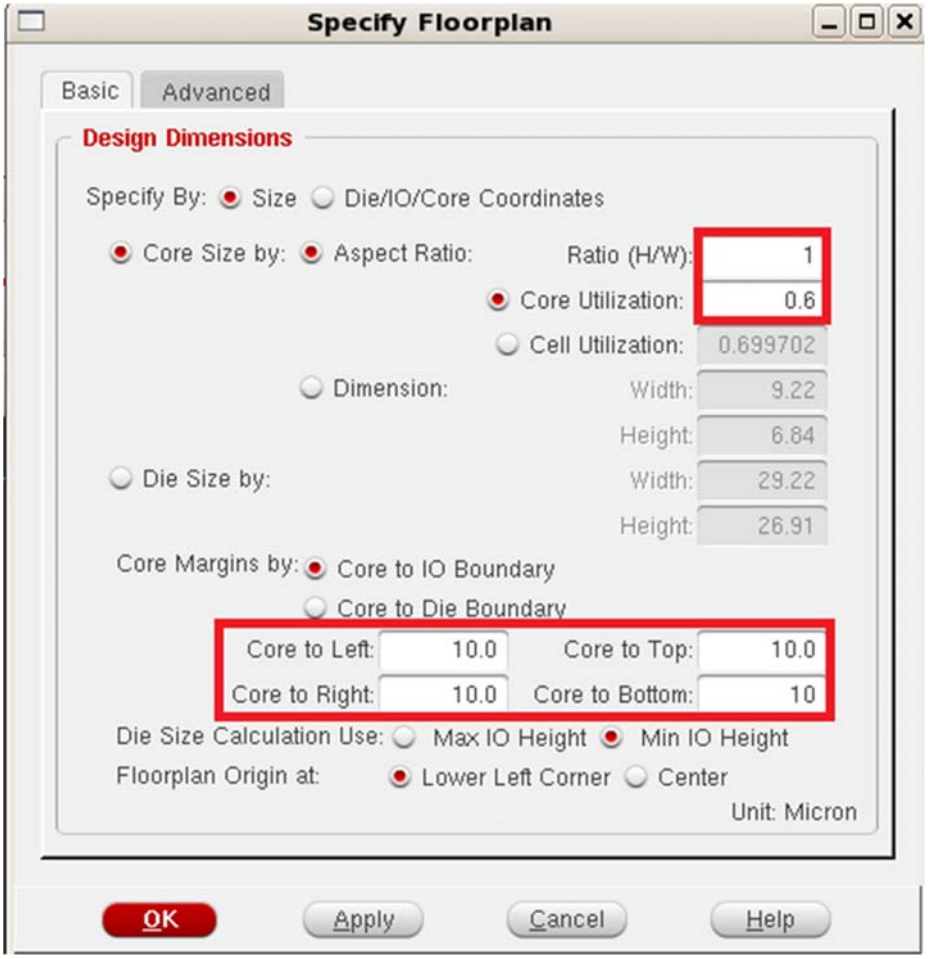

Figure Lab8-4 Floorplanning

6. We are going to add 2 supply rings for VDD and VSS.
Power→Power Planning→Add Ring. Key in the parameters as shown in Figure Lab8-5 and click **OK**.

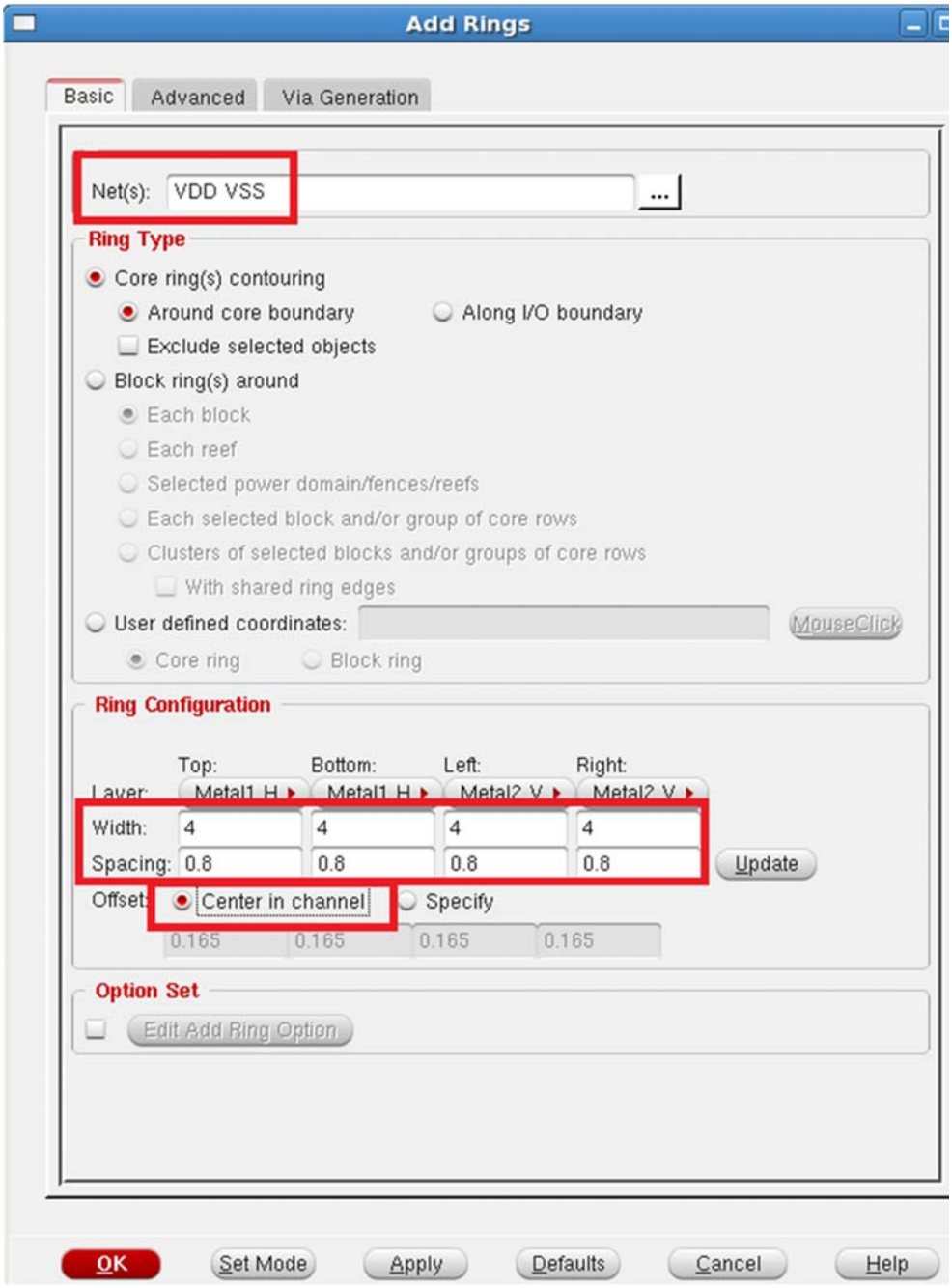

Figure Lab8-5 Add Power Ring

7. Upon completion of Step 6, the layout should be the same as shown in Figure Lab8-6. It is time to save the work thus far.
File→SaveDesign, check **Encounter** and call it **step1.enc**
Click **OK**.

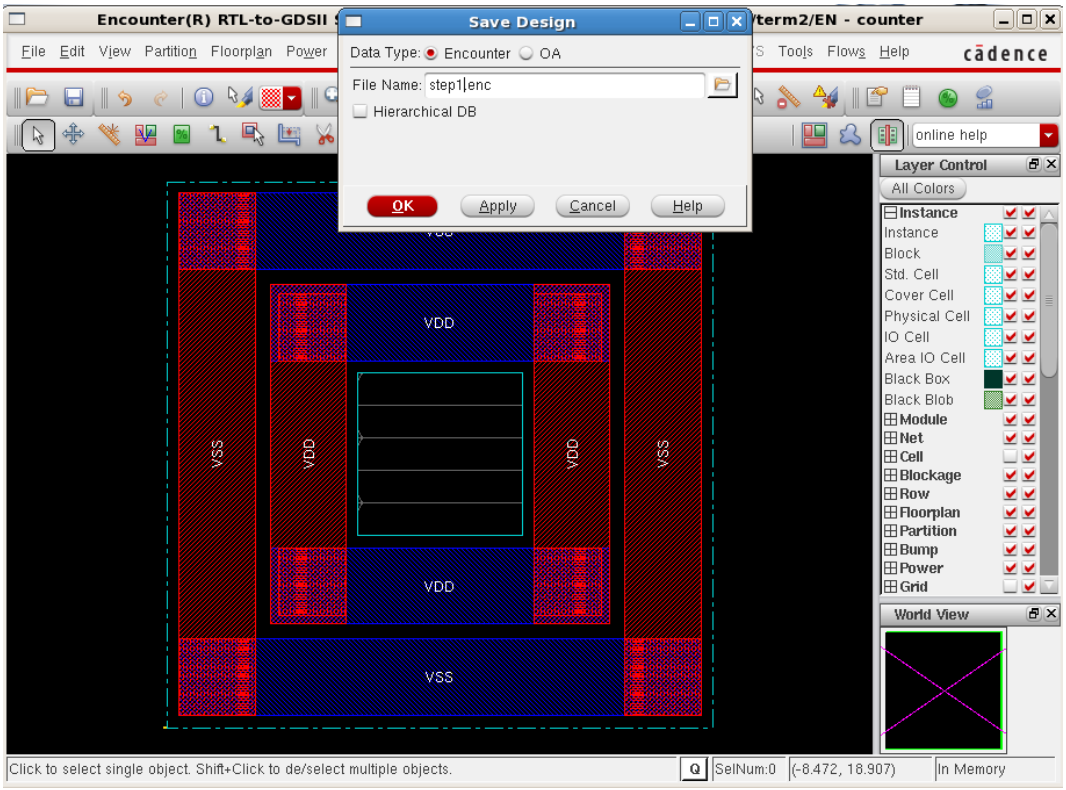

Figure Lab8-6 Save Design

8. Before we proceed further, we need to instruct Encounter to connect signals VDD or VSS, and signals that connect to logic high or logic low, to supply ring VDD and VSS respectively.

This can be done via the **Encounter-shell** as shown in Figure Lab8-7.

After typing and finish the first line of command, hit **ENTER**. To save effort in typing, hit **UP Arror Key** to bring up the previous command for modification. Key in the 4 commands as shown in the figure.

```
 0.000M) ***
encounter 1> globalNetConnect VDD -type pgpin -pin VDD -all
encounter 2> globalNetConnect VSS -type pgpin -pin VSS -all
encounter 3> globalNetConnect VDD -type tiehi
encounter 4> globalNetConnect VSS -type tielo
encounter 5>
```

Figure Lab8-7 Power Pins Connection

9. Gates are placed in the layout row-by-row. We need to provide supply rails for them. **Route→Special Route.** Key in parameters as shown in Figure Lab8-8.

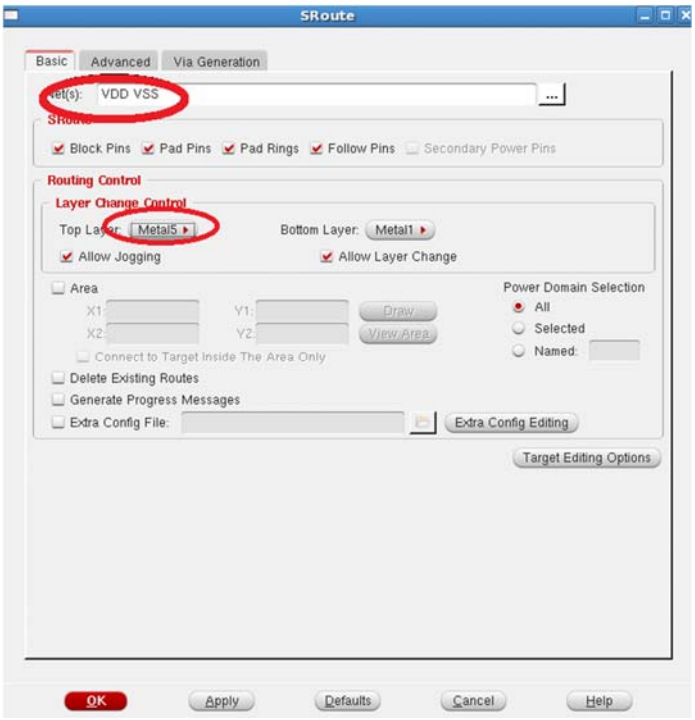

Figure Lab8-8 Supply Rails for Cells

10. Perform placement:
Place→Place Standard Cell. The cells should be placed as shown in Figure Lab8-9.
File→SaveDesign to **step2.enc**

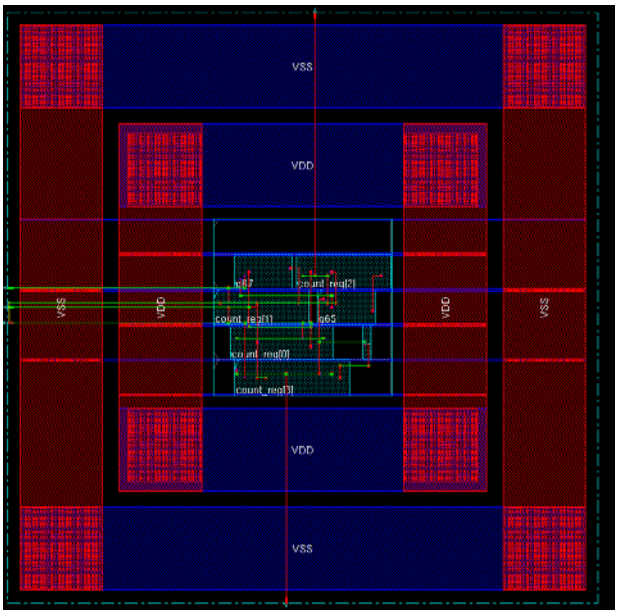

Figure Lab8-9 Placement

11. Routing

Route→ Nanoroute→Route to complete the routing.

Place→Physical Cell→Add Filler and select **FILL1, FILL1A, FILL2, FILL4, FILL8** as shown in Figure Lab 8-11. This will fill up the empty space.

This is the complete layout produce by the software.

File→SaveDesign to **step3.enc**

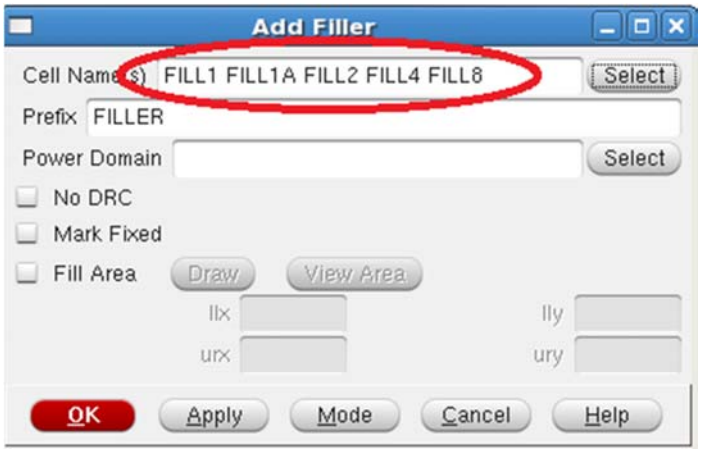

Figure Lab8-10 Add Filler

12. **File→Save Netlist** to save the netlist as **../RTL/counter_pnr.v**

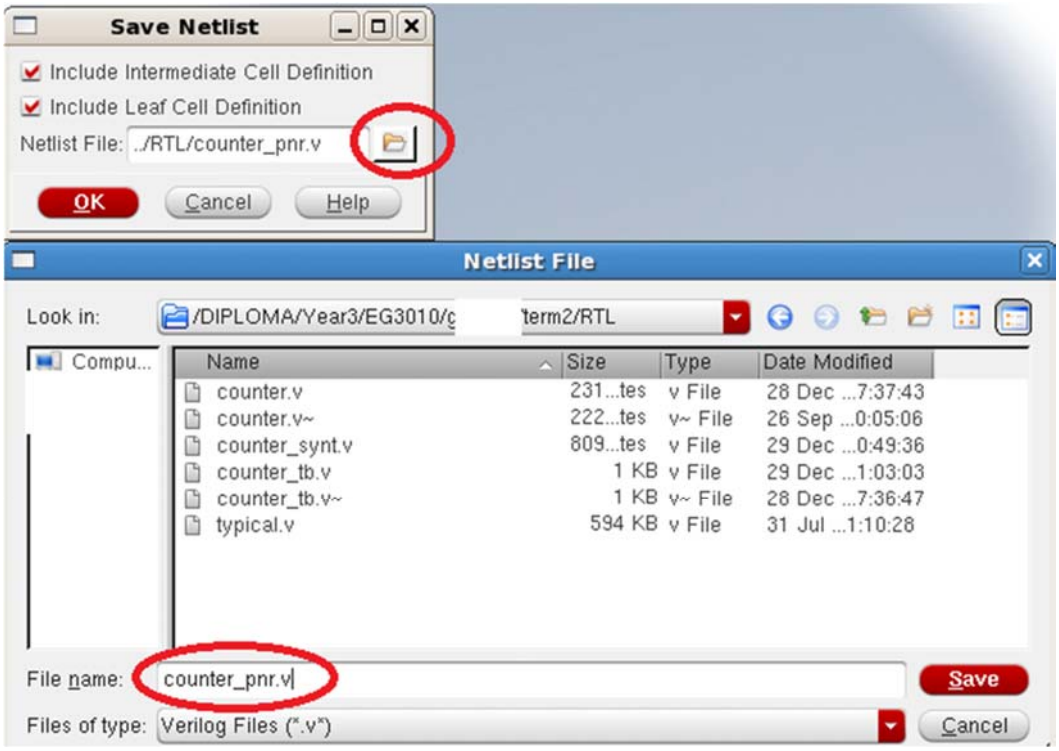

Figure Lab8-11 Save Netlist

13. **Timing→Extract RC** (as shown in Figure Lab8-12) to extract R and C of all the wires.

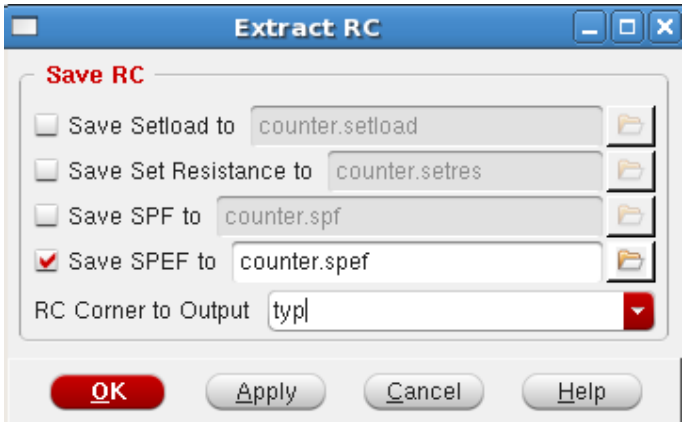

Figure Lab8-12 RC Extraction

14. From the Extracted RC file, a file that describes delay of all the wires can be produced.
Timing→Write SDF.
As shown in Figure Lab8-13, change to directory **RTL** and provide a file name of **counter.sdf**
Click **Save** and then **OK**.
We are ready to simulate the circuit again with the delay of wires included.

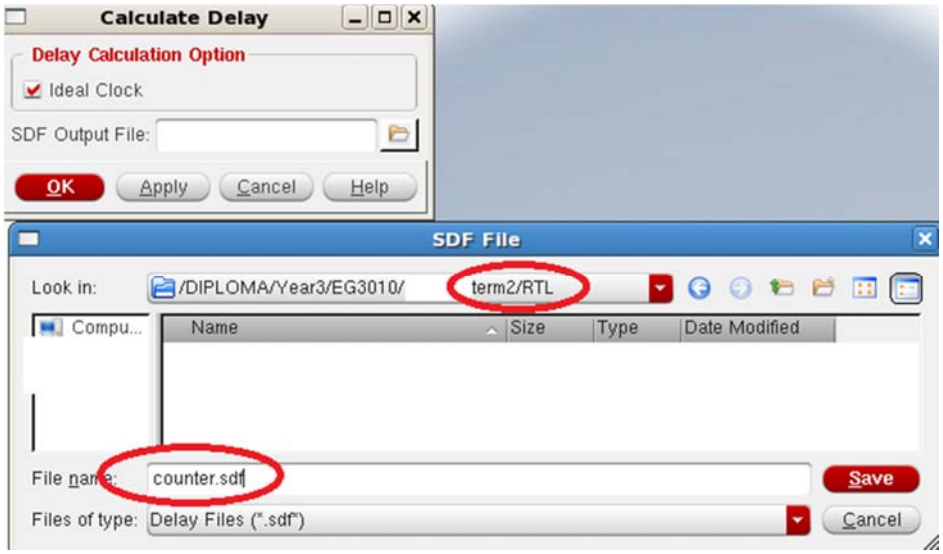

Figure Lab8-13 Delay Calculation

Exercise 2 : Post-layout simulation

1. We are going to simulate the circuit again but this time with all the delay of wiring (post-layout) taken care of. Refer to Lab7 Exercise 1 if you are not sure about the commands of the simulator.

2. Type :
   cd
   cd term2
   source cshrc
   nclaunch&

3. Select **counter_tb.v** and **right-click→Edit**.
   For the statement "define XXX", replace it with "define **PAR**".
   Select **counter_pnr.v** and **counter_tb.v** and **right-click→NCVlog.**

4. Select **worklib/counter_tb** and **right-click→NCElab**.
   Select **Snapshot/worklib.counter_tb:module** and **right-click→NCSim**.
   Select counter_tb and **right-click→Send To New→Waveform Window**.
   Select **count_tb[3:0]**. **Simulation→Run**.
   Zoom in to **count_tb[3:0]=F** as shown in Figure Lab8-14.
   Click on waveform to bring **TimerA** to the desired location.
   Right-click→Create a marker to put additional marker.

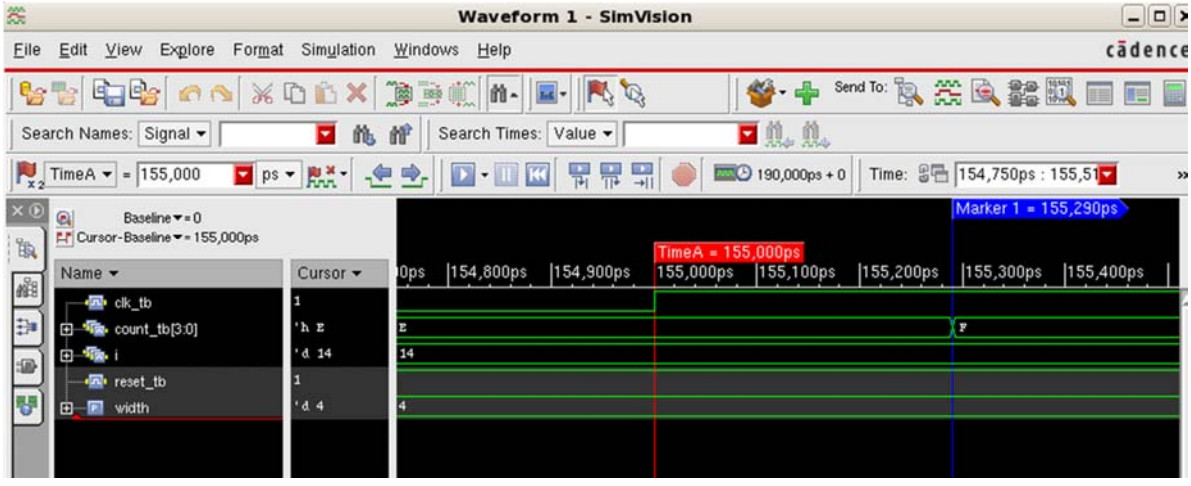

Figure Lab8-14 Result

5. As you can see, there is delay of **290ps** between postive-edge of **clk_tb** and counter's output. This is due to the gate delay and wire delay, since now we are simulating a post-layout netlist.