

## School of Engineering

# Diploma in Electronics Computer & Communications Engineering (EGDF01)

EXPERIMENT NO	:	Lab 08 (Duration : 2 hours)
EXPERIMENT TITLE	:	Place and Route of Counter using Cadence Encounter
OBJECTIVE	:	To perform place and route of Counter

### Exercise 1

To do place and route of the counter synthesized in Lab7 using Cadence software - Encounter.

- 1. Open a new Terminal Type : cd cd term2 source cshrc
- 2. Change directory

Type :

cd EN

encounter to launch the software. You should see Figure Lab8-1.



Figure Lab8-1 Encounter-shell Prompt

## 3. In Encounter GUI, **File→Import Design**.

As shown in Figure Lab8-2, click Load, select counter.globals and click Open.

Netlist: • Verilog		
Verilog		
Con . C		
Files: .	/RTL/counter_synt.v	]
	Top Cell: 🔾 Auto Assign 💿 By User: 🛛 counter	
) OA		
Library:		-
Cell:		-
View:		•
Technology/Physical Libra	ries:	
) OA		
Reference Libraries:		
Abstract View Names:		
Layout View Names:		
LEF Files	/LEF/st_gsclib045.lef	
Floorplan		
IO Assignment File:		6
Power		
Power Nets:	/DD	
Ground Nets:	/SS	
CPF File:		e
Analysis Configuration —		
MMMC View Definition File:	eg3010.view	0
	Create Analysis Configuration	
ОК	Save Cload Cancel H	eln

Figure Lab8-2 Import Design

4. Click on the icon (red cycle) as shown in Figure Lab8-3 and hit **f** to see the full view.



Figure Lab8-3 Ready for Floorplanning

## 5. Floorplanning:

Floor plan→Specify Floorplan. Key in the parameters as shown in Figure Lab8-4 and click OK.

Specif	y Floorp	lan	
asic Advanced			
Design Dimensions			
Specify By: 💿 Size 🔾 Die/	10/Core Co	ordinates	
🥑 Core Size by: 🖲 Aspe	ct Ratio:	Ratio (H/W):	1
	۲	Core Utilization:	0.6
	C	Cell Utilization:	0.699702
🔾 Dime	nsion:	Width:	9.22
		Height:	6.84
Die Size by:		Width:	29.22
		Height:	26.91
Core Margins by: 🥑 Core	to IO Bound	dary	
Core	to Die Bour	ndary	
Core to Left:	10.0	Core to Top:	10.0
Core to Right:	10.0	Core to Bottom:	10
Die Size Calculation Use:	Max IO	Height 🥑 Min IC	) Height
Floorplan Origin at:	🥑 Lower Le	eft Corner 🔾 Cent	ter
			Unit: Micr

Figure Lab8-4 Floorplanning

6. We are going to add 2 supply rings for VDD and VSS.

1

**Power**→**Power Planning**→**Add Ring**. Key in the parameters as shown in Figure Lab8-5 and click **OK**.

	VDD VSS			<u></u>	<u>,</u>
-Ring Ty	pe	a cola a			
● Core	ring(s) cont round core	ounng boundary	Along I	/O houndary	
Ē	xclude selei	cted objects	<ul> <li>Along I</li> </ul>	o boundary	
O Block	ring(s) arou	und			
. E	ach block				
O E	ach reef				
O S	elected pow	/er domain/fenc	es/reefs		
O E	ach selecte	d block and/or	group of core	rows	
O C	lusters of se	elected blocks a	and/or groups	of core rows	
1	With shar	ed ring edges			
O User	defined coo	rdinates:			MouseClin
۲	Core ring	<ul> <li>Block rin</li> </ul>	ng		
Ring Co	onfiguration				
	Ton	Dottom	L offi	Diabt	
Laver	Metal1 H	H Metal1 H	H Metal2	V Metal2 V	/ •
Width:	4	4	4	4	
Spacing	g: 0.8	0.8	0.8	0.8	<u>U</u> pdate
Offset:	<ul> <li>Center</li> </ul>	in channel	Specify		
	0.165	0.165	0.165	0.165	
	Pat				
0.11	Sof				
Option	Jet				
Option	dit Add Ring	Option			
Option	dit Add Ring	Option )			

Figure Lab8-5 Add Power Ring

 7. Upon completion of Step 6, the layout should be the same as shown in Figure Lab8-6. It is time to save the work thus far.
 File→SaveDesign, check Encounter and call it step1.enc Click OK.

Encounter(R) RTL-	to-GDSII S	Save Design		term2/EN - counter	_ <b> </b>
<u>F</u> ile <u>E</u> dit V <u>i</u> ew Partitio <u>n</u> Floorpl	<u>a</u> n Po <u>w</u> er	Data Type: 🖲 Encounter 🔾 OA		S Too <u>l</u> s Flow <u>s H</u> elp	cādence
<b>                                   </b>		File Name: step1]enc		N Solution Continue	help 🔽
		OK Anniv Cancel	Heln	All Colors	
			Tob	Instance Instance Block Std. Cell Cover Cell	
		VDD		Physical C IO Cell	
				Black Box	
SS	QQA	,	SSV	Black Blob Hodule Net Cell Blockag Row Floorpla Horpla	
		VDD		⊞ Bump ⊞ Power ⊞ Grid World Vie	
		VSS			
Click to select single object. Shift+Clic	k to de/selec	t multiple objects.	Q SelN	um:0 (-8.472, 18.907) In	Memory

Figure Lab8-6 Save Design

8. Before we proceed further, we need to instruct Encounter to connect signals VDD or VSS, and signals that connect to logic high or logic low, to supply ring VDD and VSS respectively.

This can be done via the **Encounter-shell** as shown in Figure Lab8-7.

After typing and finish the first line of command, hit **ENTER**. To save effort in typing, hit **UP Arror Key** to bring up the previous command for modification. Key in the 4 commands as shown in the figure.

```
0.000M) ***
encounter 1> globalNetConnect VDD -type pgpin -pin VDD -all
encounter 2> globalNetConnect VSS -type pgpin -pin VSS -all
encounter 3> globalNetConnect VDD -type tiehi
encounter 4> globalNetConnect VSS -type tielo
encounter 5>
```

Figure Lab8-7 Power Pins Connection

9. Gates are placed in the layout row-by-row. We need to provide supply rails for them. **Route→Special Route.** Key in parameters as shown in Figure Lab8-8.

Routing Control Layer Change Contro	L	
Top Layer Metal5	Bottom Layer:	Metal1 •
Allow Jogging	🗹 Allov	v Layer Change
Artea     X1     Connect to Tar     Delete Existing Rou     Generate Progress     Extra Config File:	Y1: Y2 get Inside The Area Only tes Messages	View Area Extra Config Editing
		Target Editing Option

Figure Lab8-8 Supply Rails for Cells

10. Perform placement:

Place → Place Standard Cell. The cells should be placed as shown in Figure Lab8-9. File → SaveDesign to step2.enc



Figure Lab8-9 Placement

11. Routing

Route→ Nanoroute→Route to complete the routing. Place→Physical Cell→Add Filler and select FILL1, FILL1A, FILL2, FILL4, FILL8 as shown in Figure Lab 8-11. This will fill up the empty space. This is the complete layout produce by the software.

File→SaveDesign to step3.enc

	Add Filler		_ 🗆 🗙
Cell Name (s)	FILL1 FILL1A FILL2 F	ILL4 FILL8	Select
Prefix FILLER			
Power Domain			Select
No DRC			
Mark Fixed			
🔲 Fill Area	Draw View Ar	rea	
	lix	lly	
	urx	ury	
<u>0</u> K	Apply Mode	Cancel	Help

Figure Lab8-10 Add Filler

## 12. File→Save Netlist to save the netlist as ../RTL/counter\_pnr.v

□ Sav ✓ Include Int ✓ Include Le Netlist File:	ve Netlist _ D × ermediate Cell Definition af Cell Definition /RTL/counter_pnr.v				
<u>0</u> K	Cancel Help				
	N	etlist File			0
Look in:	PLOMA/Year3/EG3010/g	term2/RTL	-	0066	
🛋 Compu	. Name	∧ Size	Туре	Date Modified	
	Counter.v	231tes	v File	28 Dec7:37:43	
	🗋 counter.v~	222tes	v~ File	26 Sep0:05:06	
	🗋 counter_synt.v	809tes	v File	29 Dec0:49:36	
	🗎 counter_tb.v	1 KB	v File	29 Dec1:03:03	
	Counter_tb.v~	1 KB	v~ File	28 Dec7:36:47	
	🗋 typical.v	594 KB	v File	31 Jul1:10:28	
File <u>n</u> ame:	counter_pnr.v				<u>S</u> ave
Files of type:	Verilog Files (*.v*)				<u>C</u> ancel

Figure Lab8-11 Save Netlist

13. **Timing→Extract RC** (as shown in Figure Lab8-12) to extract R and C of all the wires.

<b>—</b> I	Extract RC			
Save RC				
🔲 Save Setload to	counter.setload	Þ		
📃 Save Set Resista	ance to counter.setres	Þ		
🔲 Save SPF to 🛛	ounter.spf	e		
🗹 Save SPEF to	counter.spef	D		
RC Corner to Outpu	ut [typ]			
	<u>Apply</u> <u>Cancel</u>	elp		

Figure Lab8-12 RC Extraction

14. From the Extracted RC file, a file that describes delay of all the wires can be produced.

#### Timing→Write SDF.

As shown in Figure Lab8-13, change to directory **RTL** and provide a file name of **counter.sdf** 

#### Click Save and then OK.

We are ready to simulate the circuit again with the delay of wires included.

Calculate Delay	
Delay Calculation Option	
🗹 Ideal Clock	
SDF Output File:	
OK Apply Cancel Help	
	SDF File X
Look in: E/DIPLOMA/Year3/EG3010/	(term2/RTL) 🔽 🚱 🛞 📂 🖼 🛅
Compu Name	Size Type Date Modified
File name: counter.sdf	Save
Files of type: Delay Files (".sdf")	Cancel

Figure Lab8-13 Delay Calculation

#### **Exercise 2 :** Post-layout simulation

- 1. We are going to simulate the circuit again but this time with all the delay of wiring (post-layout) taken care of. Refer to Lab7 Exercise 1 if you are not sure about the commands of the simulator.
- 2. Type : cd cd term2 source cshrc nclaunch&
- Select counter\_tb.v and right-click→Edit.
   For the statement "define XXX", replace it with "define PAR".
   Select counter\_pnr.v and counter\_tb.v and right-click→NCVlog.
- Select worklib/counter\_tb and right-click→NCElab.
   Select Snapshot/worklib.counter\_tb:module and right-click→NCSim.
   Select counter\_tb and right-click→Send To New→Waveform Window.
   Select count\_tb[3:0]. Simulation→Run.
   Zoom in to count\_tb[3:0]=F as shown in Figure Lab8-14.
   Click on waveform to bring TimerA to the desired location.
   Right-click→Create a marker to put additional marker.

85 C	Waveform 1 - SimVision	- 0 >
<u>File Edit View Explore Format Simulation</u>	<u>₩</u> indows <u>H</u> elp	cādence
🎭 📷 🚱 😭 🗠 🖄 🛍 🗙 🔅	)	🛛 🗳 - 🕂 Send To: 🗽 🏔 🏔 🎕 🛄 📰 📰
Search Names: Signal 🗸 🔽 👬	Y Search Times: Value 🕶	<b>n</b> (). ().
R = 155,000 ■ ps = R =	💁 🛛 🕶 🖾 🔛 🖬 📦	190,000ps + 0 Time: 3 154,750ps : 155,51
Baseline = 0 Cursor-Baseline = 155,000ps	TimeA	Marker 1 = 155,290ps
Name - Cursor -	10ps  154,800ps  154,900ps  155,00	00ps  155,100ps  155,200ps  155,300ps  155,400ps
1113 clk_tb 1		
Image: The second s	E	P
🔂 🗹 'd 14	14	
🔤 — 🜆 reset_tb 1		
🐨 🗉 width 'd.4	4	



5. As you can see, there is delay of **290ps** between postive-edge of **clk\_tb** and counter's output. This is due to the gate delay and wire delay, since now we are simulating a post-layout netlist.