School of Engineering

Diploma in Electronics Computer & Communications Engineering
(EGDF01)

EXPERIMENT NO	:	Lab 06 (Duration : 4 hours)
EXPERIMENT TITLE	:	Full Custom IC Design of CMOS NOR Gate & OR Gate
OBJECTIVE	:	1. Use Virtuoso Layout Editor for Custom IC Layout of CMOS NOR gate 2. Instantiate the layout of the NOR gate and Inverter to form a CMOS OR gate 3. Apply Design Rule Check, Extraction and Layout versus Schematic Check on the completed layout

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Exercise 1 : Create the ***mask layout*** of the NOR gate in the library 'class' and schemiatc 'term2_nor'.

(i) The layout shall be based on the 90nm design rules.

(ii) The layout should lie within a P&R boundary of H=3u W=3u.

Ensure the final layout passes the Assura-DRC and Assura-LVS checks.

Exercise 2 : Create the ***mask layout*** of the OR gate captured in library 'class' and schemiatc 'term2_or' by:

(i) Instantiating the Inverter done in Lab 5.

(ii) Instantiating the NOR gate done in Lab 6 Exercise 1.

(iii) Interconnecting the NOR gate and the Inverter to form an OR gate.

(iv) The layout should lie within an area boundary H=3u W=5u.

Ensure the final layout passes the Assura-DRC and Assura-LVS checks.