Nanyang Polytechnic

School of Engineering

Diploma in Electronics Computer & Communications Engineering
(EGDF01)

EXPERIMENT NO	:	Lab 05 (Duration : 2 hours)
EXPERIMENT TITLE	:	Familiarization with Virtuoso Layout Tool and Perform Full Custom IC layout of CMOS Inverter
OBJECTIVE	:	1. Learn to use Virtuoso Layout Editor for Custom IC Layout of Basic Devices 2. Apply Design Rule Check and Layout versus Schematic Check on the completed layout

---

Virtuoso Layout Editor for Custom IC Layout of Basic Devices

Exercise : Create the ***mask layout*** of the inverter circuit done in Lab 3.
The layout shall be based on the 90nm design rules given on Page 10.

Prequsite : Edit the schematic diagram of the inverter (lab 3) such that :-
PMOS : Finger Width=280n, L=100n,
NMOS : Finger Width=120n and L=100n.

1. Familization of Virtuoso Layout Editor

(a) From Library Manager window

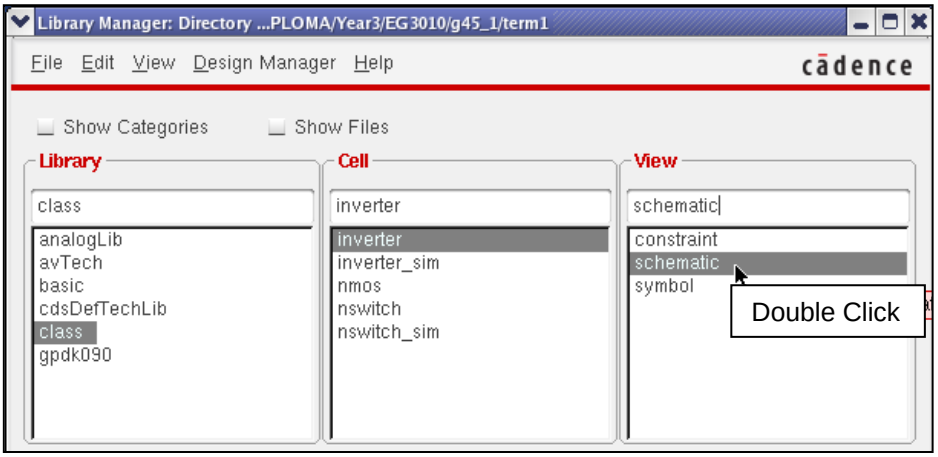


Figure Lab5-1 : Library Manager

(b) Activate Layout Editor
Launch → Layout XL

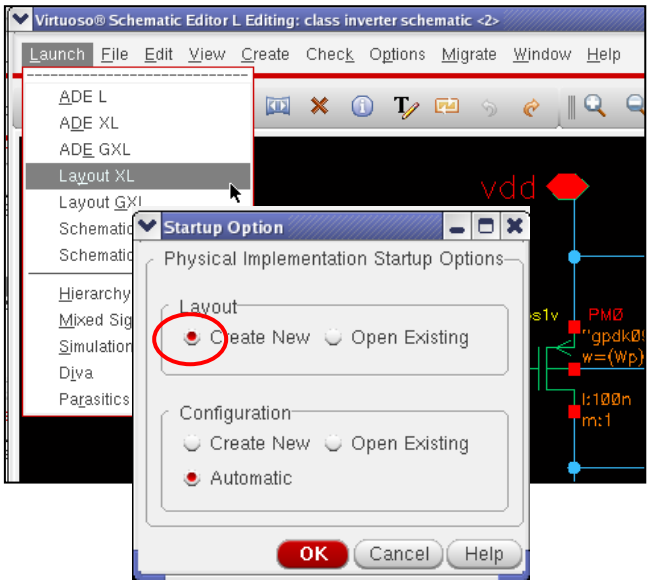


Figure Lab5-2 : Launch Layout XL

(c) Open Layer Palette

Window → Assistants → Layer

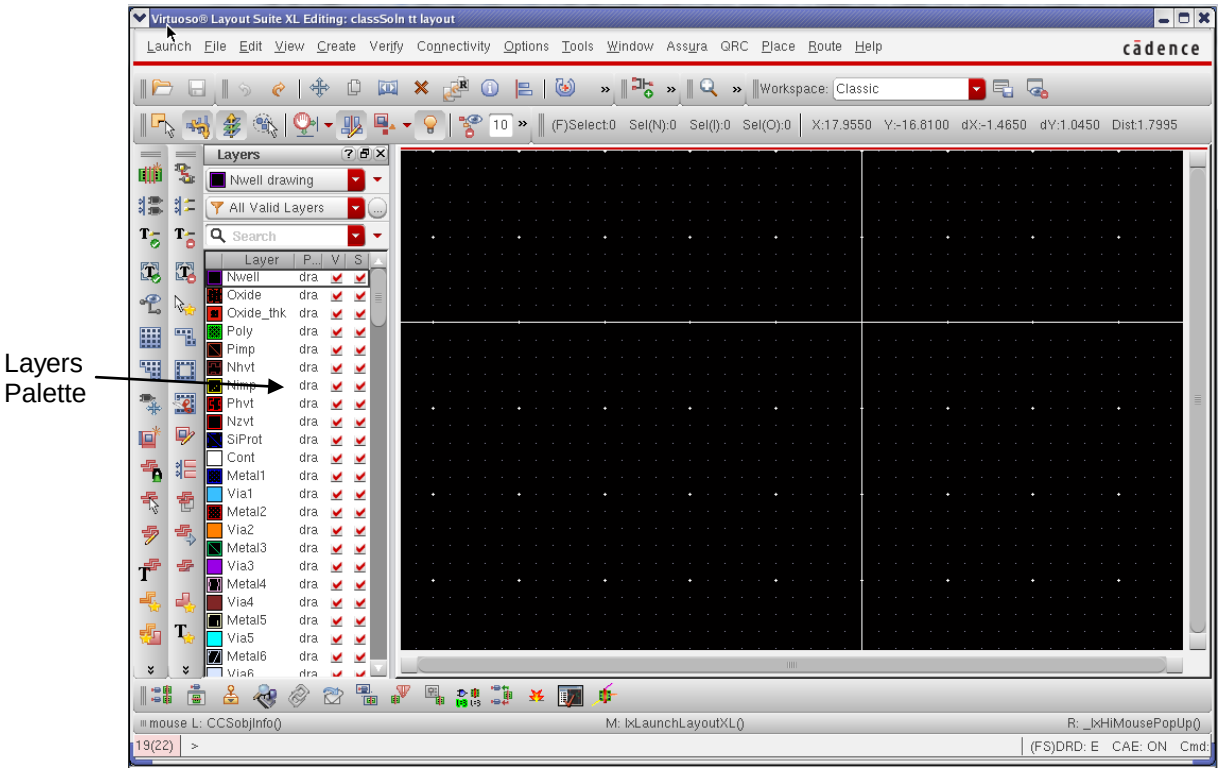


Figure Lab5-3 : Layout-XL Editor Window with Layer Palette

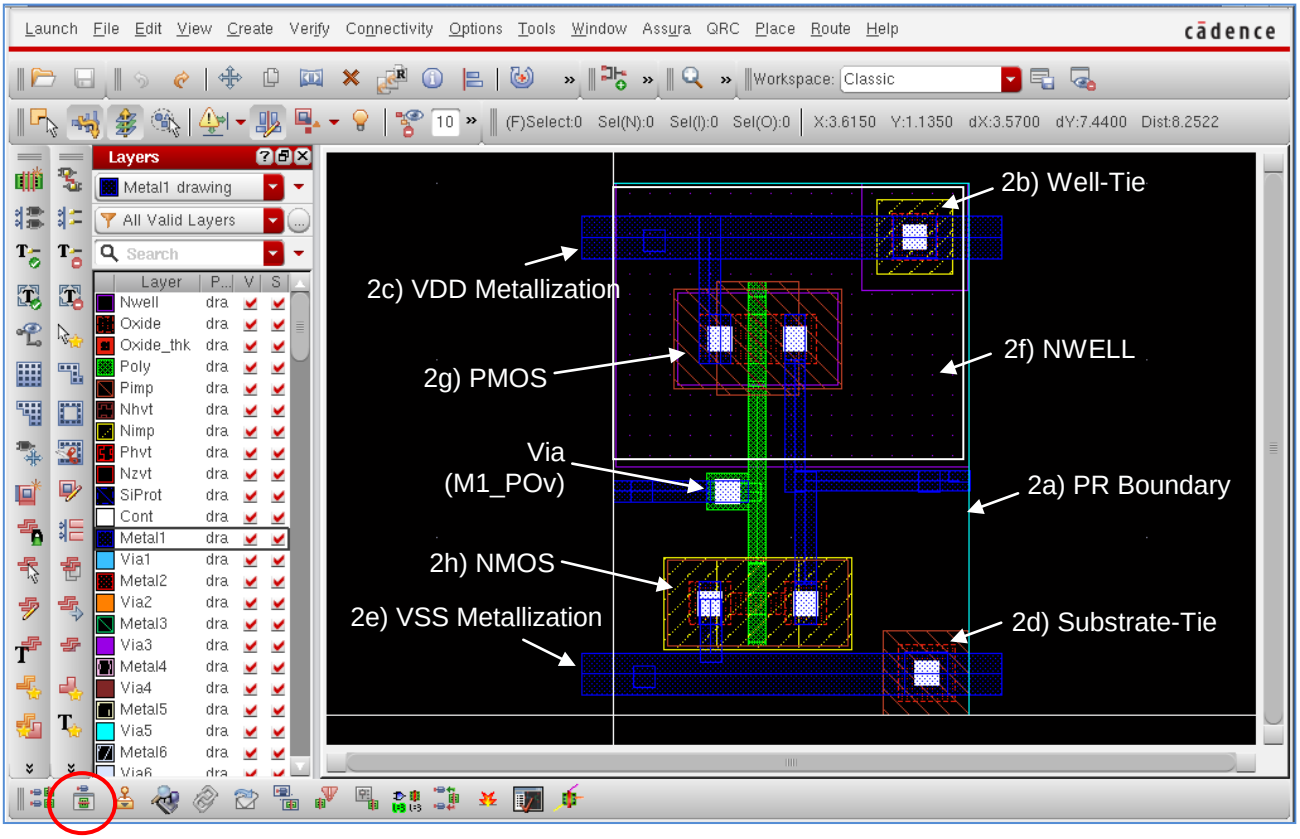
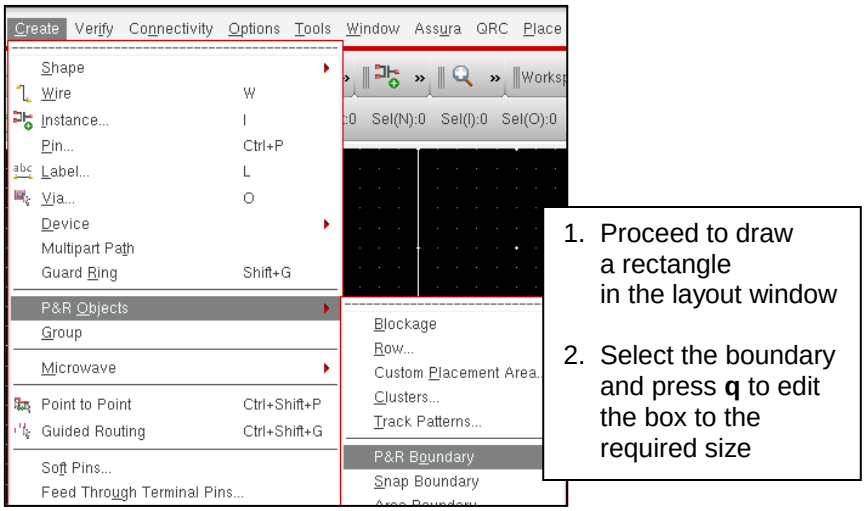


Figure Lab5-4 : Mask Layout Design Environment

2. **Create Layout** (Figure Lab5-4)

(a) Draw layout boundary of height = 3um and width = 2um
Create → P&R Objects → P&R Boundary



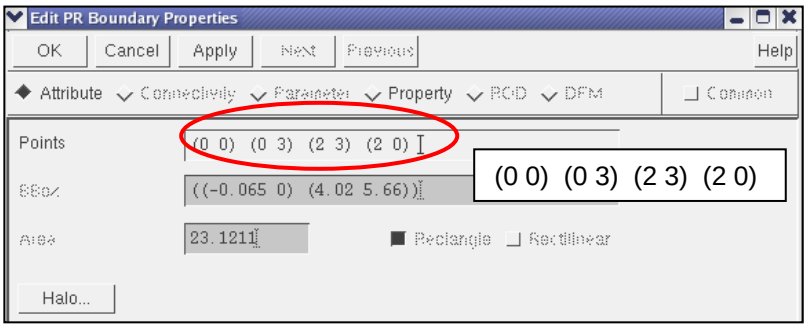


Figure Lab5-6 : Edit P&R Boundary Properties

(b) Create **Well-Tie**
Create → Via

Figure Lab5-7 : Add Well-Tie

(c) Create **vdd** metalization

(i) ***Create → wire***

(ii) Click the ***well-tie*** created in (b)

(iii) Select **Metal1**

(iv) Move **mouse** to desired position, hit **Enter**

(v) Change thickness of vdd to 0.36um
Click the **vdd** wire, press **q**

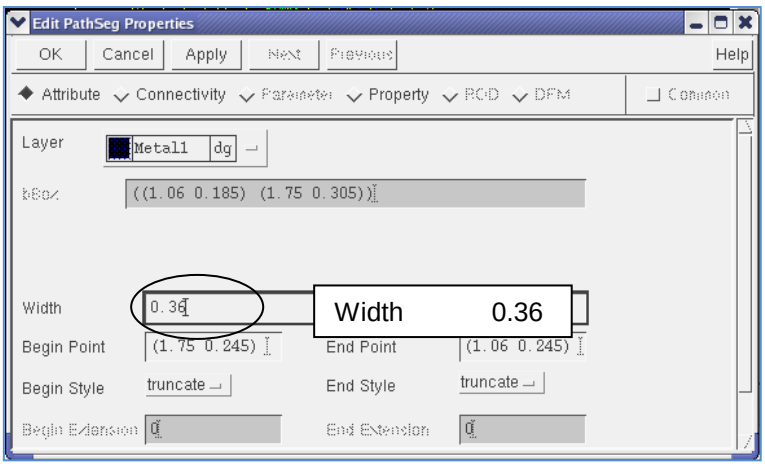


Figure Lab5-8 : Edit Property of Object

(d) Create **Substrate-Tie**
Repeat Step 2(b), select **M1_PSUB**

(e) Create **vss** metallization
Repeat Step 2(c)

(f) Draw NWELL

(i) From the Layer palette, select **NWELL** (drawing) layer

(ii) In the Layout window, create a rectangle
Create → Shape → Rectangle (or press r)

(g) Transfer component from Schematic to Layout

(i) Click on the ***Generate Selected From Source*** icon (circled in Figure Lab5-4)

(ii) From the schematic window, select the PMOS

(iii) Move mouse to the layout window, **place** the PMOS in the NWELL (without violating the design rule)

(h) Repeat Step (g) to transfer the NMOS from the schematic to the layout editor.

(j) Complete the connections (refer to page 9 for Routing Basics).

(k) Repeat Step (g) to transfer the pins ***inA***, ***outA***, ***vdd*** and ***vss*** from the schematic to the layout.

3. Assura Design Rule Checker and Extractor

Design Rule Check is to verify that the spacing, extension, enclosure and other design rules are adhered during the creation of the layout.

(a) On the Virtuoso window
Assura → Run DRC

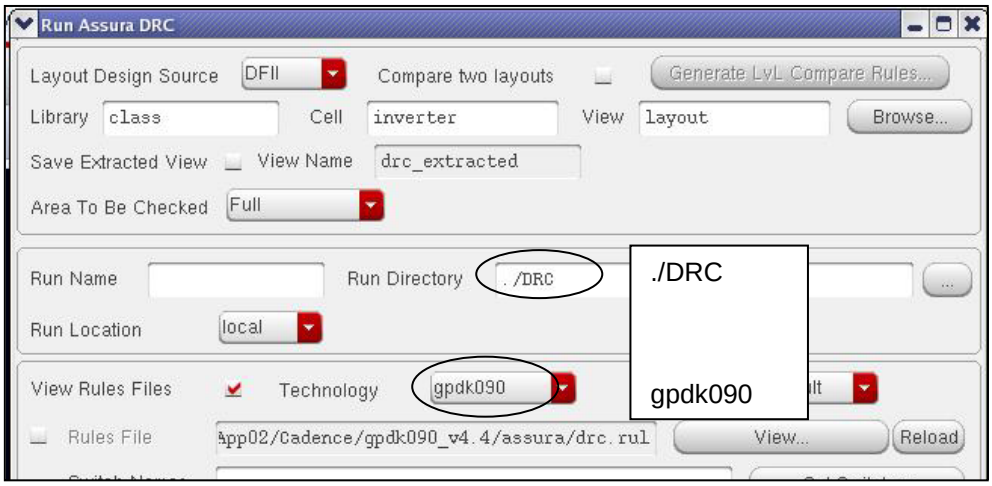


Figure Lab5-10 : DRC Window

(b) To locate DRC errors and correct errors
On the Virtuoso window
Assura → Open Run → OK

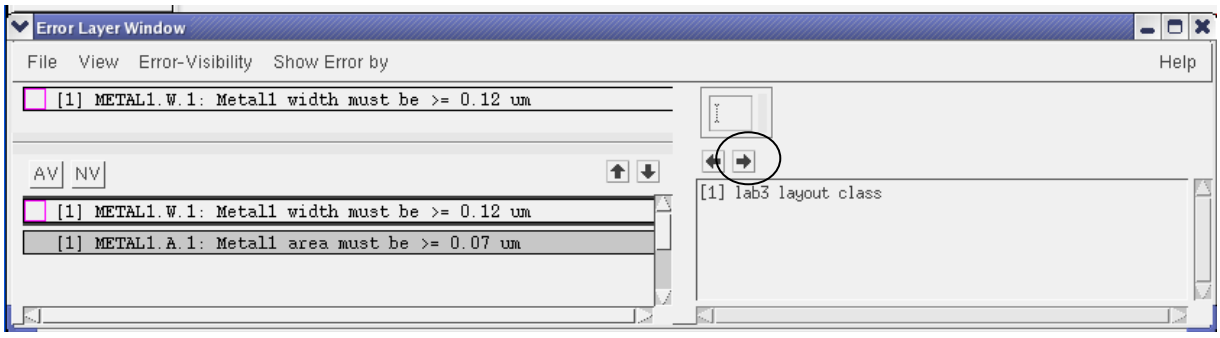


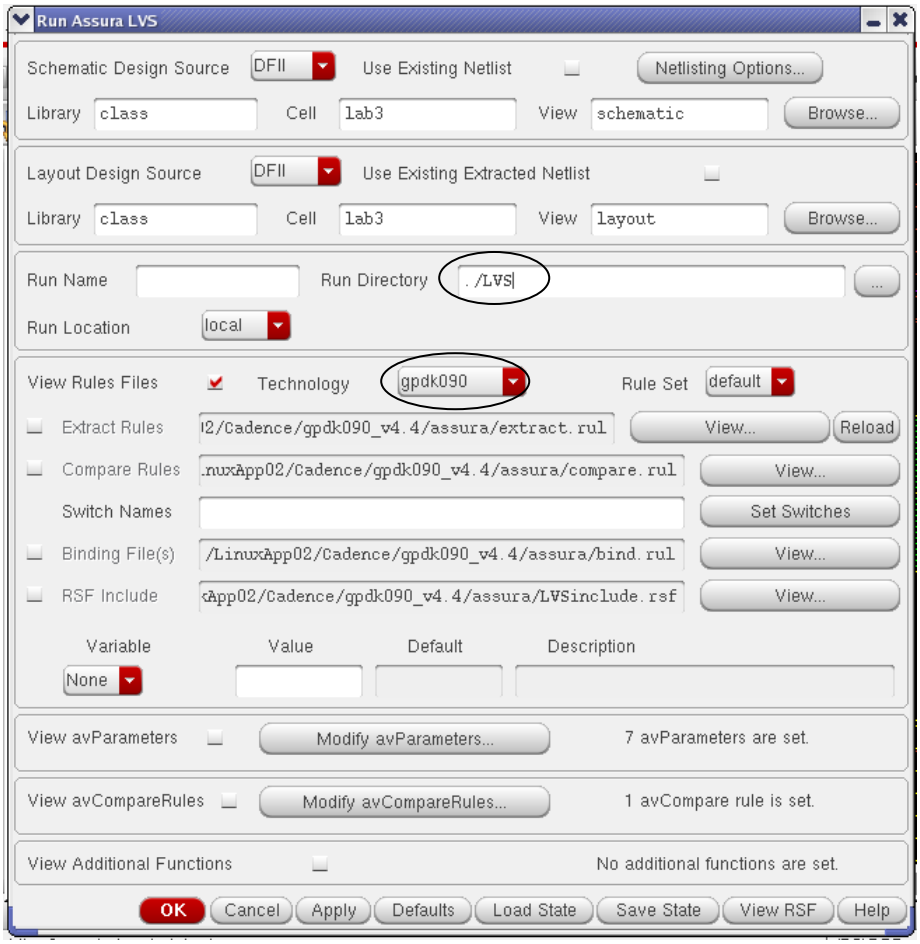
Figure Lab5-11 DRC Error Search & Display

(c) Correct the errors and check DRC until there is no more errors.

4. Assura Layout versus Schematic Checker

Layout versus Schematic Check (LVS) is to verify that the geometry is the intended circuitry in terms of devices, devices sizes and interconnects.

(a) On the virtuoso window
Assura → Run LVS



./LVS

gpdk090

Figure Lab5-12 : LVS Window

(b) For LVS with no error, the following report will appear

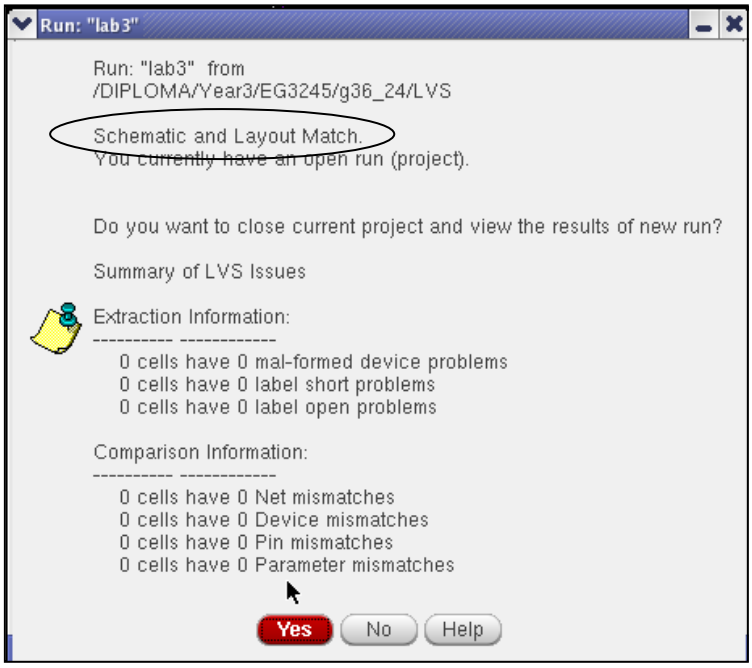


Figure Lab5-13 LVS Run Report

(c) For LVS check with errors, correct all errors in layout and perform checks

(i) Repeat Step 4 -- DRC

(ii) Repeat Step 5 -- LVS

Virtuoso Layout-XL Editor - Routing Basics

(a) How to new a layout
In Library Manager, **File/New/Cellview, Type=Layout, Open with LayoutXL**

(b) Open Layer Palettey:
Window → Assistants → Layer

(c) Draw wire
- (i) Select layer → press **w**
- (ii) Select start point → Move to end point → press **Enter**
- (iii) To change the width of metal while wiring → **F3**
- (iv) **Back Space** to undo wiring

(d) Assisted Routing
Create → Point to Point

(e) To create a geometry:
- (i) From the layout palette, **select** the layer (dra/pin)
- (ii) In the layout window,
  Create → Shape → Rectangle

(f) To measure between distance between two points in design
Press **k.** Click to make measurement. **<Shift>k** to clear rulers.

(g) To clear rulers: Press **<Shift> k**

(h) To move an object: Press **m**

(i) To fit design into display area: Press **f.**
To **Zoom:** Hold the Right-Button (of mouse) and drag.

(j) Stretch Command
Press **s** *select the edge of polygon and **drag**

(k) To view/change properties of an object
- (i) Select object
- (ii) Press **q**

(l) To clear highlighting marker: **Verify→Marker→Delete All, OK.**

(m) To clear interactive DRC check: **Option→DRD Edit → off the 'notify'**

Design Rules For 90nm Technology

Sn	Description	Dimension
1	Minimum POLY width / area	0.1 μm / 0.1μm^2
2	Minimum OXIDE width / area	0.12 μm / 0.06μm^2
3	Minimum MET1 width / area	0.12 μm / 0.07μm^2
4	Minimum MET2 width / area	0.14 μm / 0.08μm^2
5	Fixed CONT size	0.12μm x 0.12μm
6	Fixed VIA size	0.14μm x 0.14μm
7	Minimum MET1 enclosure of CONT	0.06 μm
8	Minimum OXIDE enclosure of CONT	0.06 μm
9	Minimum POLY enclosure of CONT	0.04 μm
10	Minimum IMP enclosure of OXIDE	0.14 μm
11	Minimum IMP enclosure of OXIDE (from GATE)	0.18 μm
12	Minimum NWELL enclosure of OXIDE	0.12 μm
13	Minimum POLY extension of GATE	0.18 μm
14	Minimum OXIDE extension of GATE	0.2 μm
15	Minimum MET1 to MET1 spacing	0.12 μm
16	Minimum MET2 to MET2 spacing	0.14 μm
17	Minimum POLY to POLY spacing	0.12 μm
18	Minimum OXIDE to OXIDE spacing	0.15 μm
19	Minimum GATE to GATE spacing	0.12 μm
20	Minimum CONT to CONT spacing	0.14 μm
21	Minimum VIA to VIA spacing	0.15 μm
22	Minimum IMP to IMP spacing	0.24 μm
23	Minimum NWELL to NWELL spacing	0.6 μm
24	Minimum POLY to DIFF spacing	0.1 μm
25	Minimum GATE to CONT (on OXIDE) spacing	0.1 μm
26	Minimum GATE to CONT (on POLY) spacing	0.12 μm
27	Minimum NIMP to PIMP spacing	0.16 μm
28	Minimum IMP to OXIDE spacing	0.16 μm
29	Minimum NWELL to OXIDE spacing	0.3 μm

Virtuoso Display Settings :

Display Option : Minor :1

Major : 5

X snap spacing : 0.005

Y snap spacing : 0.005

Layout Editor

Aperture : 0.1