Nanyang Polytechnic

School of Engineering

Diploma in Electronics Computer & Communications Engineering (EGDF01)

EXPERIMENT NO	:	Lab 04 (Duration : 4 hours)
EXPERIMENT TITLE	:	Evaluate performance/design parameters of a 2-input CMOS NOR and OR Gate
OBJECTIVE	:	To study the effect of design parameters on the timing performance of a : a. CMOS NOR gate b. CMOS OR gate using hierarchy approach

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Exercise 1 : Build a CMOS NOR Gate

1. Capture a CMOS NOR gate schematic with the following component parameters:-
   (a) **PMOS** of NOR gate : Finger Width=Wp1, L=100n
   (b) **NMOS** of NOR gate : Finger Width=Wn1 and L=100n
   (c) **vdd** and **vss** as pins with direction=**InputOutput**.

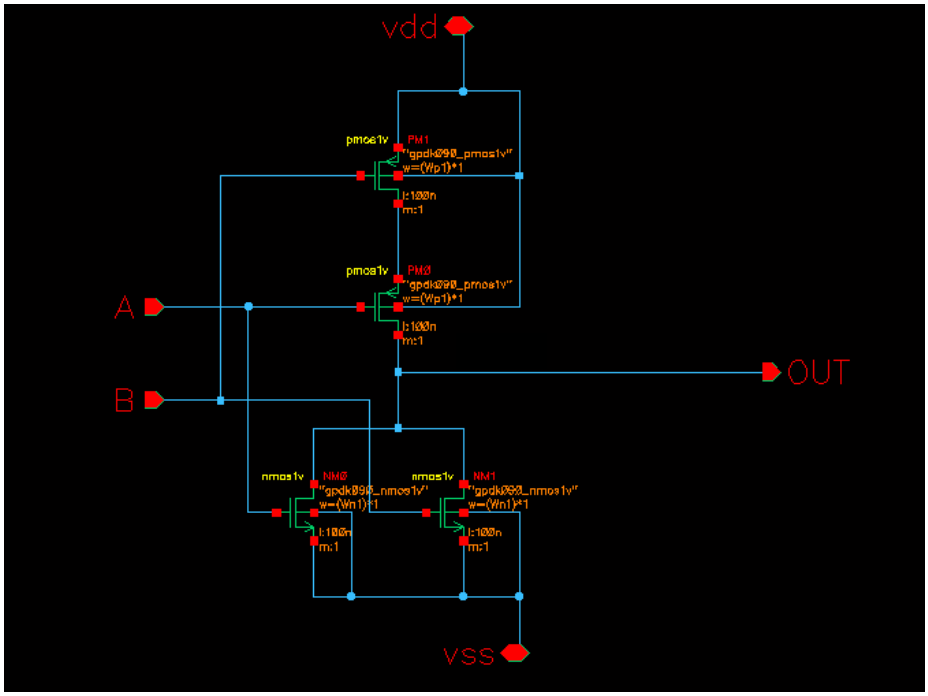

Figure Lab4-1 : 2 Input CMOS NOR Gate

2. Create a symbol for the NOR circuit of Figure Lab4-1.

3. Capture the simulation circuit shown in Figure Lab4-2.

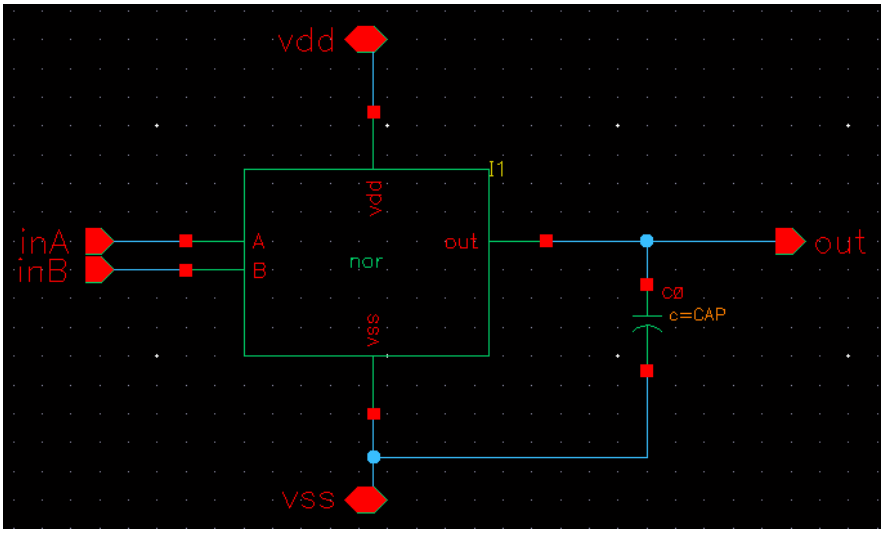

Figure Lab4-2 : NOR Gate Simulation Circuit

4. Simulate the circuit with the following **stimuli** settings:
   (a) *inA* : Pulse (0 to 1.2 V), period 15n s, 50% duty cycle
   inB : Pulse (0 to 1.2 V), period 30n s, pulse width 15n s

   (b) set ***analyses*** to tran and *stop time* to **2 times the slower period**

   (c) edit ***variable*** *CAP* to 40f
   Wp1 = 120n
   Wn1 = 120n

   (d) plot ***outputs*** → ***inA, inB*** and ***Out***

   (e) run **Simulation → Netlist & Run**

5. (a) Measure High to Low delay and Low to High delay from ***inA*** to ***Out***.

   (b) Measure the rise time and fall time of ***Out***.

6. Modify the transistor size(s) of the NOR gate to obtain as symmetrical a rise and fall time.

Exercise 2 : Build a CMOS OR Gate, using hierarchical approach (**to be used for Lab 6**)

1. Create an OR gate by instantiating the symbols of the NOR gate and the inverter, as shown in Figure Lab4-3.

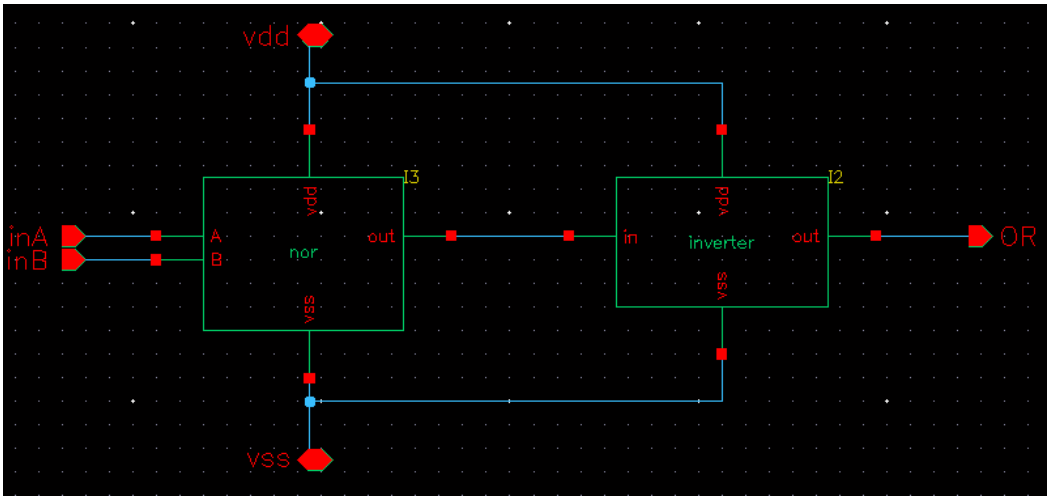

Figure Lab4-3 : A CMOS OR Gate

2. Create a simulation circuit as shown in Figure Lab4-4, to verify the functionality of the OR gate.

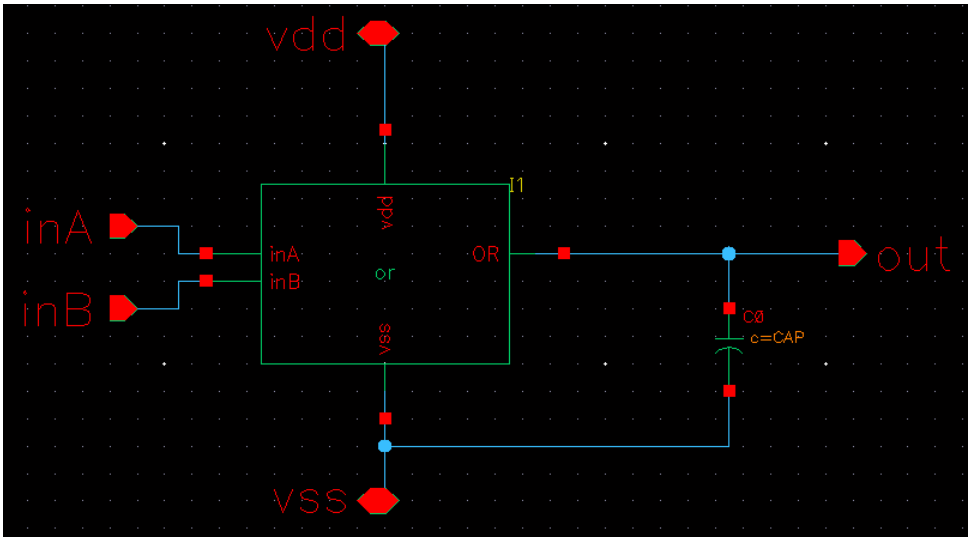

Figure Lab4-4 : OR gate simulation circuit

3. Repeat Exercise 1 - Step 4 to perform the verification with :
   CAP = 40f
   Wn1 = 120n (NMOS width of NOR)
   Wp1 = 120n (PMOS width of NOR)
   and Wp = 120n (PMOS width of inverter)

4. Verify that the functionality of OR gate is correct.

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Submission of Lab4:

Submission

12. With reference to Exercise 1 - Step 5(b),
    (a) is the rise time longer than the fall time ?
    (b) what is the ratio of rise time to fall time ?
    (c) is the ratio obtained in 12(b) agreeable with the theory ? Explain your answer. (Hint : Use series and parallel concepts)

13. With reference to Exercise 1 - Step 6,
    (a) Explain why the rise time should be adjusted to match the fall time and not otherwise.
    (b) Record the sizes of the p-transistors. What is the ratio of the p-transistors to n-transistors? Does it agree with the theory, explain ?

14. With reference to Exercise 2 – Step 4, explain how you verify that the functionality of OR gate is correct.