Nanyang Polytechnic

School of Engineering

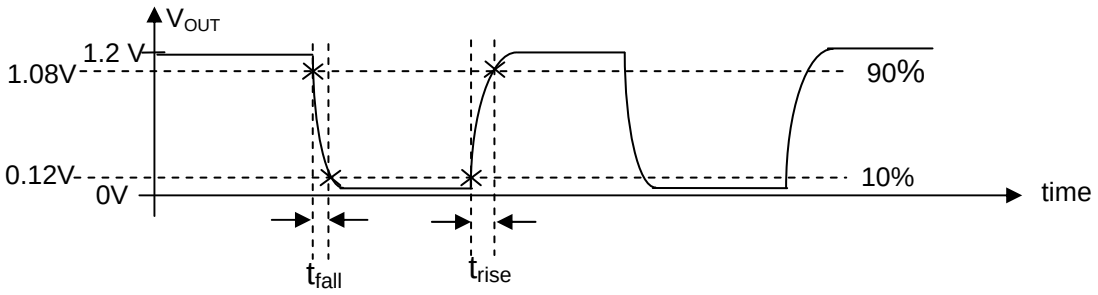
Diploma in Electronics Computer & Communications Engineering (EGDF01)

EXPERIMENT NO	:	Lab 03 (Duration : 4 hours)
EXPERIMENT TITLE	:	Evaluate performance/design parameters of a CMOS Inverter
OBJECTIVE	:	To study the rise and fall time of CMOS inverter due to (a) effect of load capacitance (b) effect of geometrical size of PMOS vs NMOS

Rise and Fall Time Measurements

Rise Time (t_{rise})
- time taken for $\mathbf{V_{OUT}}$ to rise from 10% to 90% of its final value.

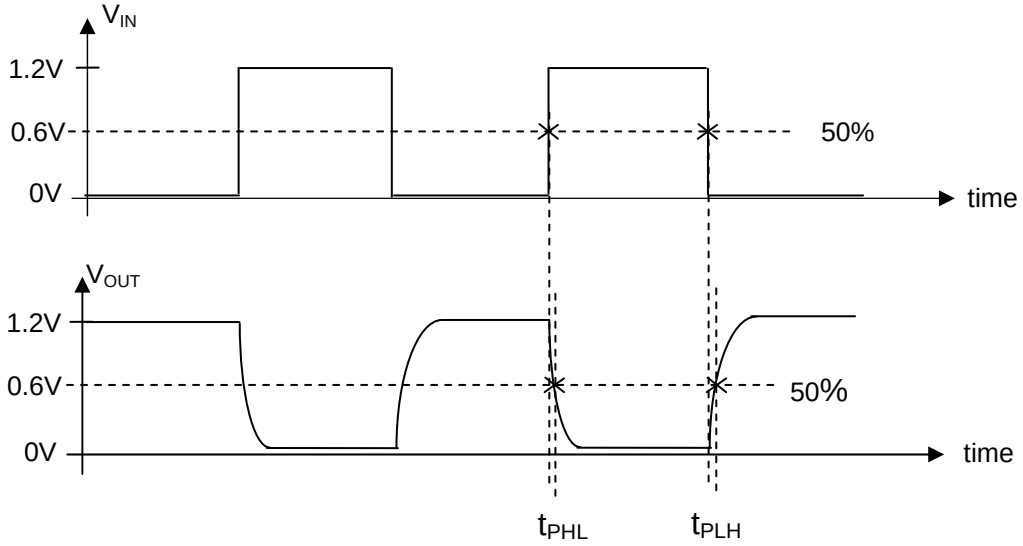
Fall Time (t_{fall})
- time taken for $\mathbf{V_{OUT}}$ to fall from 90% to 10% of its final value.



Propagation Delay Measurements

Delay Time (t_{pHL}) $\mathbf{V_{OUT}}$ going from *High* to *Low*
- measured wrt the V_{IN} edge responsible for the transition

Delay Time (t_{pLH}) $\mathbf{V_{OUT}}$ going from *Low to High*
- measured wrt the V_{IN} edge responsible for the transition



1. Capture a CMOS Inverter schematic with the following component parameters:-
   (a) **PMOS** : Finger Width=Wp and Length=100n (use pmos1v from gpdk090)
   (b) **NMOS** : Finger Width=120n and Length=100n (use nmos1v from gpdk090)

   (c) **vdd** and **vss** as pins with direction=**InputOutput**
   (*Note : **vdd** and **vss** are the power supplies. For* gpdk090 library, they *have a value of 1.2V and 0V respectively*)

   (d) **in** as pin with direction=**Input**
   (e) **out** as pin with direction=**Output**

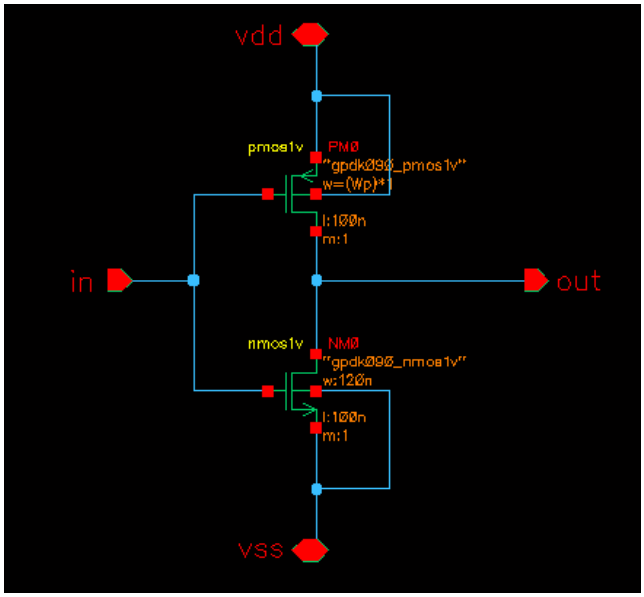


Figure Lab3-1 : CMOS Inverter schematic

2. Symbol Creation
   Create a symbol for Figure Lab3-1 with ***vss*** at the **bottom** of the symbol.

3. Built Simulation Circuit
   Open a new schematic window and capture the simulation circuit as shown in Figure Lab3-2.

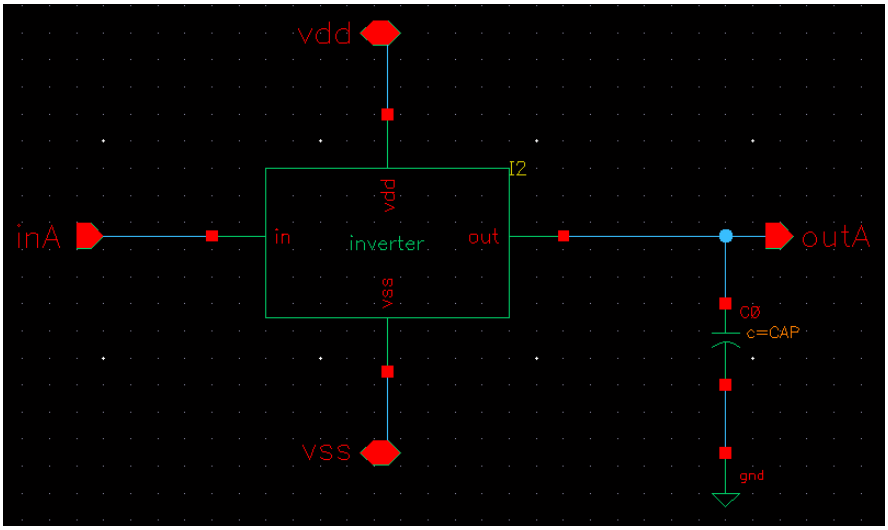


Figure Lab3-2 : Simulation Circuit

4. Circuit Simulation

Verify the performance of the inverter created in Figure Lab3-1 using the simulation circuit built in Lab3-2.

(a) Setup stimuli as follows :
set *inA* to **pulse** with *Pulse width*=20n and *Period*=40n
Voltage1 = 0 and *Voltage2* = 1.2

set *vdd* to **DC** 1.2
set *vss* to **DC** 0

(b) Set ***analyses*** to ***tran*** and ***stop time*** to 80n (2 times of period)

(c) Edit ***variable*** *CAP* to 0.04p
Wp to 120n

(d) Plot ***outputs*** (waveforms) of ***outA*** and ***inA***

(e) Run ***simulation***
Ensure that *outA* is the **invert** of *inA*. (Behavior of an inverter).

5. To study the effect of the capacitor, *CAP,* on circuit performance

(a) Assign a range of values to ***variable*** *CAP* as follows :
Tools → Parametric Analysis

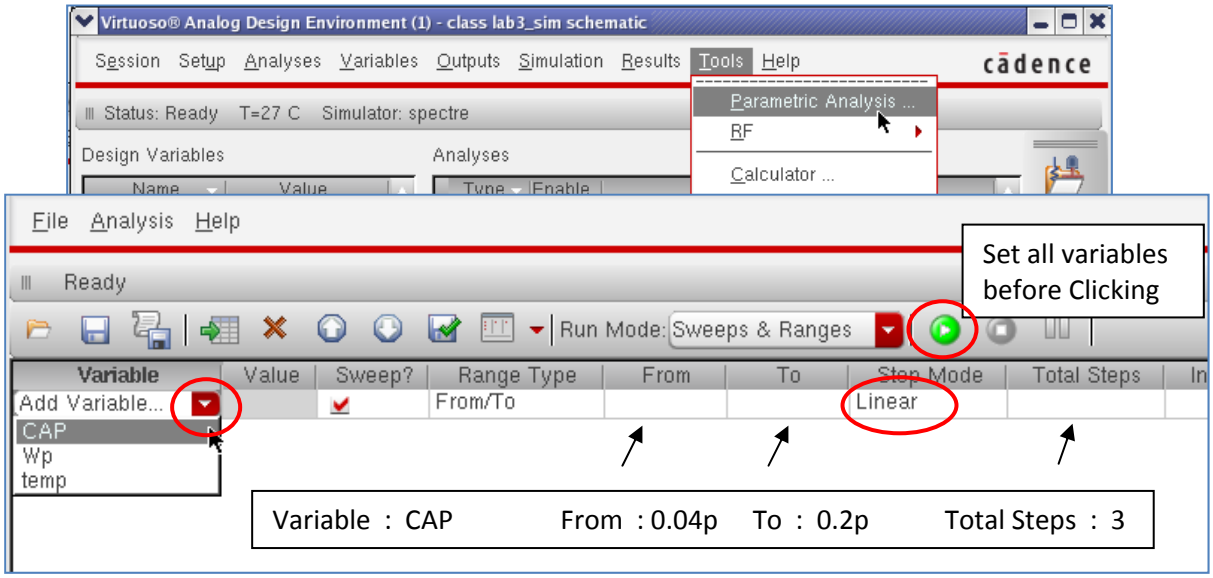


Figure Lab3-3 : Parametric Analysis

(b) Measure the **rise time (t_{rise})**, of ***outA*** *for* ***CAP=0.2p***

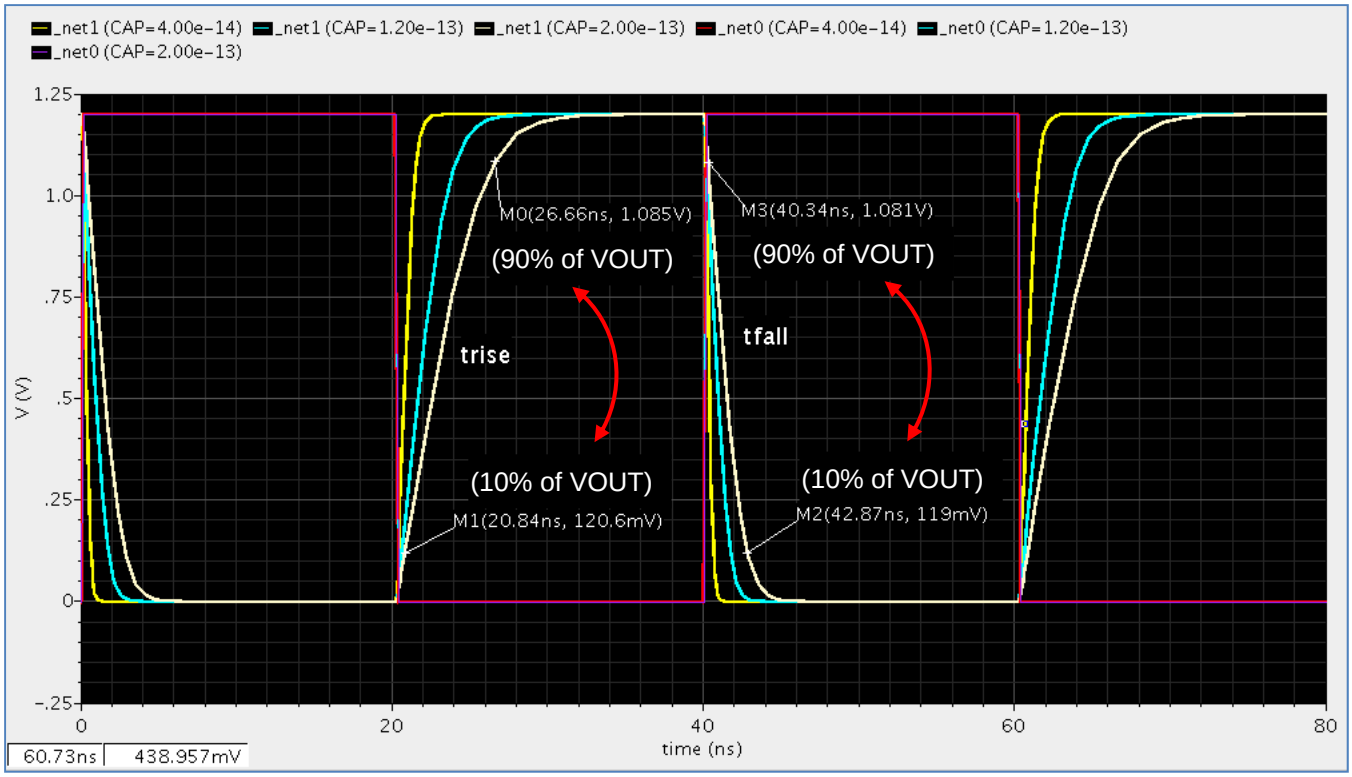


Figure Lab3-4 : t_{rise} & t_{fall} - Wp = 120n, Cap = 0.04p to 0.2p

In the Waveform Window
Marker -> Create_ Marker-->Point --> OK
Move the marker to output at y=120m V (10% of V_{OUT})

Marker -> Create_ Marker-->Point --> OK
Move the marker to output at y=1.08 V (90% of V_{OUT})

Calculate and record in Table 1, the rise time by taking the difference between the 2 measured values.

(c) Using the same method as Step 5(b), measure the **fall time** (t_{fall}) of ***outA***.

(d) **Print the waveforms**, as shown in Figure Lab3-4, with all markers attached.

(e) Measure and record the **High to Low delay (t_{pHL})** from ***inA*** to ***outA***.

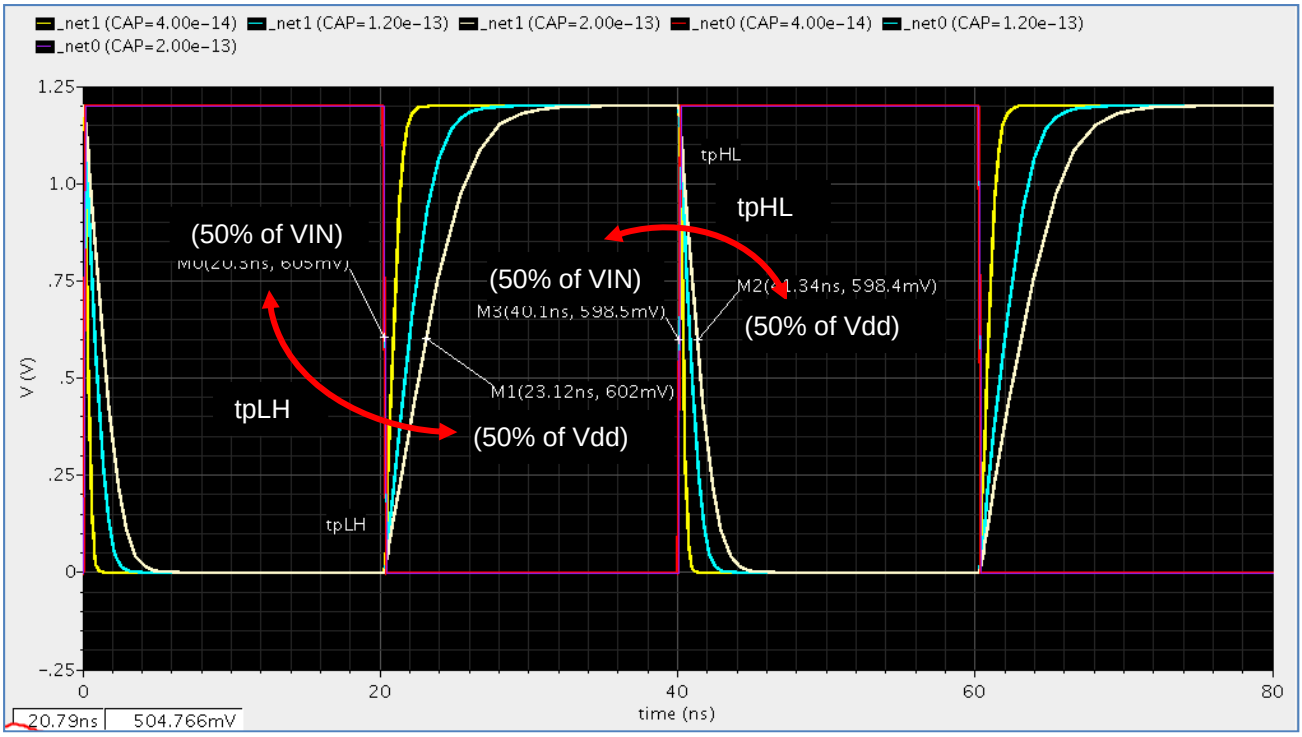


Figure Lab3-5 : tpHL & tpLH - Wp = 120n, Cap = 0.04p to 0.2p

In the Waveform Window
Marker -> Create_ Marker-->Point --> OK
Move the marker to input at y=0.6 V (50% of V_{OUT})

Marker -> Create_ Marker-->Point --> OK
Move the marker to output at y=0.6 V (50% of V_{OUT})

Calculate and record in Table 1, the t_{pHL} by taking the difference between the 2 measured values.

(f) Measure and record the **Low to High delay (t_{pLH})** from ***inA*** to ***outA***.

(g) Repeat Step 5(b) to 5(f) to obtain the timings of ***outA*** for ***CAP=0.04p***.
No printing of waveform is required.

6. To study the effect of the width of the p-transistor, Wp, on circuit performance

(a) Assign a range of values to ***variable*** Wp as per Step 5(a) with settings as follows :

Variable Name : Wp

From : 120n To : 420n

Total Steps : 3

(b) Measure the $\mathbf{t_{rise}}$ and $\mathbf{t_{fall}}$ of ***outA*** for Wp = 120n and Wp=420n.

(c) Measure the $\mathbf{t_{pLH}}$ and $\mathbf{t_{pHL}}$ of ***outA*** with reference to **inA** for Wp = 120n and Wp=420n.

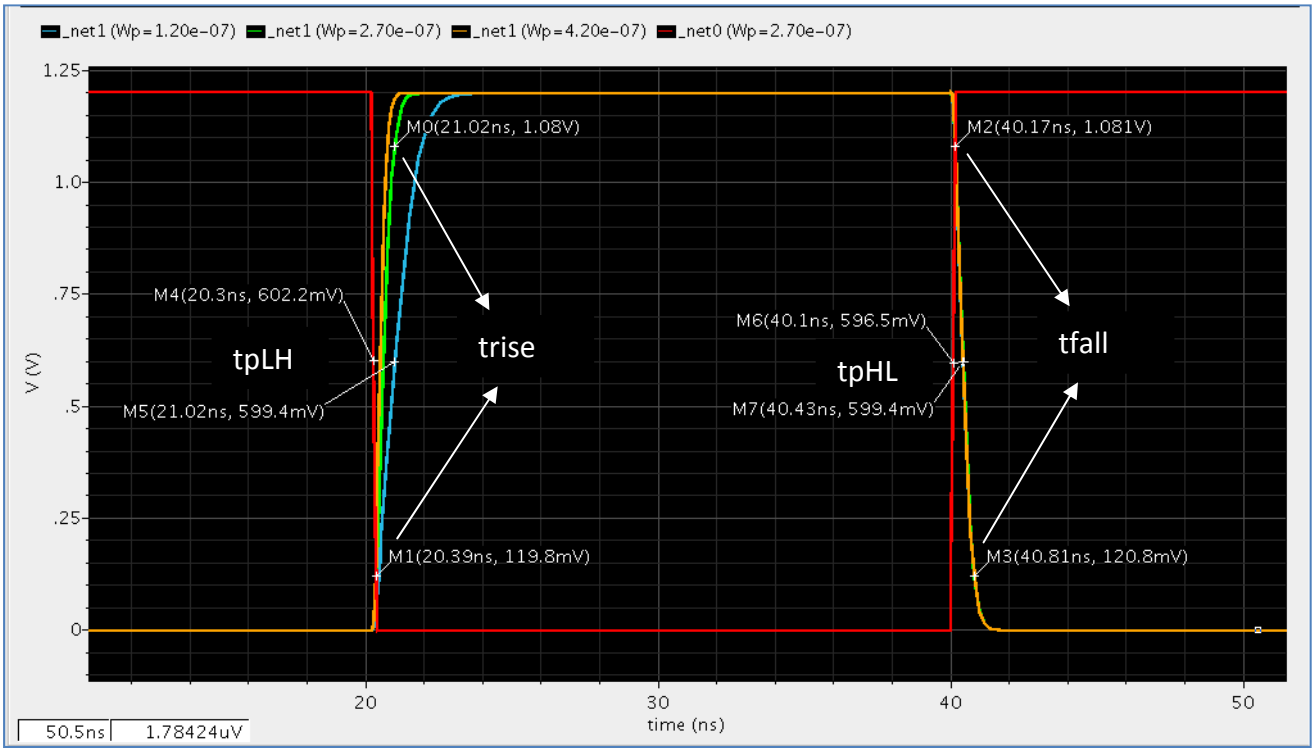


Figure Lab3-6 : CAP = 0.04p, Wp = 120n to 420n

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Submission of Lab3:

1. Submit the waveforms obtained in Step 5.

2. Tabulation of results obtained in Step 5 & Step 6:-

	Step 5		**Step 6**		
	Wp=120n M		CAP = 0.04p F		
	CAP = 0.04p F	CAP = 0.2p F	Wp = 120n M	Wp = 420n M	Wp = 270n M
t_{rise}					
t_{fall}					
$t_{rise} : t_{fall}$					
t_{pLH}					
t_{pHL}					
$t_{pLH} : t_{pHL}$					

Table 1

3. From Table 1 – Step 5, comment on how the change in capacitive load affects timing performance. Use relevant equations to substantiate your answer.

4. From Table 1 – Step 6, comment on how the change in W_p affects timing performance. Use relevant equations to substantiate your answer.

5. What is the width (W_n) of the NMOS transistor in this circuit ? From Table 1, compare the t_{pLH} and t_{pHL} obtained for W_p=W_n. Since W_p=W_n, explain why the difference in timing? (Hint : mobility).

6. From the waveforms obtained in Figure Lab3-6 (or from Table 1), determine which W_p results in approximately the same t_{pLH} and t_{pHL}.
   (i) Calculate the t_{pLH} using the W_p obtained.
   (ii) Calculate the t_{pHL} using the W_n of the circuit.
   (iii) What is the ratio of $t_{pLH} : t_{pHL}$?
   (iv) Is the theoretical ratio and the ratio obtained from the lab exercise agreeable ?

7. What impact does modifying the *length* of a transistor have on the response time ? What impact does modifying the *width* of a transistor have on the response time ?

8. Is it compulsory to make the rise and fall time the same? That is, is ratio compulsory?