

## School of Engineering

# Diploma in Electronics Computer & Communications Engineering (EGDF01)

| EXPERIMENT NO    | : | Lab 02 (Duration : 2 hours)                                    |
|------------------|---|--|
| EXPERIMENT TITLE | : | To study NMOS Transistor as a Switch                           |
| OBJECTIVE        | : | To study the characteristics of an NMOS transistor as a switch |

- 1. Capture a schematic diagram
  - (a) With reference to Step 1(b) to 1(g), launch a new *schematic* window to capture the circuit (nswitch) of Figure Lab2-1.



Figure Lab2-1 : NMOS Switches

(b) Add NMOS transistor *Create* → *Instance* 

| 6          |              |                        |                 |         |
|------------|--------------|------------------------|-----------------|---------|
| Add Ins    | tance        |                        |                 |         |
| Library    | gpdk090      | Browse                 | Library         | apdk090 |
| Cell       | nmos1v       |                        | Cell            | nmos1v  |
| View       | symbol       |                        | View            | symbol  |
| Names      |              |                        |                 | ,       |
| Array      | Rows         | 1 Columns 1            |                 |         |
|            | 🕰 Rotate 📄 🕼 | Sideways 🕞 Upside Down |                 |         |
|            |              |                        |                 |         |
| Model Na   | ume          | gpdk090_nmos1v         |                 |         |
| Multiplier |              | 1                      | l an aith       | 100m M  |
| Length     |              | 100n M                 | Length          |         |
| Total Widf | th           | 120n M                 | Einger Width    | Wn M    |
| Finger Wi  | dth          | Wh M                   | i iligei wiatti |         |
| Fingers    |              | 1                      |                 |         |
| Threshold  | I            | 120n M                 |                 |         |
| Apply Thr  | reshold      | <u> </u>               |                 |         |
| Gate Con   | nection      | None                   |                 |         |
| Lise DEM   | Bules        | Minimum 🚽              |                 |         |

Figure Lab2-2 : Add NMOS Transistor

(c) *Click* on the schematic window to place component; press *ESC* to cancel command.

## (d) Add pin

| Create         | e → Pin          |               |                  |              |               |
|----------------|------------------|---------------|------------------|--------------|---------------|
| 🗙 Add Pin      |                  |               |                  |              |               |
| Pin Names      | vss              |               |                  | Pin Names    | VSS           |
| Direction      | inputOutput      | Bus Expansion | 💩 off 🥥 on       | Direction    |               |
| Usage          | schematic 🔽      | Placement     | 🧕 single 🧅 mult  | iple         | InputOutput   |
| Attach Net Exp | iression: 🛛 🖲 No | 🥥 Yes         |                  | Attach Net I | Expression No |
| Property Name  |                  |               |                  |              |               |
| Default Net Na | me               |               |                  |              |               |
| Font Height    | 0.0625           | Font Style    | stick            |              |               |
| 🕼 Rotate       |                  | 🗧 Upside Down | Show Sensitivity | / >>         |               |
|                |                  | (Hide) Canc   | el Defaults H    | Help         |               |

Figure Lab2-3 : Add Pin

- (e) Add pin *input, nmos1, nmos2* -- direction *input* Add pin *01nmos, 02nmos* -- direction *output*
- (f) **Click** on the schematic window to place the pin; press **ESC** to cancel command.
- (g) Wire up the circuit as shown in Figure Lab2-1.
   Create → Wire (narrow)
- (g) Check and Save Design File → Check & Save

- 2. Create a symbol
  - (a) With reference to Step 2(b) to 2(c), create a symbol for the circuit captured in Step 1 (Figure Lab2-1). From the *schematic window*,



Create  $\rightarrow$  Cellview  $\rightarrow$  From Cellview

Figure Lab2-4 : Steps to create symbol

(b) Accept all default values in the pop-up windows

|                  |                   | Cellview From Cell | view      |             |                 | _ D X         |          |          |    |
|------------------|-------------------|--------------------|-----------|-------------|-----------------|---------------|----------|----------|----|
|                  |                   | Library Name       | class     |             |                 | Browse        |          |          |    |
|                  |                   | Cell Name          | lab2      |             |                 |               |          |          |    |
|                  |                   | From View Name     | schematic |             |                 |               |          |          |    |
|                  |                   | To View Name       | symbol    | )           |                 |               |          |          |    |
| Y Symbol Genera  | ation Options     |                    |           |             | _ ×             |               |          |          |    |
| Library Name     |                   | Cell Name          |           | View Name   |                 |               |          |          |    |
| class            | ]                 | lab2               |           | symbol      | ]               |               |          |          |    |
| Pin Specificatio | ons               |                    |           |             | A divile ut e e |               |          |          |    |
| Left Pins        | input nmos1 nm    | os2                |           |             |                 |               |          |          |    |
| Right Pins       | Olomos Olomos     |                    |           |             |                 |               | [@instai | nceName] | J. |
|                  |                   |                    |           |             |                 |               |          |          |    |
| Top Pins         |                   |                    |           |             |                 | [@a.a.th]amal |          |          |    |
| Bottom Pin       | vss               |                    |           |             |                 | [@partivame]  |          |          |    |
| Exclude Inherit  | ed Connection Pin | 3:                 |           |             |                 |               |          |          |    |
| 💌 None 😀         | All 😄 Only these  | :                  |           |             |                 |               |          |          |    |
| 0                |                   |                    |           |             |                 |               |          |          |    |
| Load/Save 📃      | Edit Attrib       | utes 📃 Edit L      | abels 📃   | Edit Prop   | er 💶            |               |          |          |    |
|                  |                   |                    | ОК        | Cancel Appl | у               |               | <br>     |          |    |

Figure Lab2-5 : Symbol Creation

(c) From the symbol window
File → Check & Save
File → Close

- 3. Create a simulation circuit
  - (a) Start another new schematic window and capture the simulation circuit (nswitch\_sim) shown in Figure Lab2-6.



Figure Lab2-6 : Simulation Circuit

(b) Instantiate the symbol obtained in Step 2.
 Create → Instance

| class<br>(name used in step<br>symbol | 1)   |
|---------------------------------------|--|
| Symbol                                |  |
|                                       | class<br><i>(name used in step</i><br>symbol |

(c) Add load capacitors Create → Instance

**analogLib** cap symbol

Capacitance CAP F Initial condition 0 ∨

- (d) Repeat (c) for the other capacitor
- (e) Repeat (c) to instantiate *gnd* from *analogLib* library.
- (f) Complete the connections of the circuit shown in Figure Lab2-6.
- (g) File  $\rightarrow$  Check & Save

### 4. Simulate the Circuit

- (a) Launch Analog Design Environment for simulation Launch  $\rightarrow$  ADE L
- (b) Setup the stimulus
   Setup → Stimuli
   set nmos1 to DC 1.2 (Volts)

| J <u>e</u> ssion Set <u>up An</u> alyses <u>V</u> | <u>/ariables O</u> utputs <u>S</u> imulation <u>R</u> esu | lts <u>T</u> ools <u>H</u> elp <b>cāde</b> | n c e |
|---|---|--|-------|
| Status: F Design<br>Simulator/Directo             | nrv/Host  |  |       |
| esign Va Tur <u>b</u> o/Parasitic F               | Reduction Ivses   |  | L.    |
| Name <u>M</u> odel Libraries                      | /pe -  Enable   | Arguments                                  |       |
| Stim <u>u</u> li                                  | ✓ Setup Analog Stimuli                                    |  | . X   |
| Simulation <u>F</u> iles                          | Stimulus Type   | Global Sources                             |       |
| MATLAB/Simulir<br>Environment                     |   |  | -     |
|   | 1 : Select the  | desired signal                             |       |
|   | OFF (nmos1)/gnd! Voltag                                   | e bit                                      |       |
|   | OFF input /gnd! Voltag                                    | e bit<br>e bit                             |       |
|   |   |  |       |
|   |   | 3 : Select                                 |       |
| <u>&lt; (</u>                                     | 2 : Enable /  | Function                                   |       |
| ><br>Stimuli                                      |   |  | =     |
| Sundi   | Enabled 🗹 🛛 Function                                      | dc Type Voltage                            |       |
|   | DC voltage  | 1.2 4. Update Settings                     |       |
|   | AC magnitude  |  |       |
|   | AC phase  |  |       |
|   | XF magnitude  |  |       |
|   | PAC magnitude   |  |       |
|   | PAC phase   |  | 9     |
|   | Temperature coefficient 1                                 |  |       |
|   | Temperature coefficient 2                                 |  |       |
|   | Nominal temperature                                       |  |       |
|   | Source type   | de   |       |
|   | Noise file name   |  |       |
|   | Number of poice/free poice                                | 0  |       |
|   |   |  |       |
|   | Freq  |  |       |
|   | NOISE 1   |  |       |
|   | Fred 2  |  |       |

Figure Lab2-7: Setup Stimulus

- (c) Click **Apply** to accept the settings of each signal.
- (d) Continue to stimuli setup for the following :-
  - (i) set *nmos2* to **DC** 1.2

(ii) set *input* to **pulse** with *Pulse width* = 20n, *Period* = 40n,*Voltage1* = 0 and *Voltage2* = 1.2



Figure Lab2-8 : Pulse Definition



- (e) Click **OK** when all signals have been setup.
- (f) Setup the analysis to perform
   Analysis → Choose → tran
   set Stop Time to 80n (2 times of period)

| ❤ Virtuoso® Analog Design Envi                                   | ronment (1) - class lab1 schem   | atic   |   | - O X             |
|--|--|--|---|-------------------|
| S <u>e</u> ssion Set <u>u</u> t <u>A</u> nalyses                 | ariables <u>O</u> utputs <u>S</u> imulat   | ion <u>R</u> esults <u>T</u> ools <u>I</u>   | <u>H</u> elp  | cādence           |
| III Status: Ready<br>Design Variables<br>Name Disable<br>Disable | Analysis<br>Choosing Analyses Virt<br>Analysis<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran<br>Tran | uoso® Analog Design Er<br>dc dc ac<br>sens dcmatch<br>sp envlp<br>pstb pnoise<br>qpss qpac<br>qpsp hb<br>fransient Analysis<br>preset) | nvironment (3) 👝 🗙<br>C noise<br>C stb<br>C pss<br>C pxf<br>C qpnoise<br>C hbac | AC<br>OC<br>Trans |

Figure Lab2-9 : Setup Analysis

(g) Assign values to the variables used in the circuit Variable → Edit → Copy from set CAP to 0.05p set Wn to 120n



Figure Lab2-10 : Edit Variables

- (h) Select signals to be monitored (plotted) graphically
   Outputs → To Be Plotted → Select from Schematic
   Select the wire of input, 01nmos and 02nmos
  - Note : By clicking on the *wire*, the voltage of this wire wrt gnd is being monitored.

Press **ESC** (to avoid toggling effect of unselecting the desired signals)

(j) Run Simulation Simulation → Netlist and Run Account Number: g4[ ]\_[ ]

Name:\_\_\_\_

#### Submission of Lab2:

- 5. What are the functions of the NMOS transistors *in this circuit ?*
- 6. How does I3 (Figure Lab2-1) affects the voltage of 01nmos?
- 7. Measure the voltage level at *01nmos* and *02nmos*. Explain the difference in voltage between the 2 voltages.

In the Waveform Window

- (a) *Marker* → *Create\_Marker* → *Point* → *OK*, then drag the marker to the desired location.
- (b) Place cursor at the highest point of 01nmos and 02nmos.

8. To simulate the circuit with a new set of values

From Analog Environment Window

- (a) **Variable**  $\rightarrow$  Edit  $\rightarrow$  Wn  $\rightarrow$  300n (change the width of the transistor)
- (b) **Simulation**  $\rightarrow$  **Run** (rerun with the new settings)
- 9. What is the effect of changing the width of the N-pass transistors on the voltage of *O1nmos and O2nmos* ? Substantiate your answer with relevant equations.