Nanyang Polytechnic

School of Engineering

Diploma in Electronics Computer & Communications Engineering (EGDF01)

EXPERIMENT NO   :   Lab 02 (Duration : 2 hours)

EXPERIMENT TITLE   :   To study NMOS Transistor as a Switch

OBJECTIVE   :   To study the characteristics of an NMOS transistor as a switch

---

1.   Capture a schematic diagram

(a)   With reference to Step 1(b) to 1(g), launch a new **schematic** window to capture the circuit (nswitch) of Figure Lab2-1.
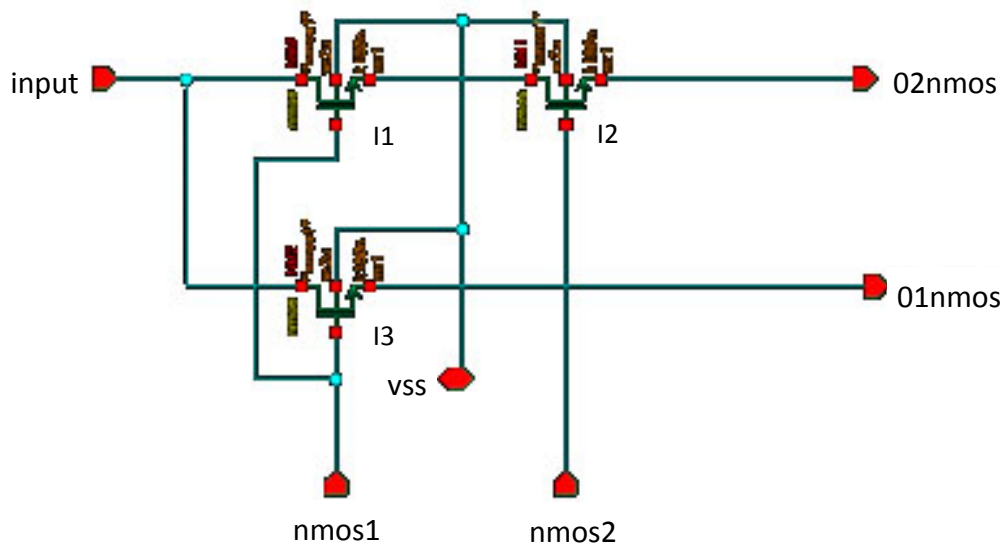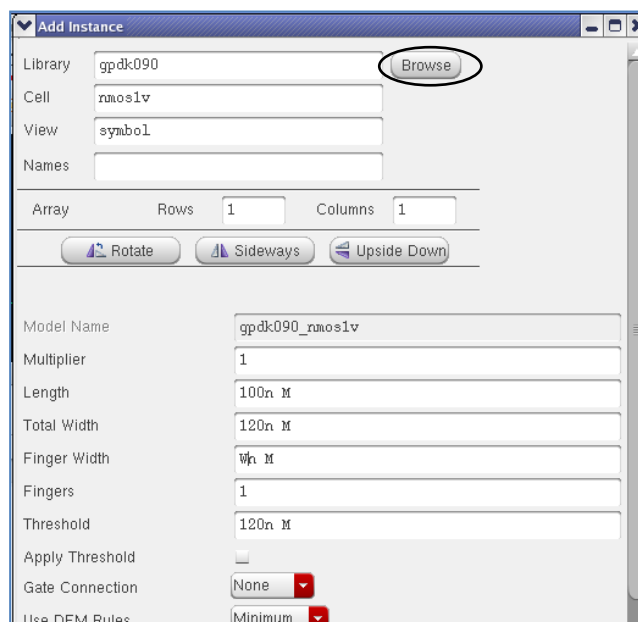

Figure Lab2-1 : NMOS Switches

(b)   Add NMOS transistor
       Create → Instance

Library	**gpdk090**
Cell	nmos1v
View	symbol
Length	100n M
Finger Width	Wn M

Figure Lab2-2 : Add NMOS Transistor

(c)   **Click** on the schematic window to place component; press **ESC** to cancel command.

(d)   Add pin
       Create → Pin

Pin Names   vss

Direction   inputOutput

Attach Net Expression   No

Figure Lab2-3 : Add Pin

(e)   Add pin *input, nmos1, nmos2* -- direction *input*
       Add pin *01nmos, 02nmos* -- direction *output*

(f)   *Click* on the schematic window to place the pin; press *ESC* to cancel
       command.

(g)   Wire up the circuit as shown in Figure Lab2-1.
       Create → Wire (narrow)

(g)   Check and Save Design
       File → Check & Save

2. Create a symbol

   (a) With reference to Step 2(b) to 2(c), create a symbol for the circuit captured in Step 1 (Figure Lab2-1). From the *schematic* window,
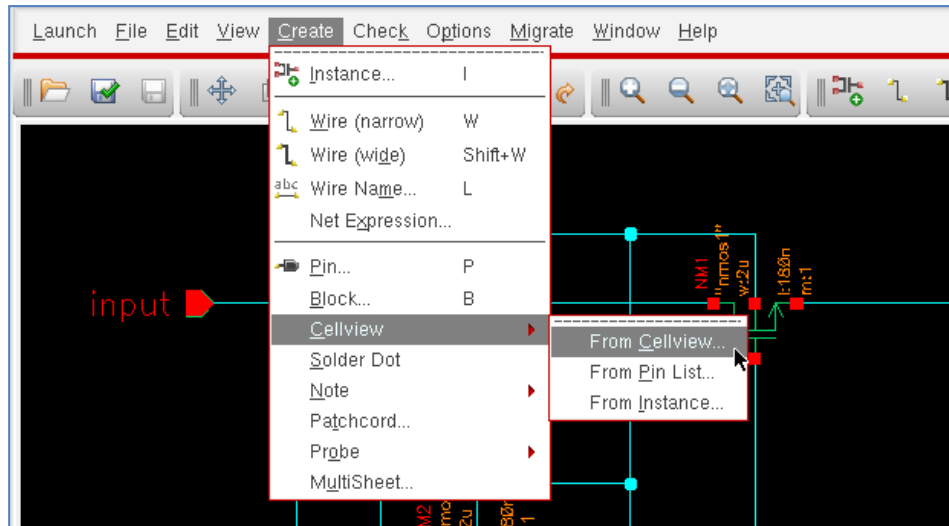
   Create → Cellview → From Cellview

Figure Lab2-4 : Steps to create symbol

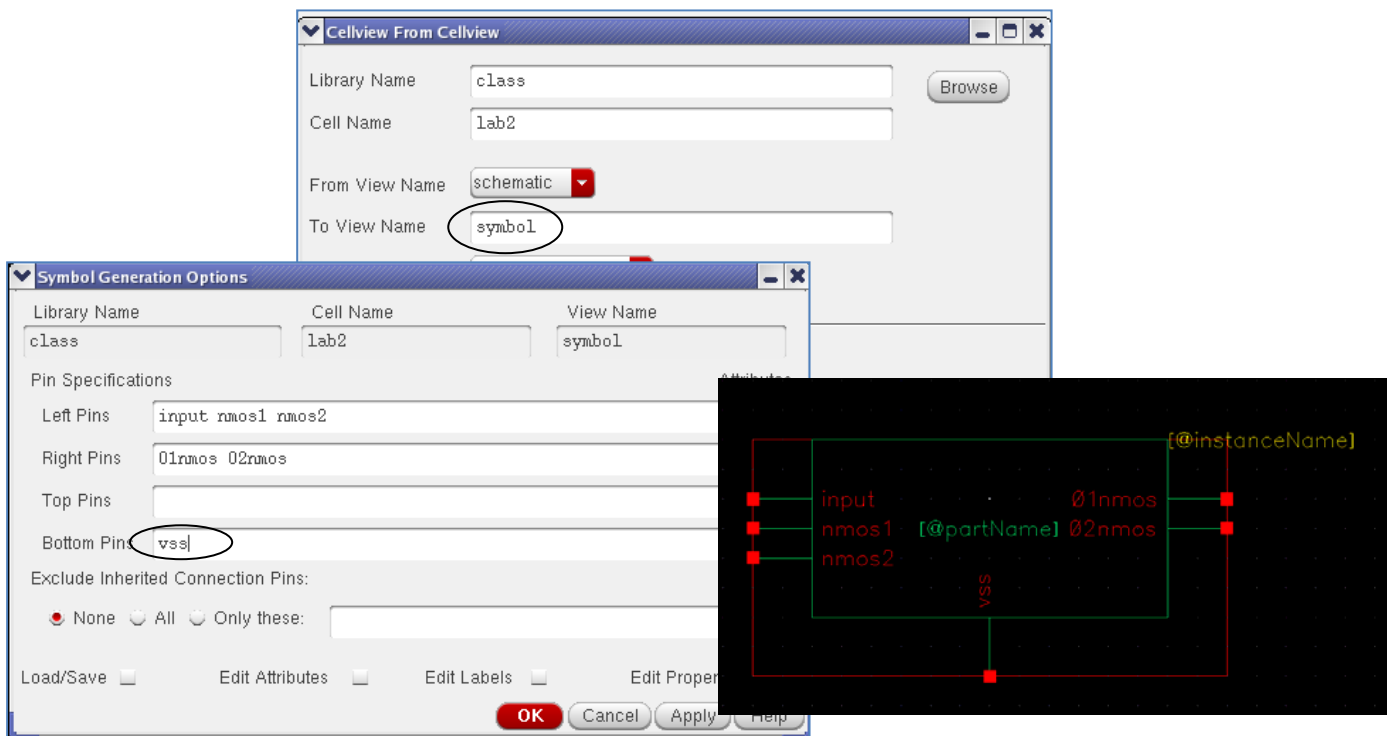   (b) Accept all default values in the pop-up windows

Figure Lab2-5 : Symbol Creation

   (c) From the *symbol* window
       File → Check & Save
       File → Close

3.   Create a simulation circuit

(a) Start another new schematic window and capture the simulation circuit (nswitch_sim) shown in Figure Lab2-6.
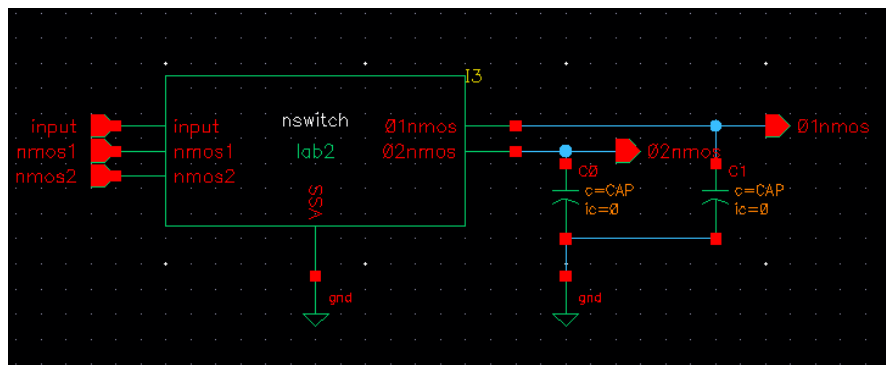

Figure Lab2-6 : Simulation Circuit

(b)   Instantiate the symbol obtained in Step 2.
       Create → Instance

Library	class
Cell	*(name used in step 1)*
View	symbol

(c)   Add load capacitors
       Create → Instance

Library	**analogLib**
Cell	cap
View	symbol
Capacitance	**CAP** F
Initial condition	**0** V

(d)   Repeat (c) for *the other capacitor*

(e)   Repeat (c) to instantiate **gnd** from **analogLib** library.

(f)   Complete the connections of the circuit shown in Figure Lab2-6.

(g)   **File → Check & Save**

4.   Simulate the Circuit

(a)   Launch Analog Design Environment for simulation
       Launch → ADE L

(b)   Setup the stimulus
       Setup → Stimuli
       set **nmos1** to **DC** 1.2 (Volts)
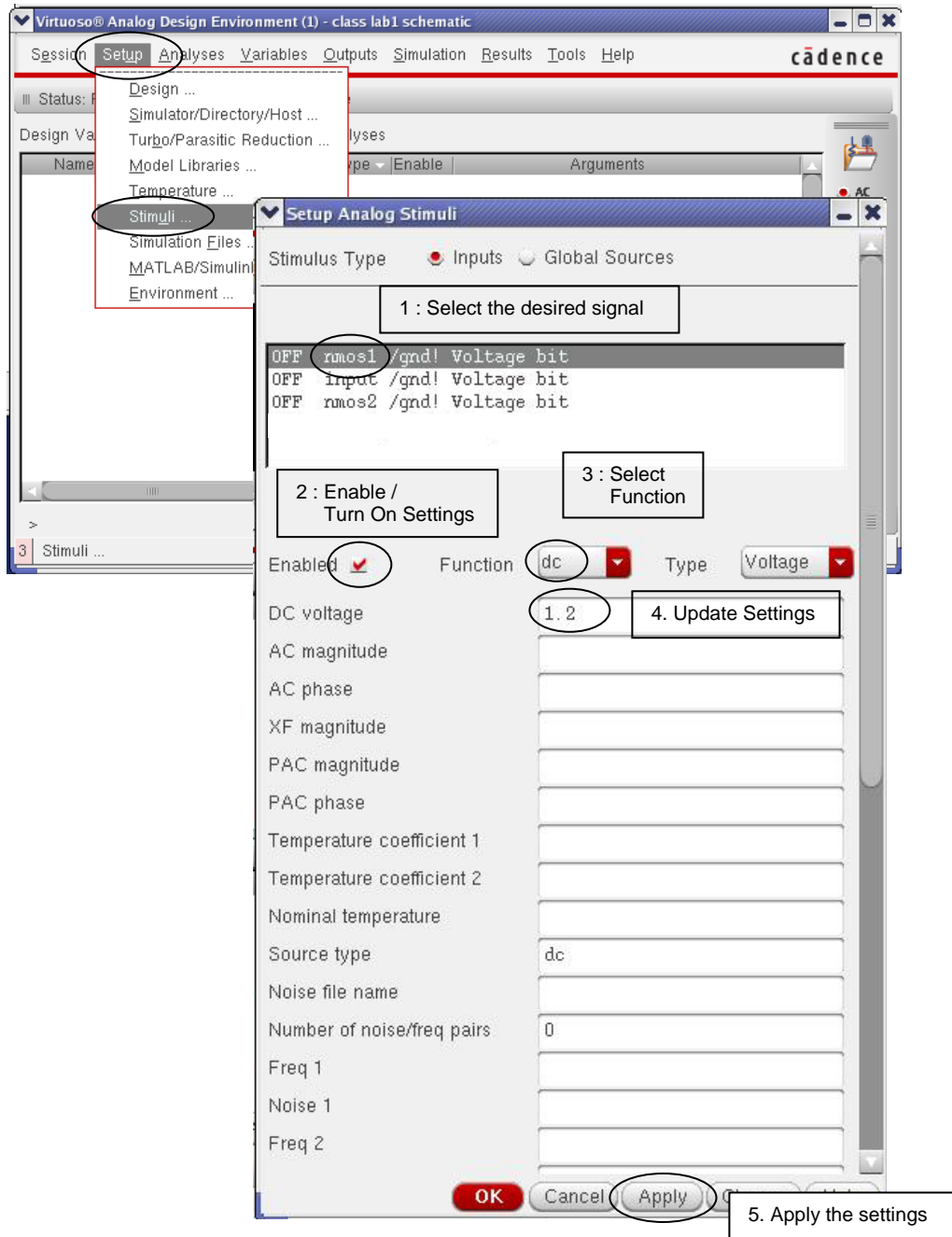
Figure Lab2-7: Setup Stimulus

(c)   Click **Apply** to accept the settings of each signal.

(d)   Continue to stimuli setup for the following :-
     (i)   set *nmos2* to **DC** 1.2

(ii)   set **input** to **pulse** with *Pulse width* = 20n, *Period* = 40n,
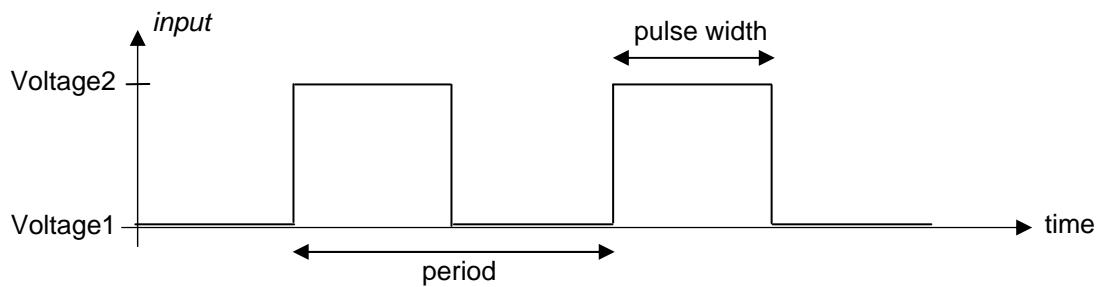   *Voltage1* = 0 and *Voltage2* = 1.2

Figure Lab2-8 : Pulse Definition

$$f = \frac{1}{T} \ (Hz) \qquad \text{where T = period (in seconds)}$$

$$duty \ cycle = \frac{pulse \ width}{period} * 100\%$$

(e)   Click **OK** when all signals have been setup.

(f)   Setup the analysis to perform
         Analysis → Choose → tran
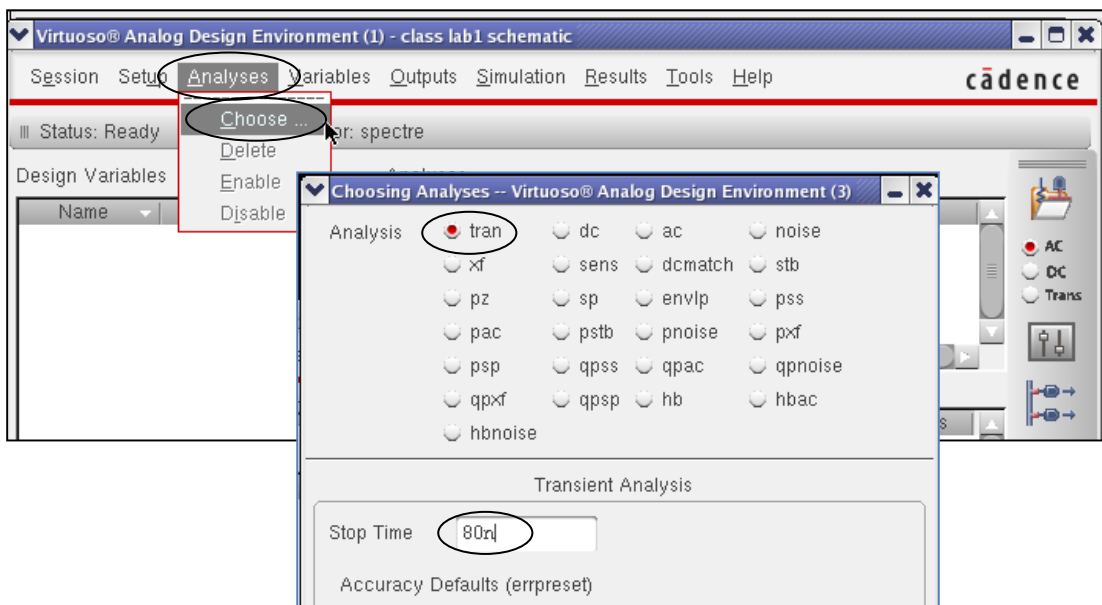   set *Stop Time* to 80n (2 times of period)

Figure Lab2-9 : Setup Analysis

(g)   Assign values to the variables used in the circuit
        Variable → Edit → Copy from
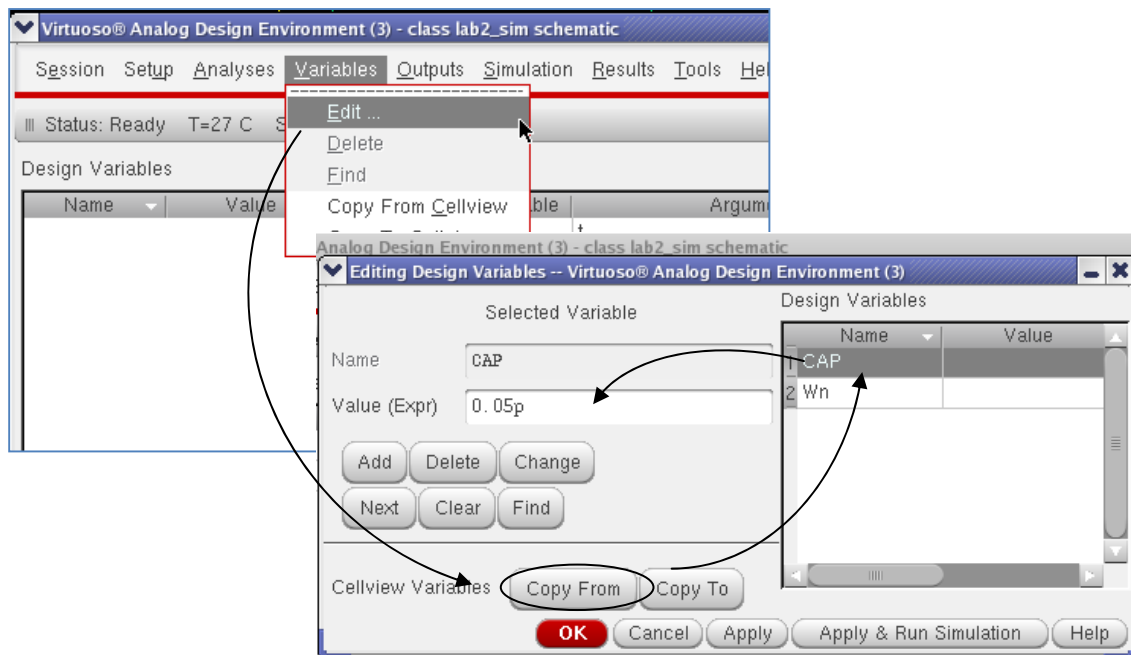   set **CAP** to 0.05p
        set **Wn** to 120n

Figure Lab2-10 : Edit Variables

(h)   Select signals to be monitored (plotted) graphically
        Outputs → To Be Plotted → Select from Schematic
        Select the **wire** *of input, 01nmos and 02nmos*

        Note : By clicking on the **wire**, the voltage of this wire wrt gnd is being
                monitored.

        Press **ESC**   (to avoid toggling effect of unselecting the desired signals)

(j)   Run Simulation
        Simulation → Netlist and Run

Account Number: g4[ ]_[   ]   **Name:_____**

Submission of Lab2:

5.   What are the functions of the NMOS transistors *in this circuit ?*

6.   How does I3 (Figure Lab2-1) affects the voltage of 01nmos ?

7.   Measure the voltage level at *01nmos* and *02nmos.* Explain the difference in voltage between the 2 voltages.

          In the Waveform Window
          (a)   ***Marker → Create_Marker→Point→OK,*** then drag the marker to the desired location.

          (b)   Place cursor at the highest point of 01nmos and 02nmos.

8.   To simulate the circuit with a new set of values

          From Analog Environment Window
          (a)   ***Variable → Edit → Wn → 300n*** (change the width of the transistor)

          (b)   ***Simulation → Run*** (rerun with the new settings)

9.   What is the effect of changing the width of the N-pass transistors on the voltage of *01nmos and 02nmos* ? Substantiate your answer with relevant equations.