Nanyang Polytechnic

School of Engineering

Diploma in Electronics Computer & Communications Engineering (EGDF01)

EXPERIMENT NO	:	Lab 01 (Duration : 2 hours)
EXPERIMENT TITLE	:	To study the I_{ds} vs V_{ds} of an NMOS transistor
OBJECTIVE	:	1. Familiarization with Sun Desktop User Environment and Analog Environment - Spectre simulator 2. Study the characteristic of an NMOS transistor

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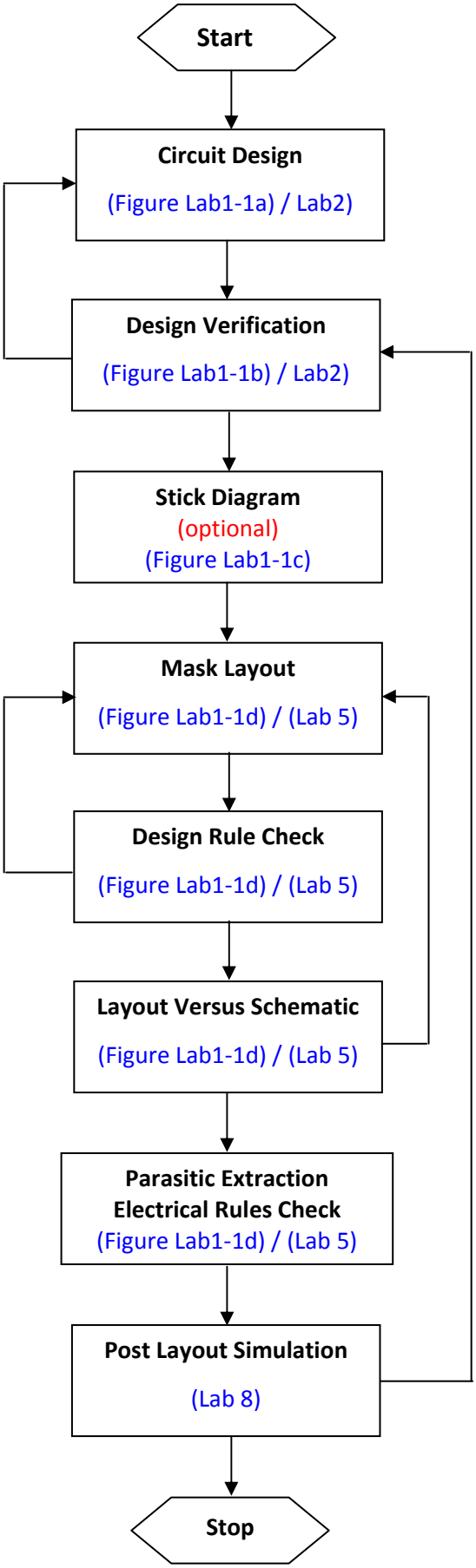


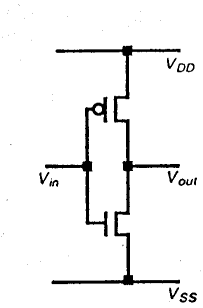


Figure Lab1-1a
Transistor Level Schematic

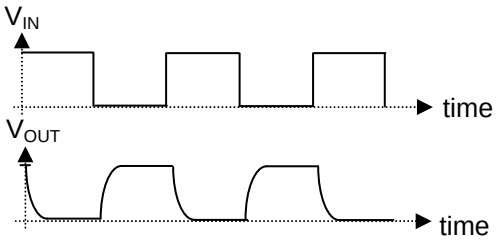


Figure Lab1-1b
Simulation / Verification

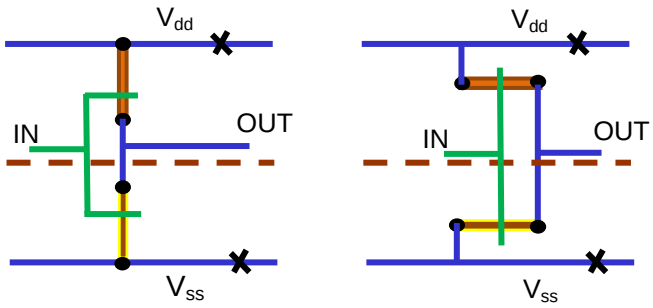


Figure Lab1-1c
Stick Diagram

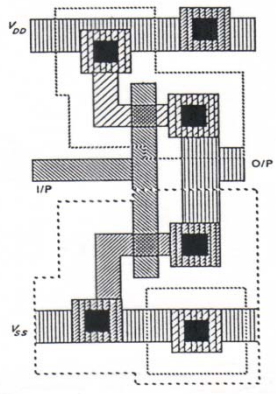


Figure Lab1-1d
Mask Layout

Design Verification

The objective of design verification is to ensure that the design meets the required specifications and fabrication design rules before the masks are submitted to the factory for mass production.

Simulator (Spectre)
The simulator helps ensure that the circuits designed **(Figure Lab1-1a)** perform the intended functions. It also checks that the circuit meets the timing/speed or frequency response requirements.

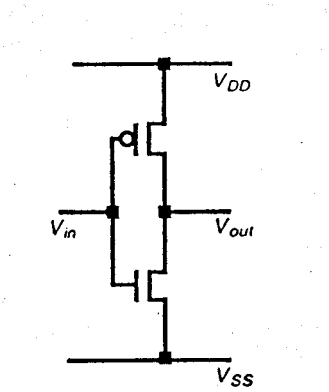


Figure Lab1-1a
Transistor Level Schematic

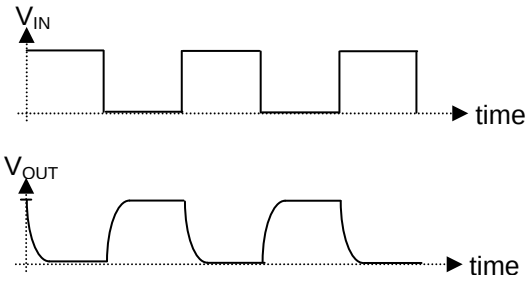
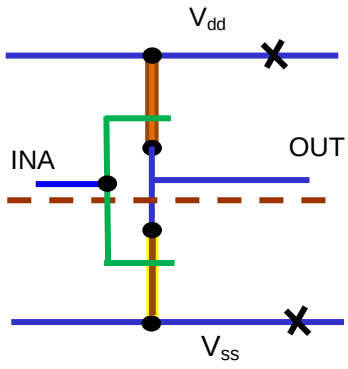


Figure Lab1-1b
Simulation / Verification
(Analog Environment)

Mask Layout

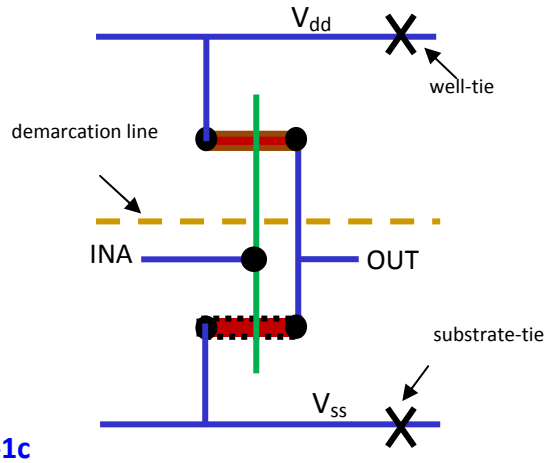
(i) Stick Diagram

Stick diagram is used as the intermediate step when translating schematic circuit to geometrical data so that orientation of the layout (e.g. input/output pins, power line, transistors, etc) can be organized before actual layout design in carried out in the CAD environment.



Stick Diagram A

Figure Lab1-1c



Stick Diagram B
(preferred style)

(ii) Layout (Virtuoso)

The stick diagram of each design is converted to mask design (MOS layers) in a CAD environment (eg Virtuoso) and interconnect to mask layout of other cells to form the functional block. There are 3 main layers used in mask layout design, namely the diffusion layer (green), the polysilicon layer (red) and the metal layer (blue). Each of these layers is isolated from one another by either thick or thin silicon oxide.

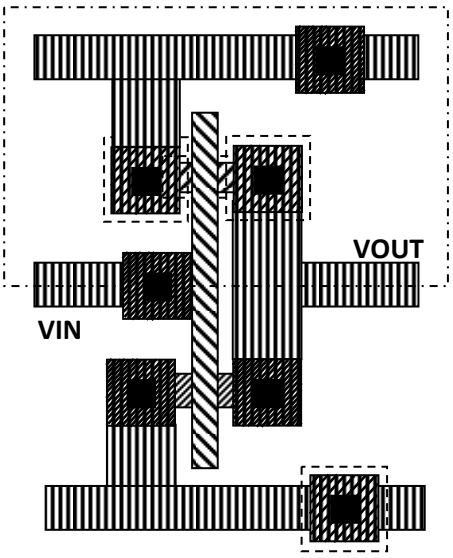
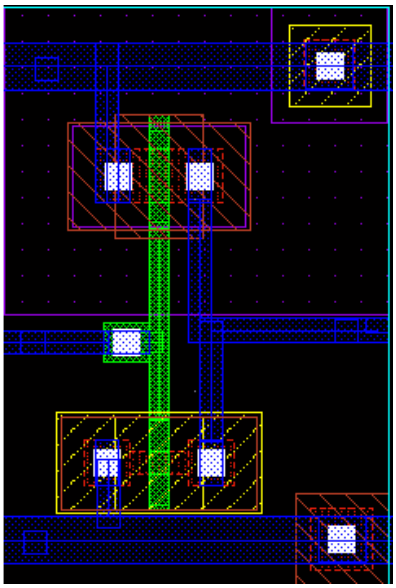


Figure Lab1-1d
Mask Layout



(iii) Design Rule Checker (DRC)

This tool verifies that the mask layout designed **(Figure Lab1-1d)** meets the design rules specified by the target process technology.

(iv) Layout Versus Schematic Check (LVS)

The LVS verify that the mask layout design **(Figure Lab1-1d)** is the same as the intended schematic **(Figure Lab1-1a)** in terms of devices (transistors type, resistor, etc), size of the transistors, value of the resistors, etc as well as the interconnects. It also helps locate unconnected, partly connected or extra devices.

Part of LVS check also includes the function of Electrical Rules Check (ERC). ERC verify power connections and check for minimum conductor width for current specifications. It also locates floating nodes (gate of transistors), short circuits and as well as disabled transistors.

(v) Layout Parasitic Extractor (LPE)

LPE extracts the parasitic resistance and capacitance value based on the completed mask layout design. This is done through calculating the resistance and capacitance values based on the geometry drawn.

Post-Layout Simulation

Post-layout simulation gives a more accurate performance index because the extracted parasitic resistances and capacitances values are feedback into the simulator environment (values are added to the respective nodes in the circuit) and timing check is done to ensure that it still meets the specifications.

Familiarisation with Sun Java Desktop Environment

Logging into the System

(a) Key in User Name:

Figure Lab1-1 : Solaris Login Screen

(b) Login : **gXX_X** (to be assigned)
Password : **gXX_X**

Note: All Unix commands are case sensitive.

(c) Upon login to a typical Sun Java Desktop Panel, open a terminal window
Right Click → Open Terminal

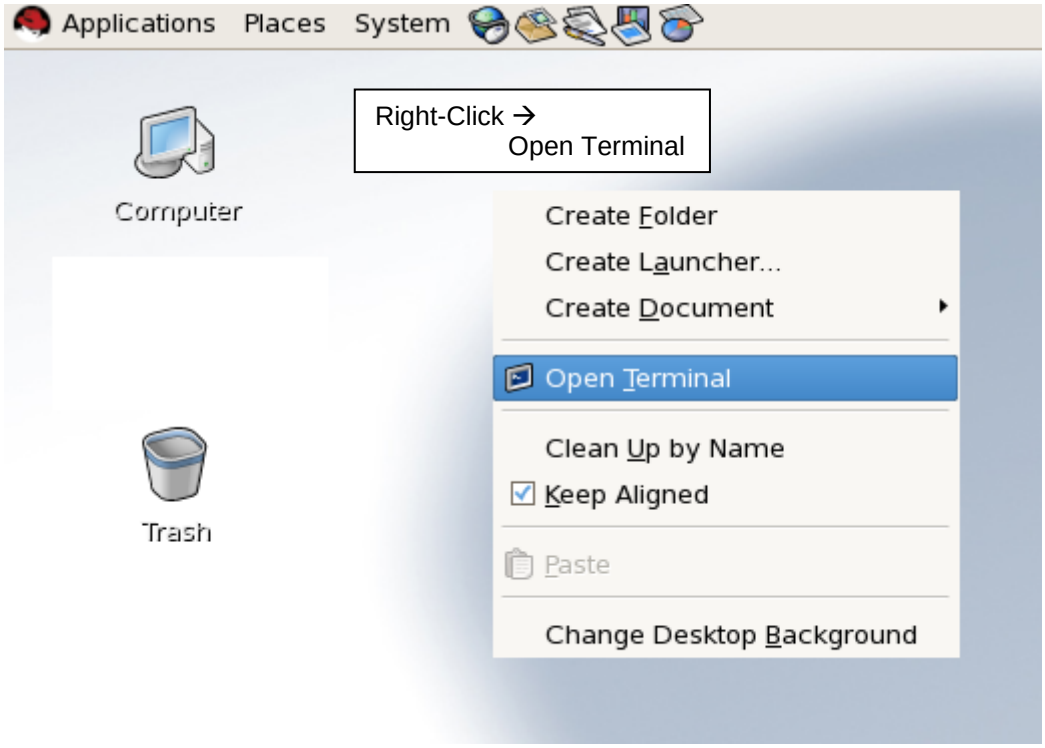


Figure Lab1-2 : Solaris Java Desktop Environment

(d) The computer interacts with the user via this terminal.

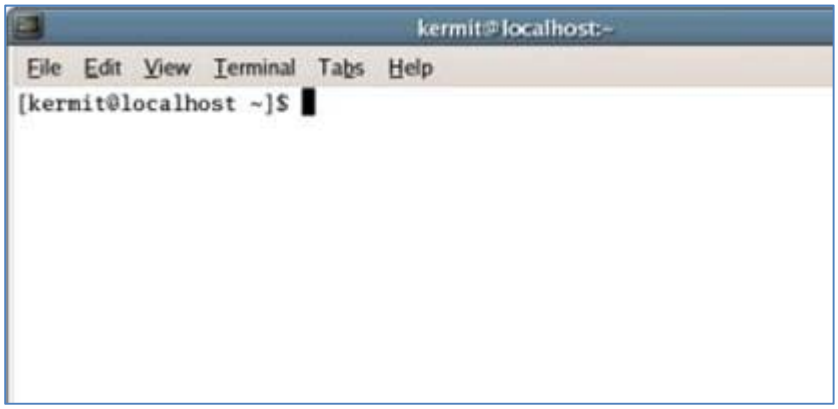


Figure Lab1-3 : Solaris Command Terminal

(e) To exit the Desktop environment,
System → Logout gXX_XX

1 *Familiarization with Cadence Design Software*

(a) **cd term1**

(b) **source cshrc**

(c) **virtuoso &**

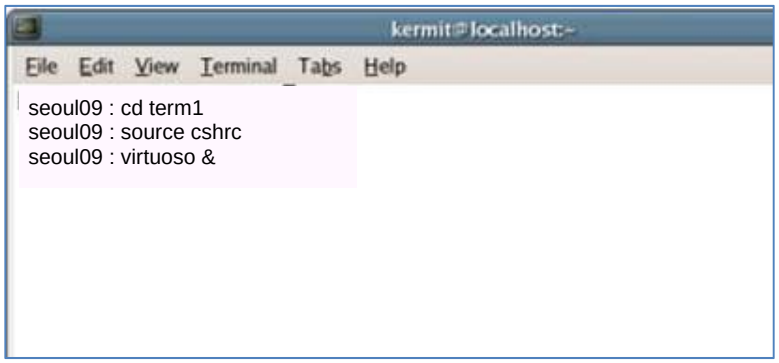


Figure Lab1-3a : Solaris Command Terminal

(d) The Command Interface Window (CIW) of the Cadence Design software displays the process and command executed by the software. It also displays the errors encountered during execution.

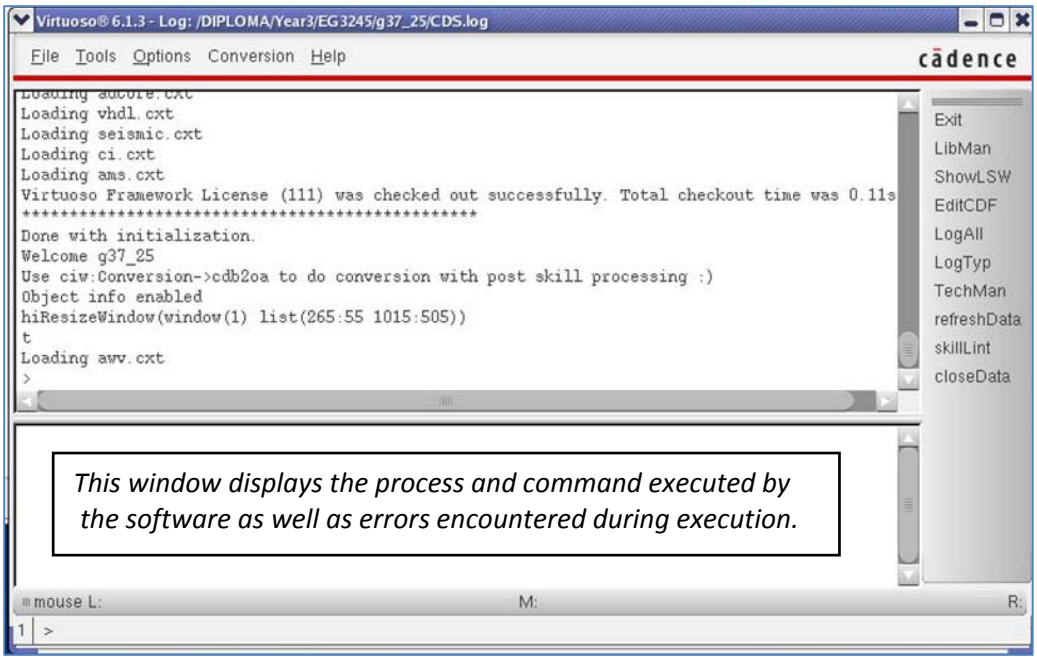


Figure Lab1-4 : Cadence Command Interface Window

(e) Tools -> Library Manager (shows reference libraries database and class library)

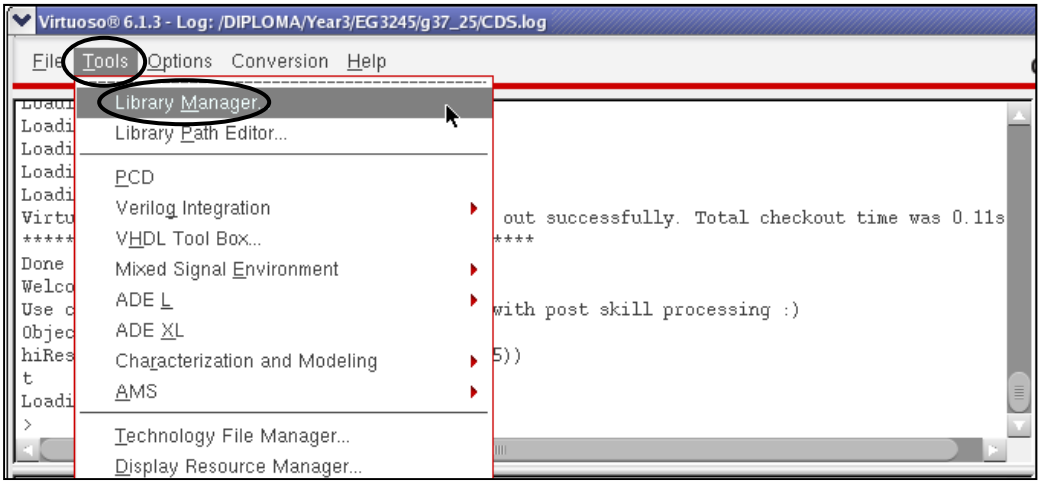


Figure Lab1-5 : Steps to invoke Library Manager

(f) ***class*** library is where your design is created. Others are reference libraries holding standard components used for design.

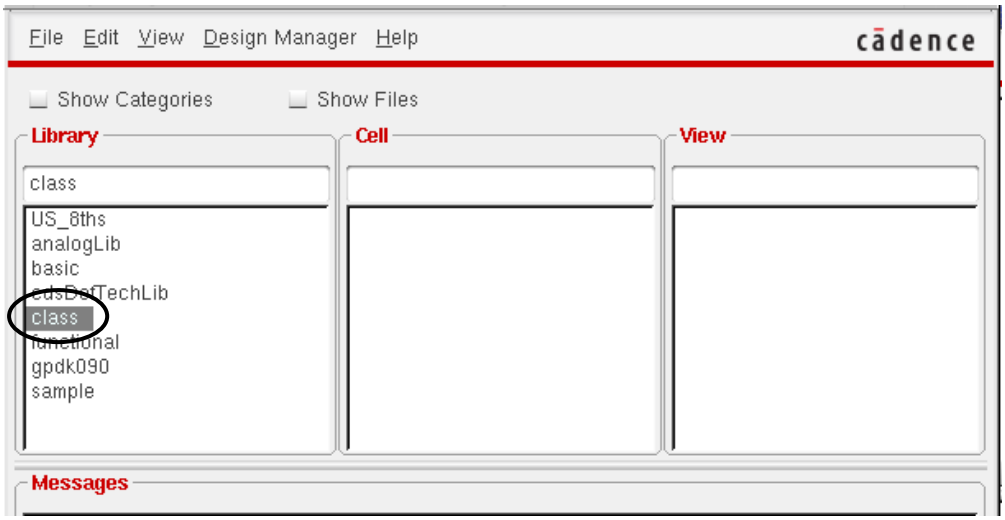


Figure Lab1-6 : Library Manager Window

2 *Capture schematic of a NMOS Biasing Circuit*

(a) To ***create*** a new schematic design
File → New → Cellview

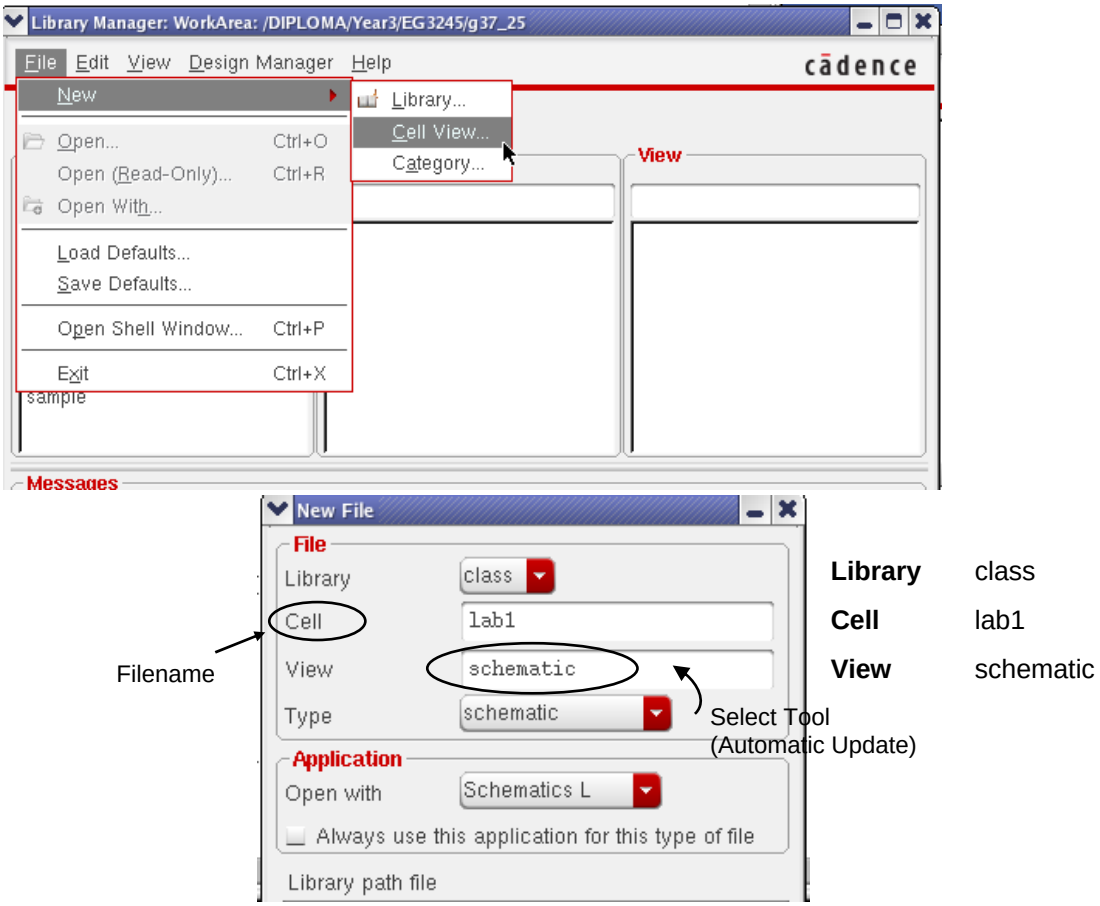


Figure Lab1-7 : Create New Cellview - Schematic

(b) Create a new schematic as shown in Figure Lab1-8.

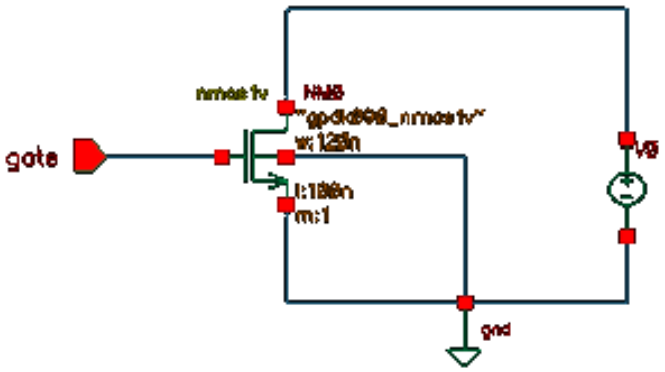
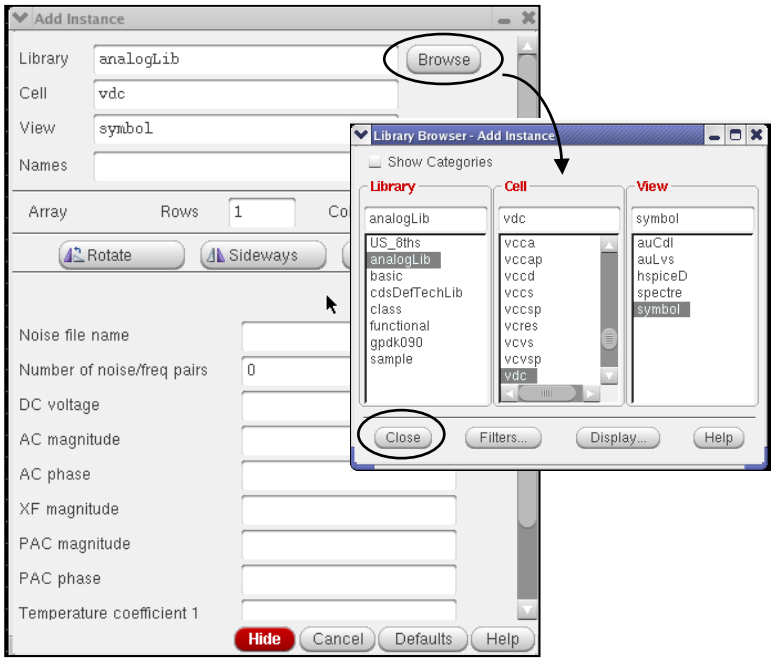


Figure Lab1-8 : NMOS Biasing Circuit

(c) ***Create → Instance***



Library analogLib
Cell vdc
View symbol

Figure Lab1-9 : Add Supply Source

(d) ***Click*** on the schematic window to place component, then press ***ESC*** to cancel command.

(e) ***Create → Instance***

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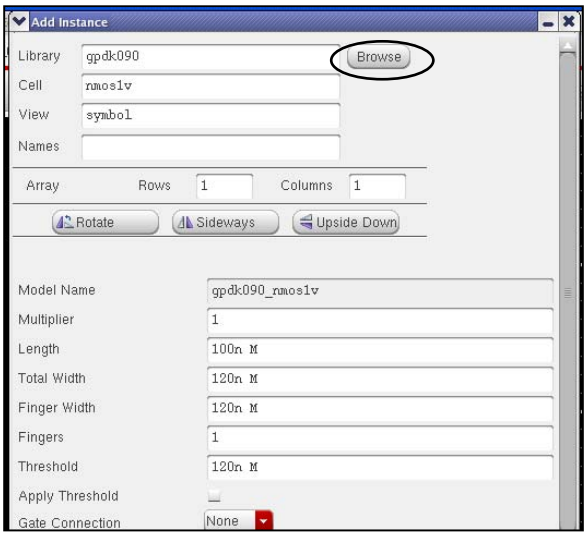


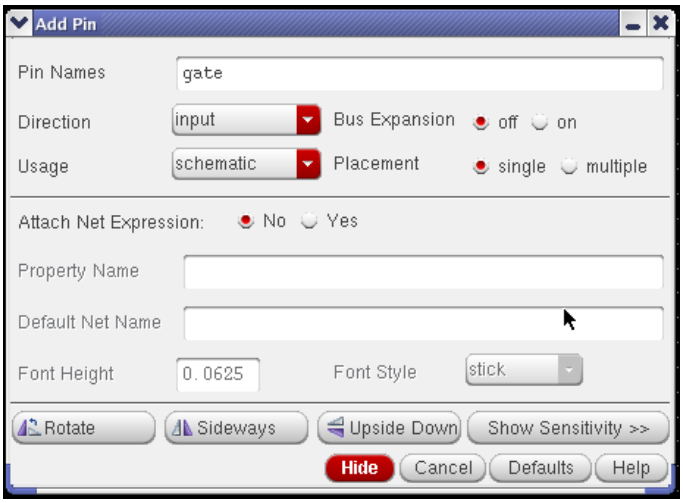
Library gpdk090
Cell nmos1v
View symbol

Length 100n M
Finger Width 120n M

Figure Lab1-10 : Add NMOS Transistor

(f) Repeat step (c) to instantiate ***gnd*** from ***analogLib*** library.

(g) ***Create → Pin***



Pin Names gate

Direction input

Attach Net Expression No

Figure Lab1-11 : Add Pin

(h) To make connections
Create → Wire (narrow)

(i) To add names to interconnections for ease of referencing/probing
Create → wire name

(j) To check the properties associated of gate/instance or wire, pins, etc
Use left mouse button to select an instance and type **q**

(k) ***File → Check and Save***

3 *Familiarisation with Spectre simulator - Analog Design Environment*

(a) non-linear analogue circuit simulator
(b) allows verifying functionality of analogue electronic design captured by schematic editor composer
(c) supports various modeling models such as hspice, BSIM3, spectre

Analog Analysis supported by simulator

- *Transient analyses*
  Provides the transient (momentary) output response of the circuit with respect to time.

- *AC analyses*
  Simulates the ac performance of the circuit as a function of frequency, and is based on small-signal frequency response model.

- *DC analyses*
  Determines the dc operating point of the circuit based on the parameters present on the schematic, assuming all capacitors opened and all inductors shorted.

- *Sweep analyses*
  Generates dc transfer characteristics for the circuit by varying a user specified independent source over a range of values.

4 *To Obtain the I_{ds} vs V_{ds} Characteristic Curve of an NMOS transistor*

(a) Launch Analog Design Environment for simulation
Launch → ADE L

(b) Setup the stimulus and type of analysis
Setup → Stimuli
set *gate* to **DC** 1.2 (Volts)

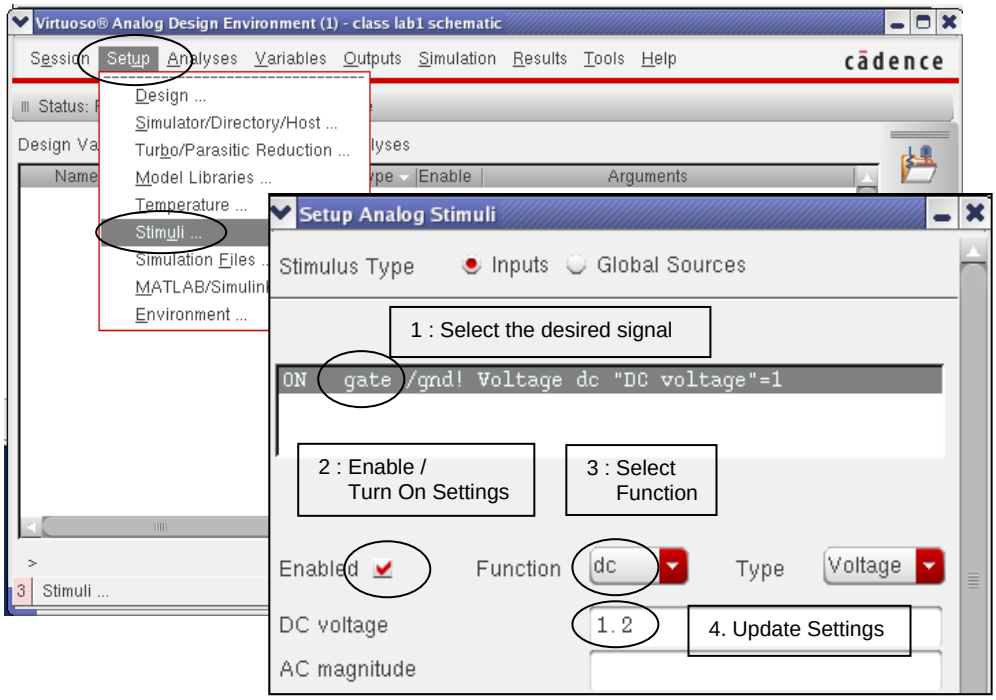


Figure Lab1-12 : Setup Stimulus

(c) **Analysis → Choose**

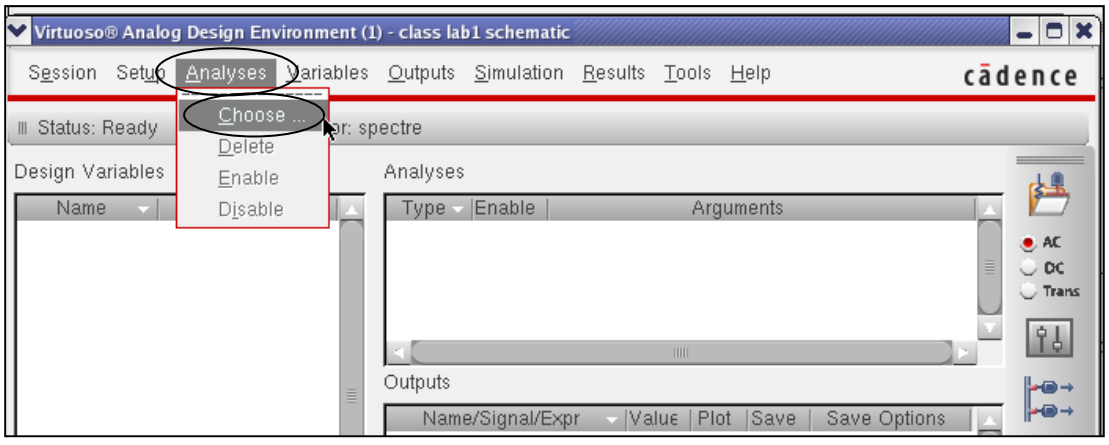


Figure Lab1-13 : Choose Analysis

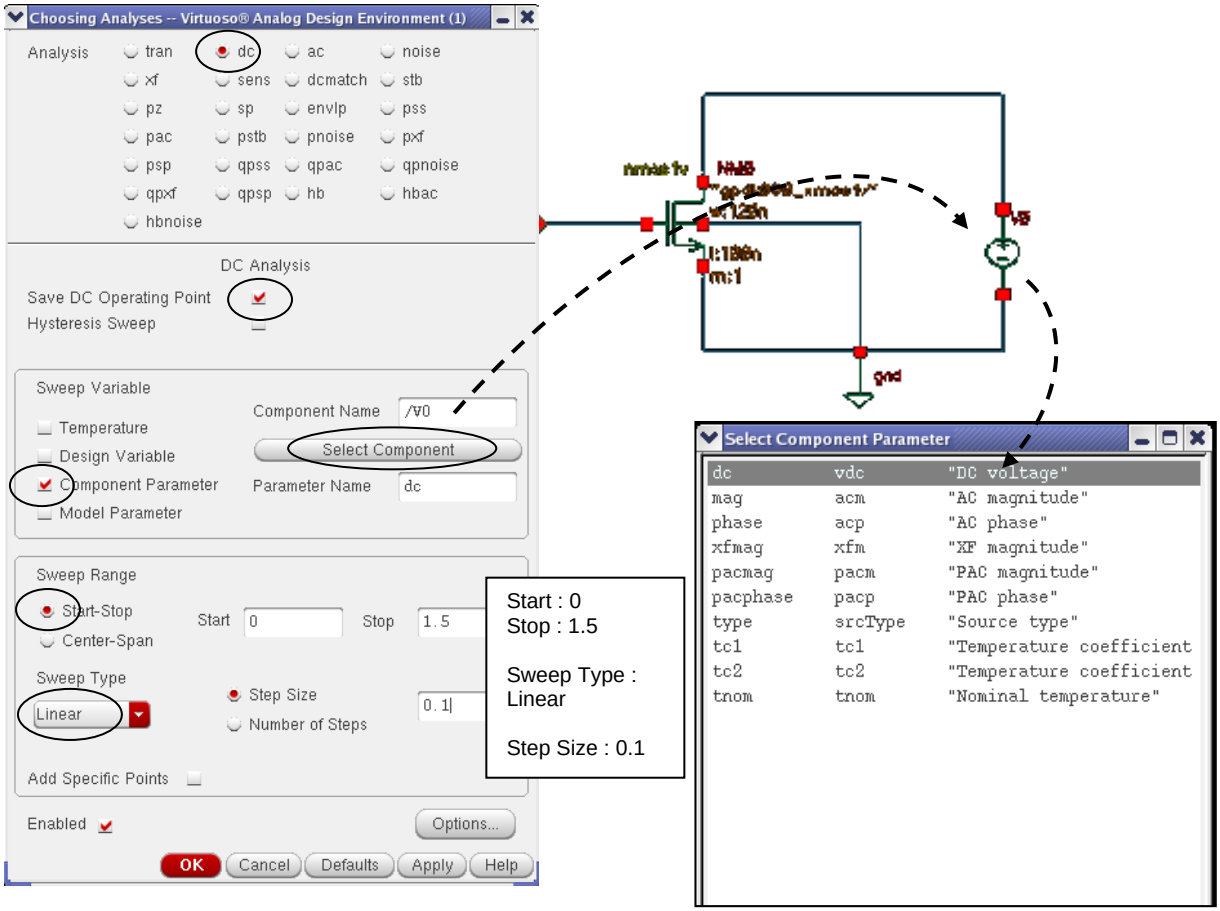


Figure Lab1-14 : Setup DC Sweep Parameter

(d) ***Output → To Be Plotted → Select on Schematic***
(click on the **drain** terminal of the transistor to monitor I_{ds} current and press **ESC**)

*Note: if click on the **terminal** (of component) it will probe and plot **current** level
*Note: if click on the **wire** (net) it will probe and plot **voltage** level

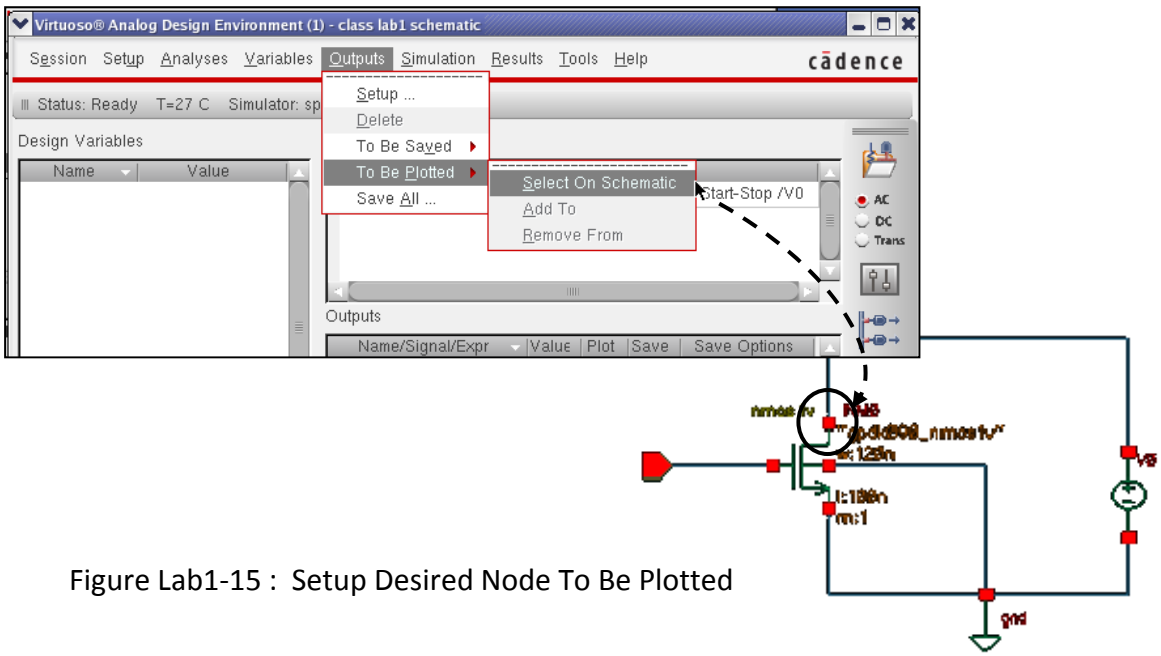


Figure Lab1-15 : Setup Desired Node To Be Plotted

(e) **Run** Simulation

Simulation → Netlist and Run

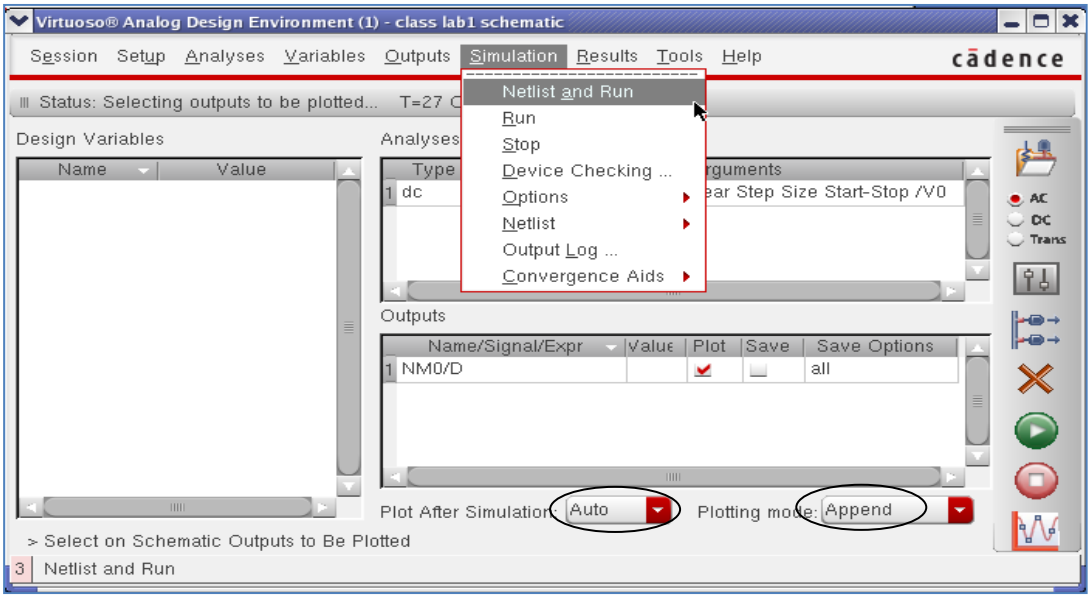


Figure Lab1-16 : Run Simulation

(f) Repeat step (b) and **set** *gate* to 1.0 : DC

(g) Repeat step (e) to run simulation

Note : The graph for *gate=1.0* will be appended to the waveform window of the first simulation.

(h) Repeat step (b) and (e) for *gate* = 0.8, 0.6, 0.4 and 0.2.

(I) For the I_{ds} vs V_{ds} characteristic curve obtained, (refer Figure Lab1-17)

- Edit Chart Title

  Double-Click the title (1) → *Edit it to* ***Ids vs Vds characteristic Curve***

- Label all curves

  Double-Click the legend (2) → *Edit it to* ***NM0/D (1.2)***

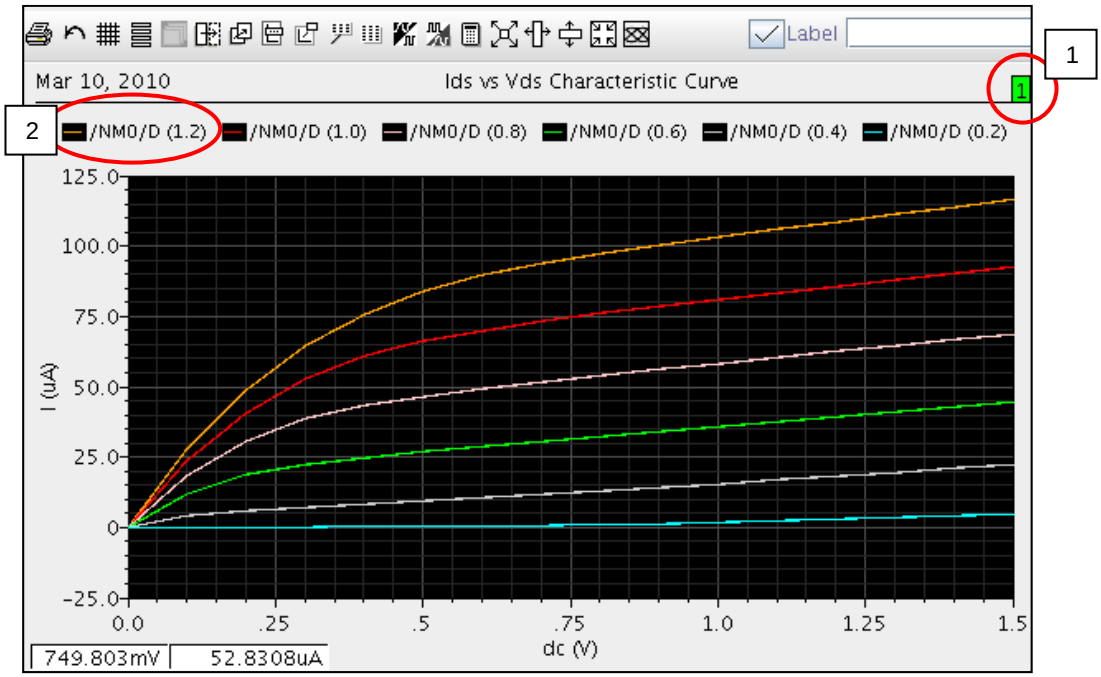


Figure Lab1-17 : Waveform Window

Submission

Print the chart and

(i) draw the line that separates the linear and saturation region.

(ii) label the 3 regions of operation.

(iii) state the voltage equations for each of the region.