School of Engineering

Diploma in Electronics Computer & Communications Engineering
(EGDF01)

EXPERIMENT NO	:	Lab 10 (Duration : 2 hours)
EXPERIMENT TITLE	:	Place and Route of Shifter using Cadence Encounter
OBJECTIVE	:	To perform place and route of Shifter

Exercise 1

To do place and route of the Shifter synthesized in Lab9 using Cadence Encounter

1. Open a new Terminal
   Type :
   cd
   cd term2
   source cshrc

2. Change directory
   Type :
   cd EN
   encounter to launch the software.

3. In Encounter GUI, **File→Import Design**.
   Click **Load**, select **shifter_top.globals** and click **Open**.

4. Floorplanning:
   Floor plan→Specify Floorplan.
   Ratio=1, Core Utilization=0.6, Core to Left/Right/Top/Bottom=10.
   click **OK**.

5. We are going to add 2 supply rings for VDD and VSS.
   Power→Power Planning→Add Ring.
   Nets: VDD VSS
   Width=4, Spacing=0.8, Center in Channel.
   Click **OK**.

6. **File→SaveDesign**, check **Encounter** and call it **stepS1.enc**
   Click **OK**.

7. Before we proceed further, we need to instruct Encounter to connect signals VDD or VSS, and signals that connect to logic high or logic low, to supply ring VDD and VSS respectively.

   This can be done via the **Encounter-shell** as shown in Figure 1.

```
 0.000M) ***
encounter 1> globalNetConnect VDD -type pgpin -pin VDD -all
encounter 2> globalNetConnect VSS -type pgpin -pin VSS -all
encounter 3> globalNetConnect VDD -type tiehi
encounter 4> globalNetConnect VSS -type tielo
encounter 5>
```

Figure 1 Power Pins Connection

8. Gates are placed in the layout row-by-row. We need to provide supply rails for them.
Route→Special Route.
Nets: VDD VSS
Top Layer: Metal5

9. Perform placement:
Place→Place Standard Cell.
File→SaveDesign to **stepS2.enc**

10. Routing
Route→ Nanoroute→Route to complete the routing.
Place→Physical Cell→Add Filler and select **FILL1, FILL1A, FILL2, FILL4, FILL8**
The complete layout produce by the software is shown in Figure 2.
File→SaveDesign to **stepS3.enc**

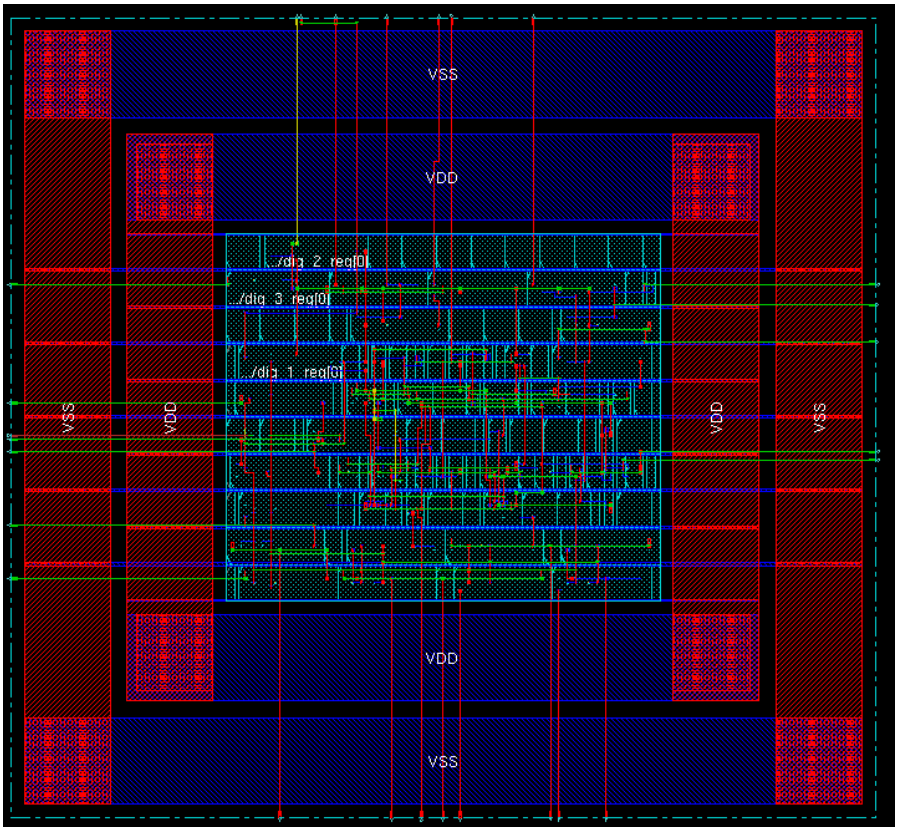

Figure 2 Complete Layout

11. **File→Save Netlist** to save the netlist as **../RTL/shifter_top_pnr.v**
Timing→Extract RC. Remember to check 'save SDF …'.
. **Timing→Write SDF.** Name the file as **shifter_top_pnr.sdf** (in /RTL directory).
We are ready to simulate the circuit again with the delay of wires included.
You can exit all the software.

Exercise 2 : Post-layout simulation

1. Type:
   cd .. to go up to …/term2.
   nclaunch&

2. **Right-click→Edit** on RTL/shifter_top_tb.v
   Change the variable to **PAR**.
   Save and **close** the file.

3. Select **shifter_top_pnr.v, shifter_top_tb.v** and **typical.v** and **right-click→NCVlog**
   *Note : This may take a while for the **typical.v** file to be compiled.*

4. Select **worklib/shifter_top_tb** and **right-click→NCElab**.
   Select **Snapshot/worklib.shifter_top_tb:module** and **right-click→NCSim**.
   Select **shifter_top_tb** and **right-click→Send To New→Waveform Window**.
   Simulation→Run.
   Click on waveform to bring **TimerA** to the desired location.
   Right-click→Create a marker to put additional marker.

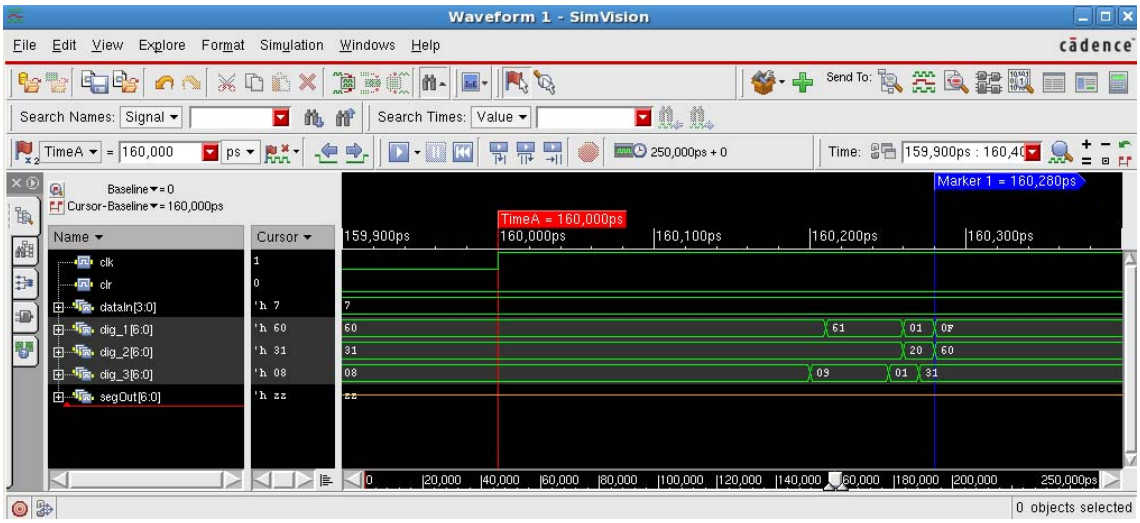

Figure 3 Result

5. As you can see, there is delay of **280ps** between postive-edge of **clk** and shifter's output. This is due to the gate delay and wiring since now we are simulating a post-layout circuit.