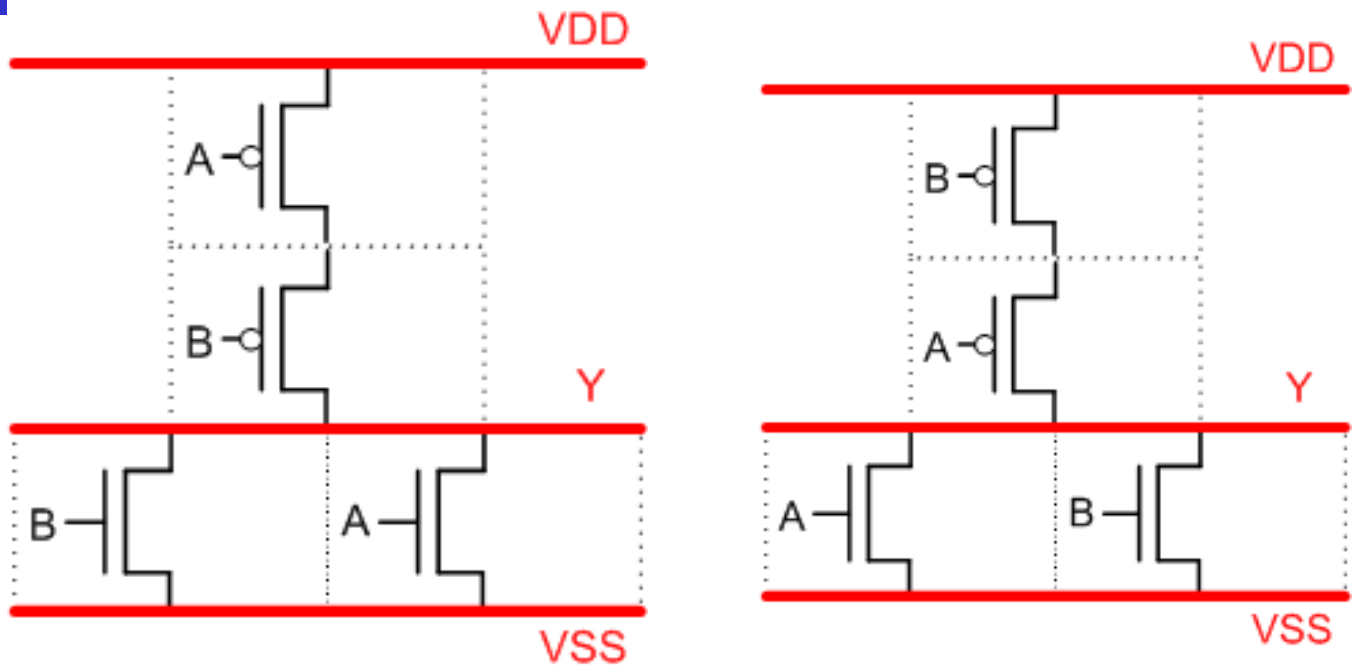
NOR gate

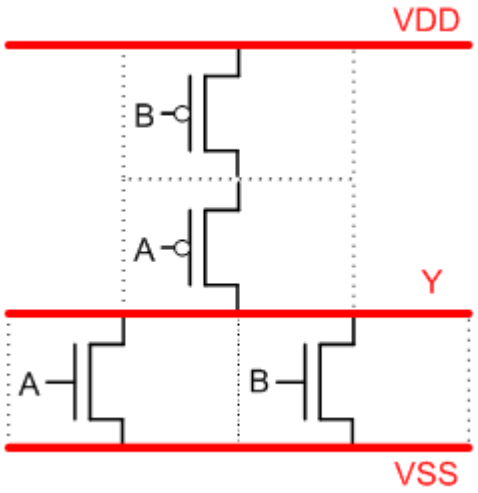


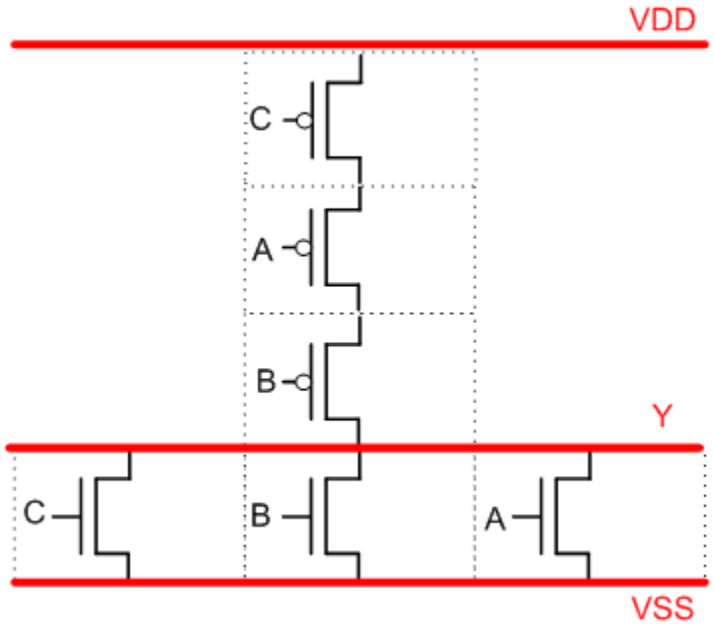
2-input NOR gate.

Note 1: The order of inputs does not affect its logic equation.

$$Y = \overline{(A + B)}$$

Multiple Inputs NOR





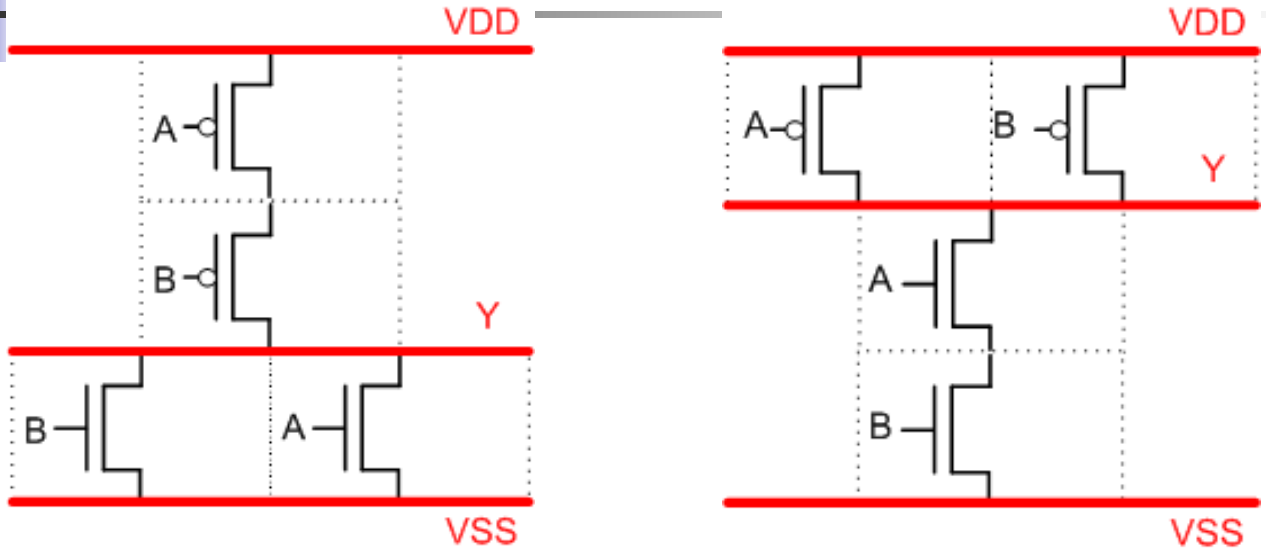
Note 2:

You can have more that 2 inputs. Similarly for NAND gate.

$$Y = \overline{(A + B)}$$

$$Y = \overline{(A + B + C)}$$

NOR and NAND



Note 3:
Top Part (divided by VOUT line) use PMOS and Bottom Part use NMOS.

Note 4: Duality.
If Top Part in series, Bottom Part in parallel.
If Bottom Part in series, Top Part in parallel.

Note 5:
NOR/OR is top series. NAND/AND is bottom series.

DeMorgan's Theorems

You should know DeMorgan's Theorems:

Note 6:

$$\overline{(A + B)} = \overline{(A)}.\overline{(B)}$$

$$\overline{(A.B)} = \overline{(A)} + \overline{(B)}$$

You might need to manipulate the logic equation, before implementation of complex gate.

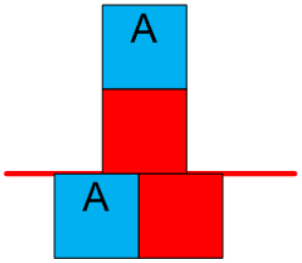
Conversion back and forth:

$$A + B = \overline{\overline{(A + B)}} = \overline{\overline{(A)}.\overline{(B)}} = \overline{\overline{(A)}} + \overline{\overline{(B)}} = A + B$$

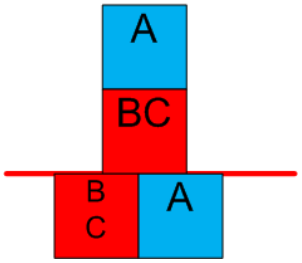
$$A.B = \overline{\overline{(A.B)}} = \overline{\overline{(A)} + \overline{(B)}} = \overline{\overline{(A)}}.\overline{\overline{(B)}} = A.B$$

Example 1: $Y = \overline{A + BC}$

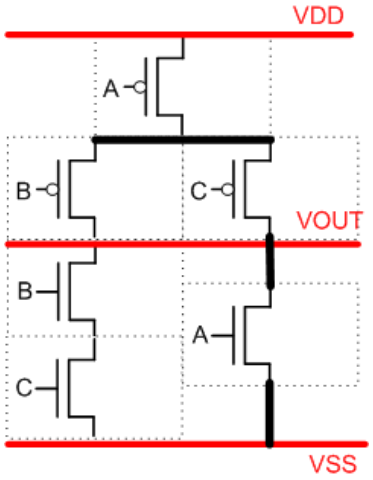
1. This is 2-input NOR → top-series.



2. BC → AND, bottom-series

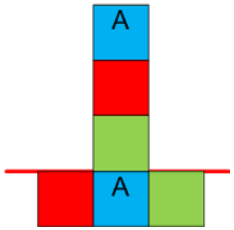


3. Substitute with PMOS and NMOS

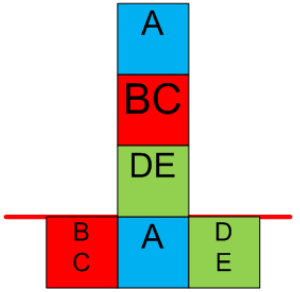


Example 2: $Y = \overline{(A + BC + DE)}$

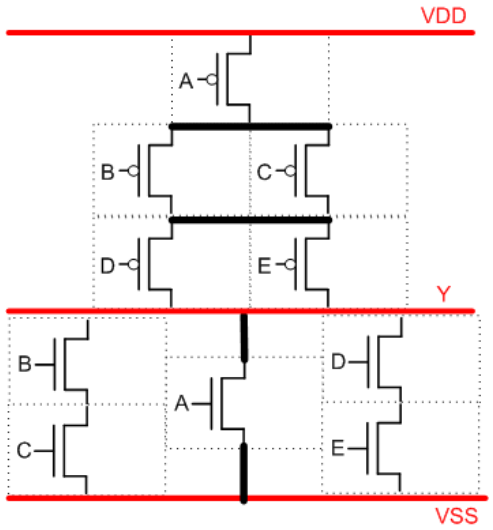
1. This is 3-input NOR → top-series.



2. BC → bottom-series
   DE → bottom-series



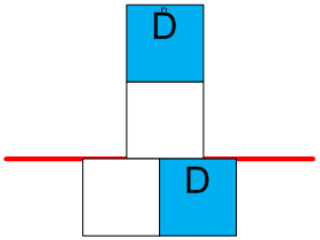
3. Substitute with PMOS and NMOS



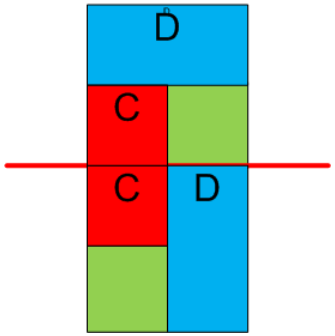
4. Since substitution of MOS is straight forward, we will not focus on this from now on.

Example 3: $Y = \overline{(A + B)C + D}$

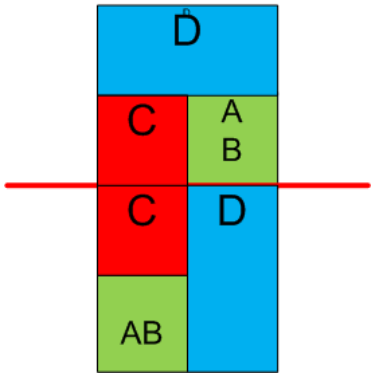
1. This is 2-input NOR → top-series.



2. (A+B) C → AND, bottom-series

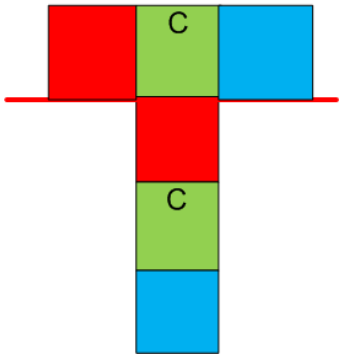


3. (A+B) → OR, top-series

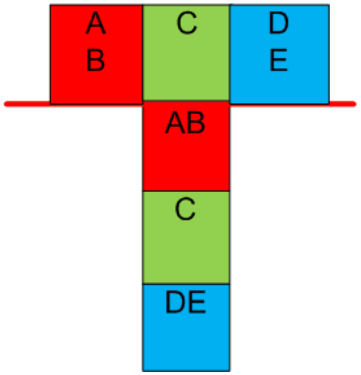


Example 4: $Y = \overline{(A+B).C.(D+E)}$

1. This is 3-input NAND → bottom-series.

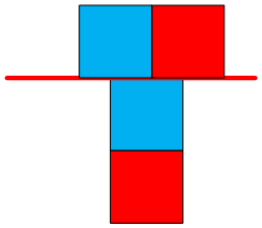


2. (A+B) → OR, top-series
   (D+E) → OR, top-series



Example 5: $Y = \overline{\overline{A + B}.(C + DE)}$

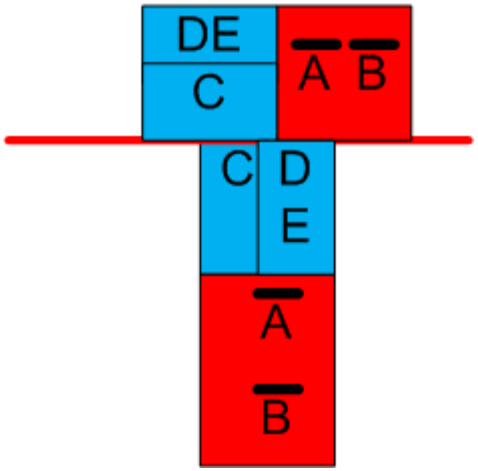
1. This is 2-input NAND → bottom-series.



2. $\overline{A + B} = \overline{A}.\overline{B}$ → must be converted. AND, bottom-series

Note 8: Only AND or OR are allowed under the 1 big bar.

$$Y = \overline{\overline{A}.\overline{B}.(C + DE)}$$



3. Negated Inputs are allowed

Example 6: $Y = \overline{\overline{AB} + (C + DE)}$

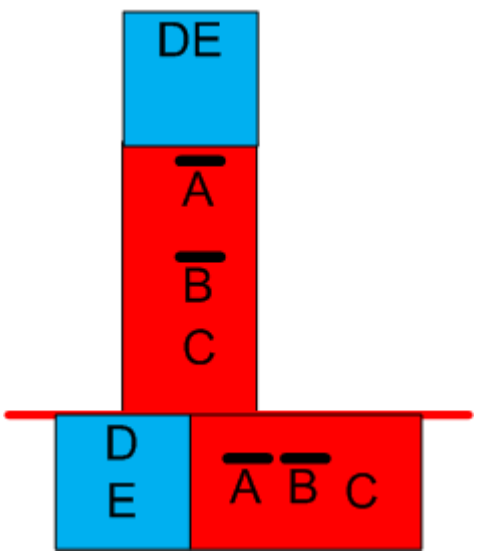
1. $\overline{\overline{AB}} = \overline{A} + \overline{B}$ → must be converted.

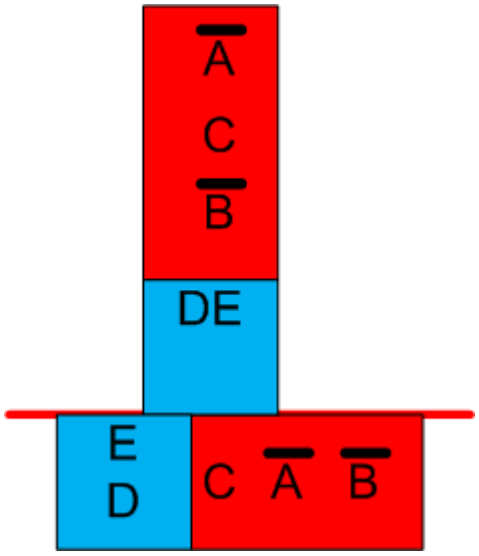
Note 8: Only AND or OR are allowed under the 1 big bar.

2. This is 4-input NAND → top-series.

3. DE → AND, bottom-series

$$Y = \overline{\overline{A} + \overline{B} + C + DE}$$





4. Order of inputs does not affect logic equation. Both solutions are acceptable

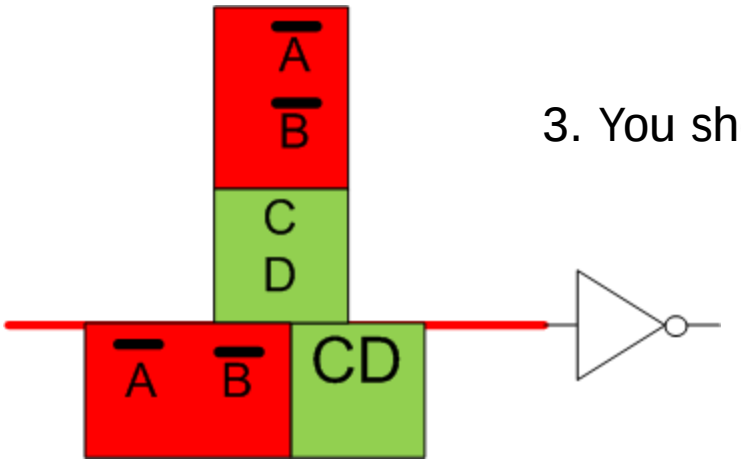
Example 7: $Y = \overline{AB} + (C + D)$

1. The equation is not in NAND or NOR form. You need to add 2 bars.

2. This is a 3-input NOR + INVERTER $Y = \overline{\overline{AB} + C + D}$

3. $\overline{AB} = \overline{A} + \overline{B}$ → OR, top series. must be converted.

Note 8: Only AND or OR are allowed under the 1 big bar.



3. You should draw the schematic of inverter

Example 8: $Y = (A + B)(\overline{C} + \overline{D})$

1. The equation is not in NAND or NOR form. You need to add 2 bars.

2. This a 2-input NAND + INVERTER $Y = \overline{(A + B)\ (\overline{C} + \overline{D})}$