VCO Design
(1 JULY 2002)

Tan See Teck

1 Introduction

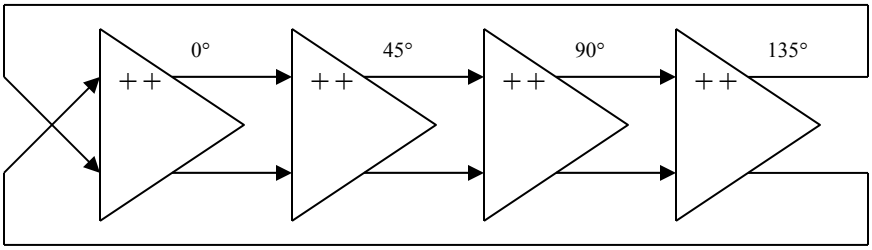
The objective is to design a VCO that center at 5GHz with five clock phases. It must be able to work under various process variations, temperature variation of 0 to 85°C and supply variation of 3.15 to 3.45V.

To obtain the five phases required by the phase detector (PD), ring type VCO is the most direct and simple choice.

Two types of ring VCO are suitable for our application – either ring LC VCO or ring RC VCO. Ring LC VCO has better phase noise performance than ring RC VCO. However, a total of 8 inductors will be required and large space will be needed as each inductor is about 200um by 200um.

RC VCO has poorer phase noise compare to LC VCO. However, for most CDR that utilities bang-bang type phase detector, ring type VCO with poorer phase noise are typically used. With ring RC VCO, substantial amount of space are saved.

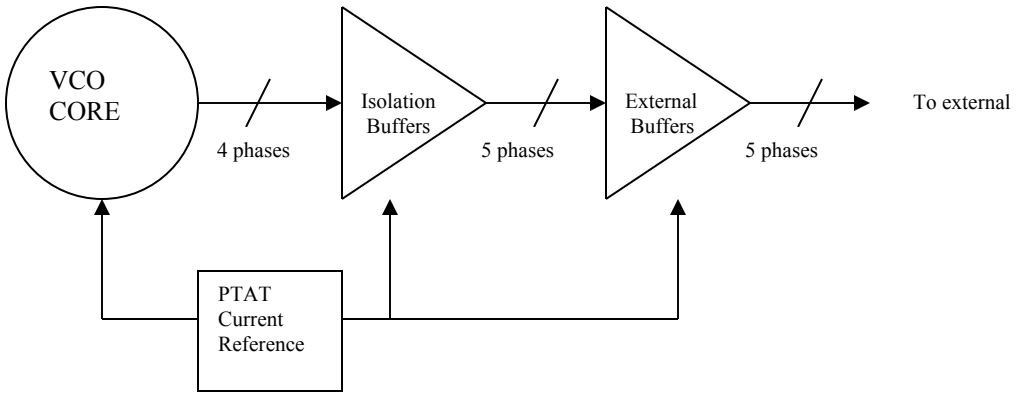
The VCO need to supply four clock phases (differential signal), namely 0°, 45°, 90°, 135° and 180° for the bang-bang phase detector. The 180° can be obtained from 0° by using an inverter. A four-stage ring with one of its outputs cross-connected (180° phase shift) to the next stage will be able to provide the required phases.



The overall delay through the loop will determine the oscillation frequency (Fosc). If the delay per stage is Td, then the Period of oscillation is 8*Td and Fosc=1/(8*Td).

2 Overview

The block diagram of the VCO, references, tuning network and buffers are shown.



VCO core will generate four phases of 0°, 45°, 90° and 135°. 180° phase is obtained by passing 0° phase through an inverter.

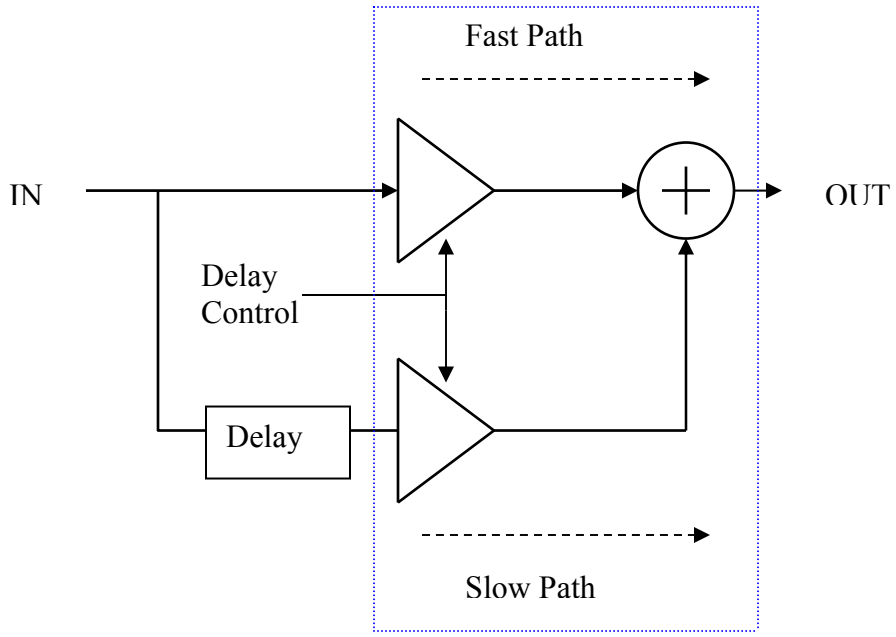
The Isolation Buffers provide isolation to prevent VCO pulling.

External Buffers provide driving capability for external 50Ω environment. It consists of cascade of emitter follower and current switch.

The External Buffers are not required if VCO and PD is integrated into one dice.

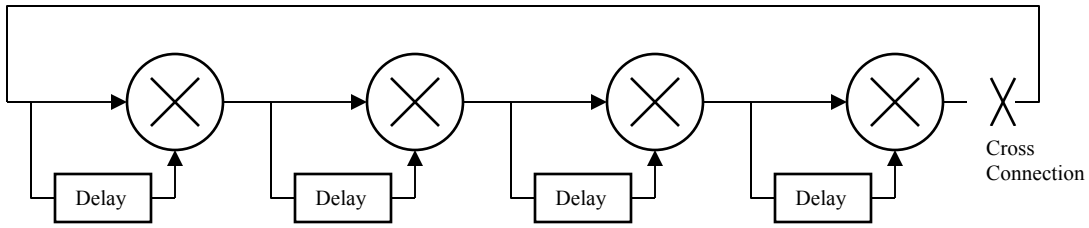
3 Tuning Method

Delay interpolation is adapted for the tuning of VCO. Interpolation is accomplished by varying the tail current of the 2 amplifiers in opposite directions to realize a fast path and a slow path. This method allows a wide and robust tuning range to be accomplished so as to tolerate process and temperature variations.

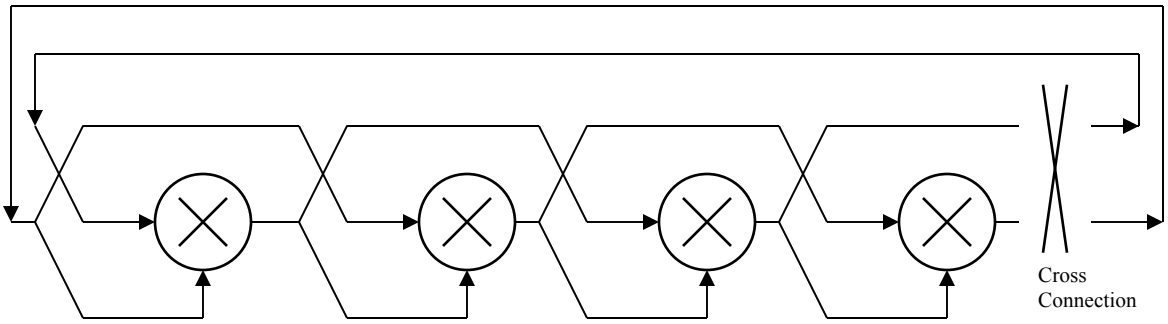


Interpolator

VCO could be connected as shown by using four delay networks and four interpolators.



With the following connection, similar function is achieved without delay networks. This type of VCO is termed feed-forward VCO.

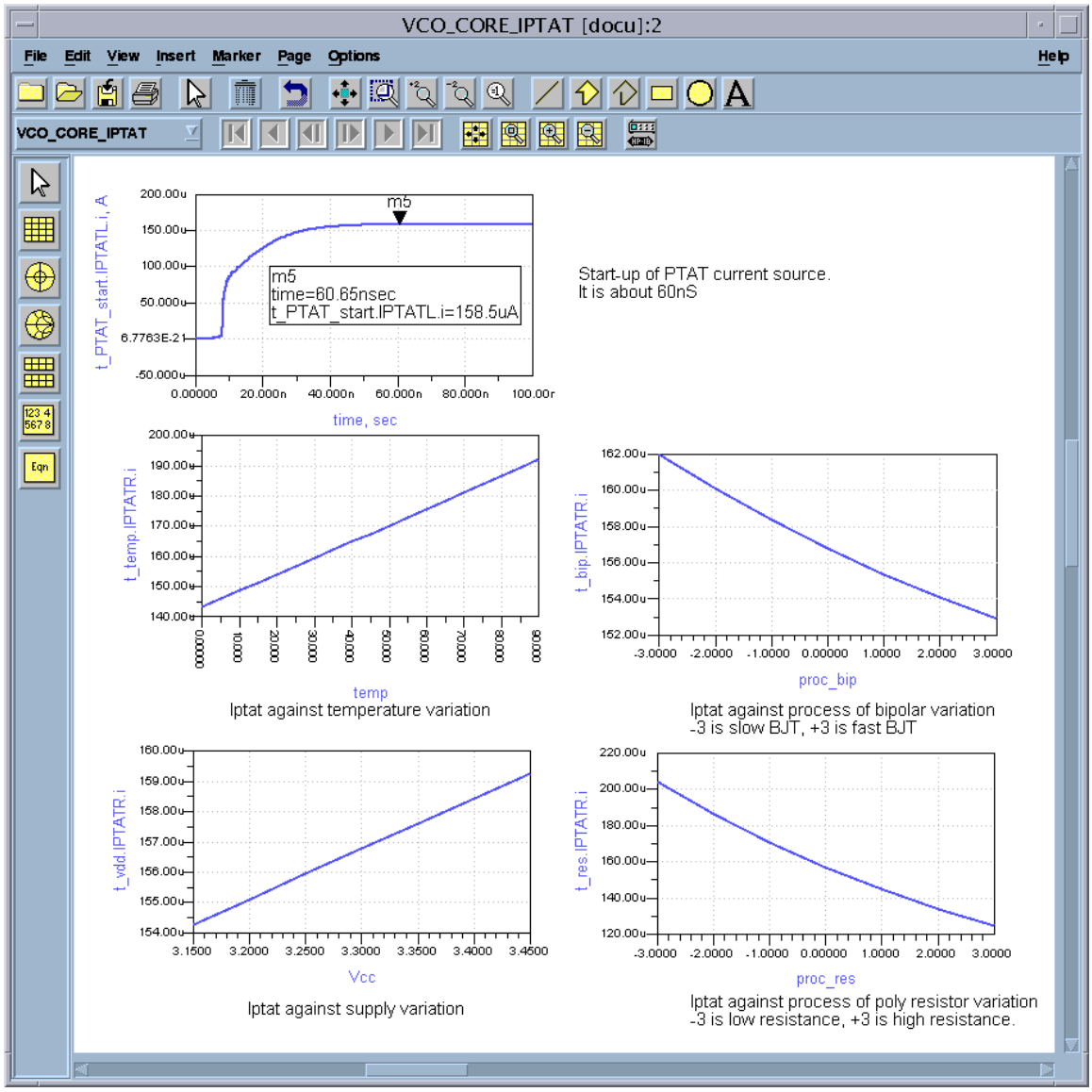


4 PTAT Current Reference

The VCO Core current sources are referred to a PTAT Current Reference (150uA). PTAT Current Reference is used because it has better power supply rejection ratio. If the supply rejection is poor, noise on supply line will modulate the current reference, and this in term will modulate the VCO and causes jitter.

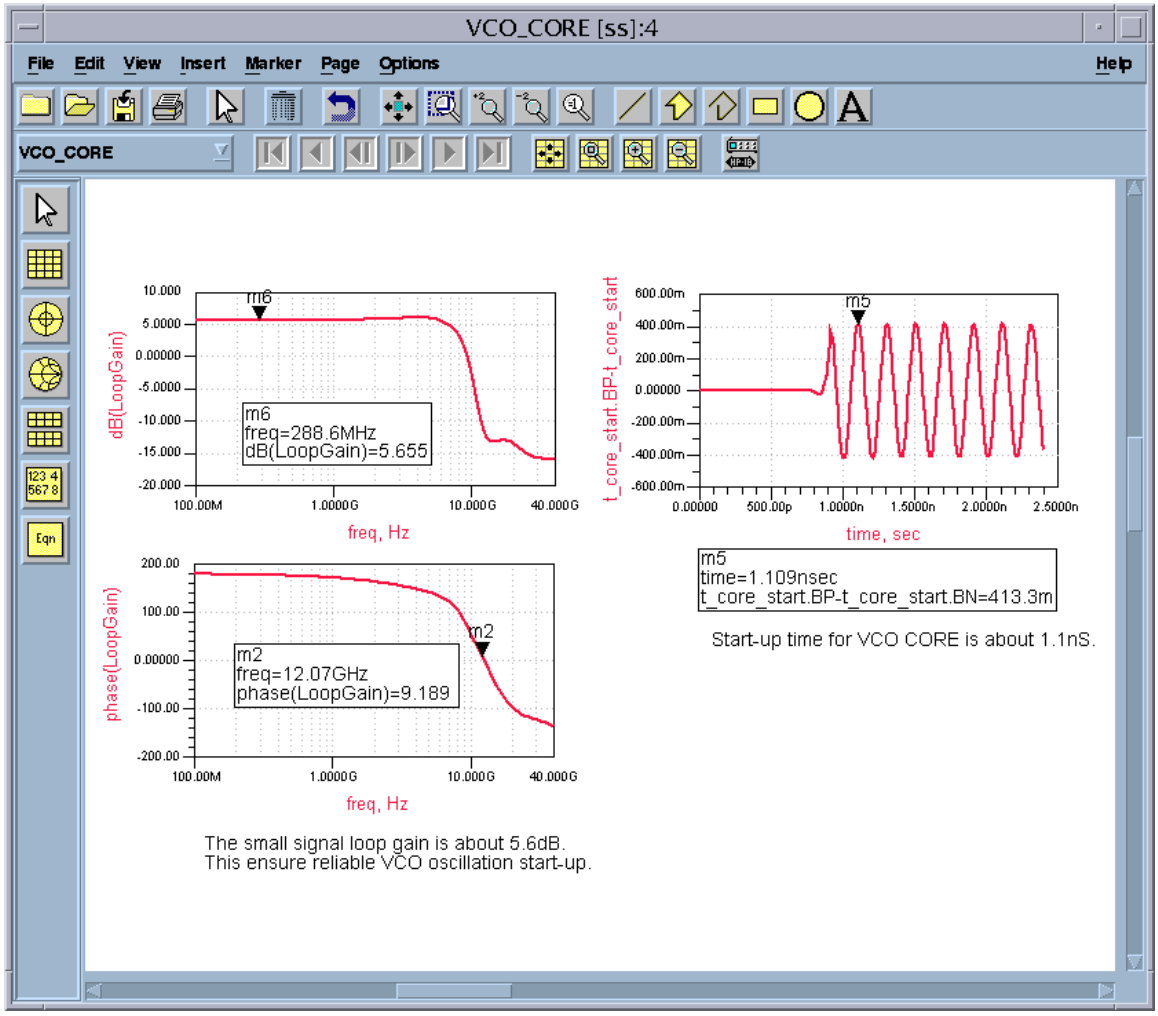
The start-up time for the PTAT Current Reference is about 60ns as shown.

The variation of PTAT current reference against process, supply and temperature are also shown.

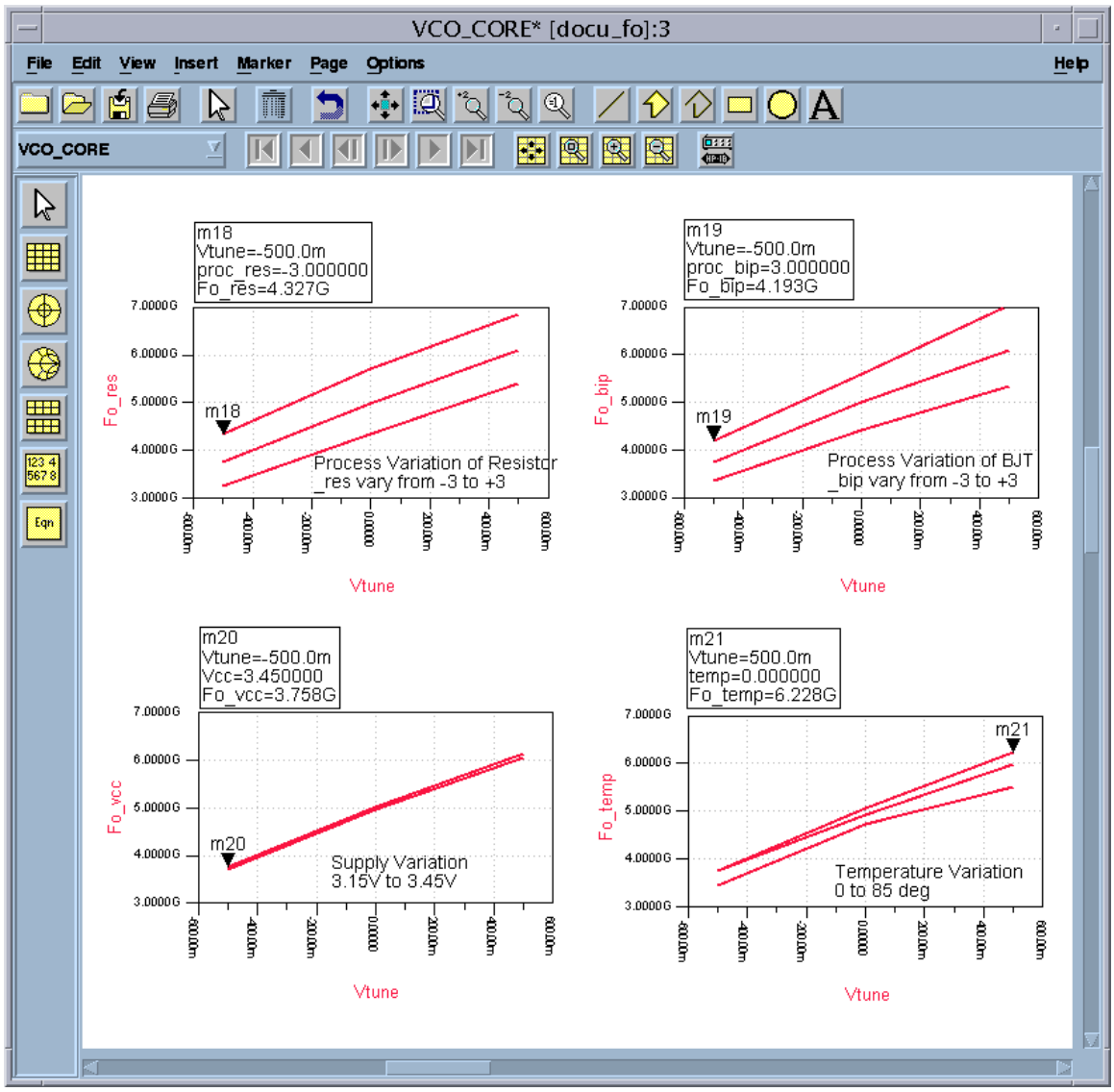


5 Result

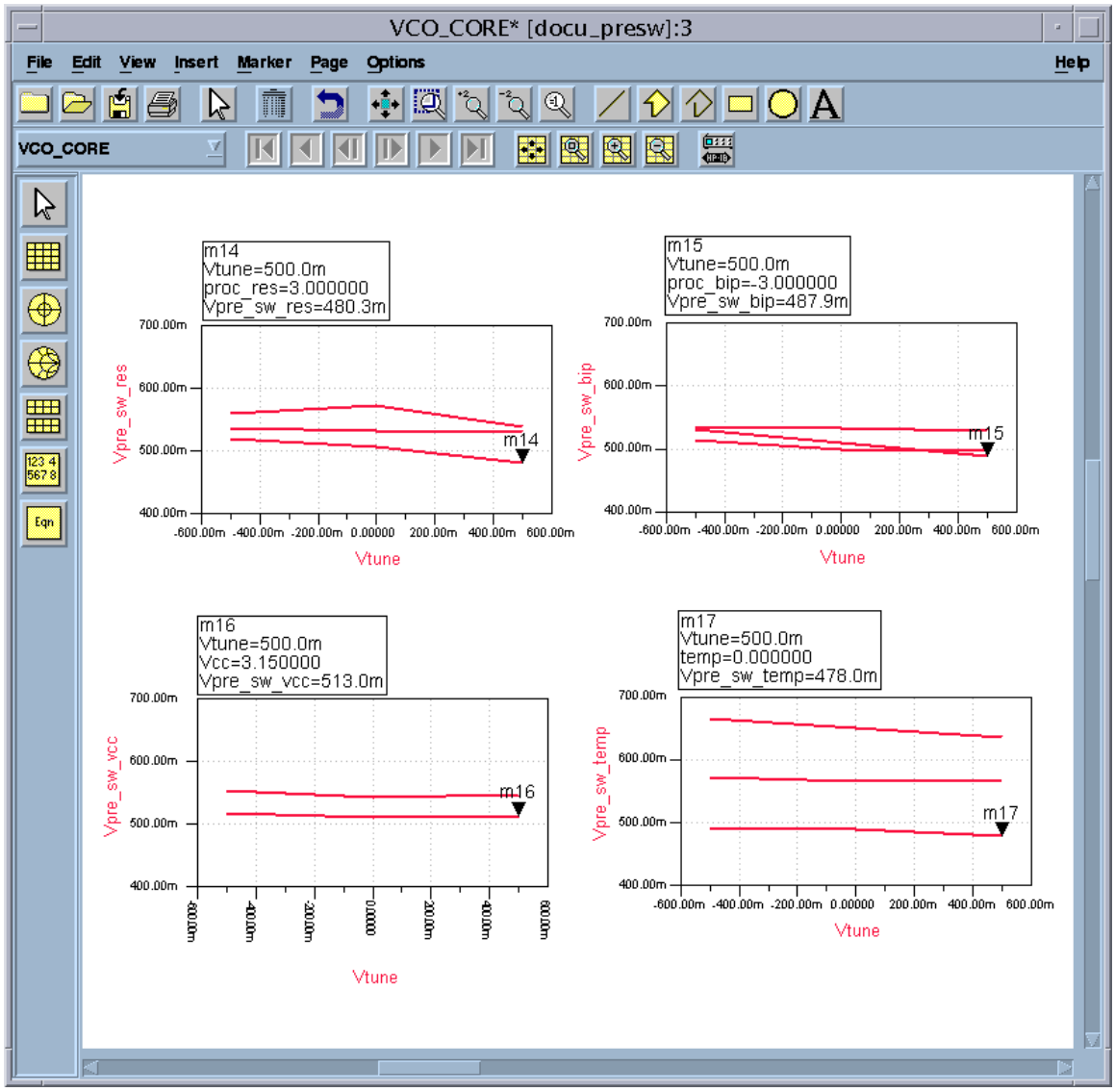
The small signal open loop gain of the VCO Core is about 5.5dB to ensure reliable start-up of oscillation. The start-up time of oscillation is 1.1nS as shown.



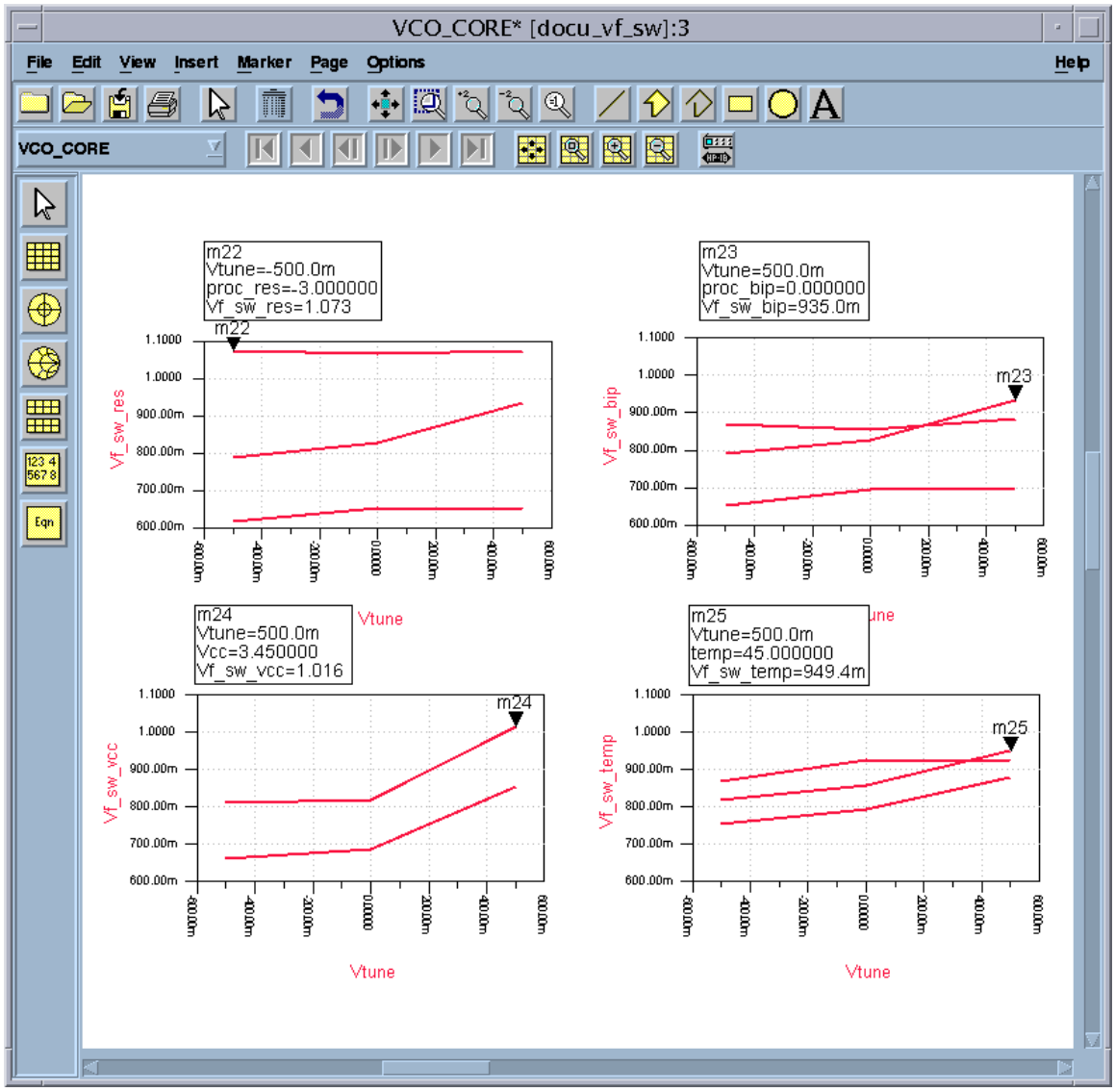
The sensitivities of tuning curves towards variations of process/supply/temperature are shown. The tuning curve is sensitive to process variation of BJT and Resistor.



The voltage amplitudes (differential, Vpeak-to-peak) at the output of Isolation Buffer, under variations of process/supply/temperature are shown. The amplitude is >480mVpp differentially, enough to drive the PD when VCO and PD are integrated into the same dice.



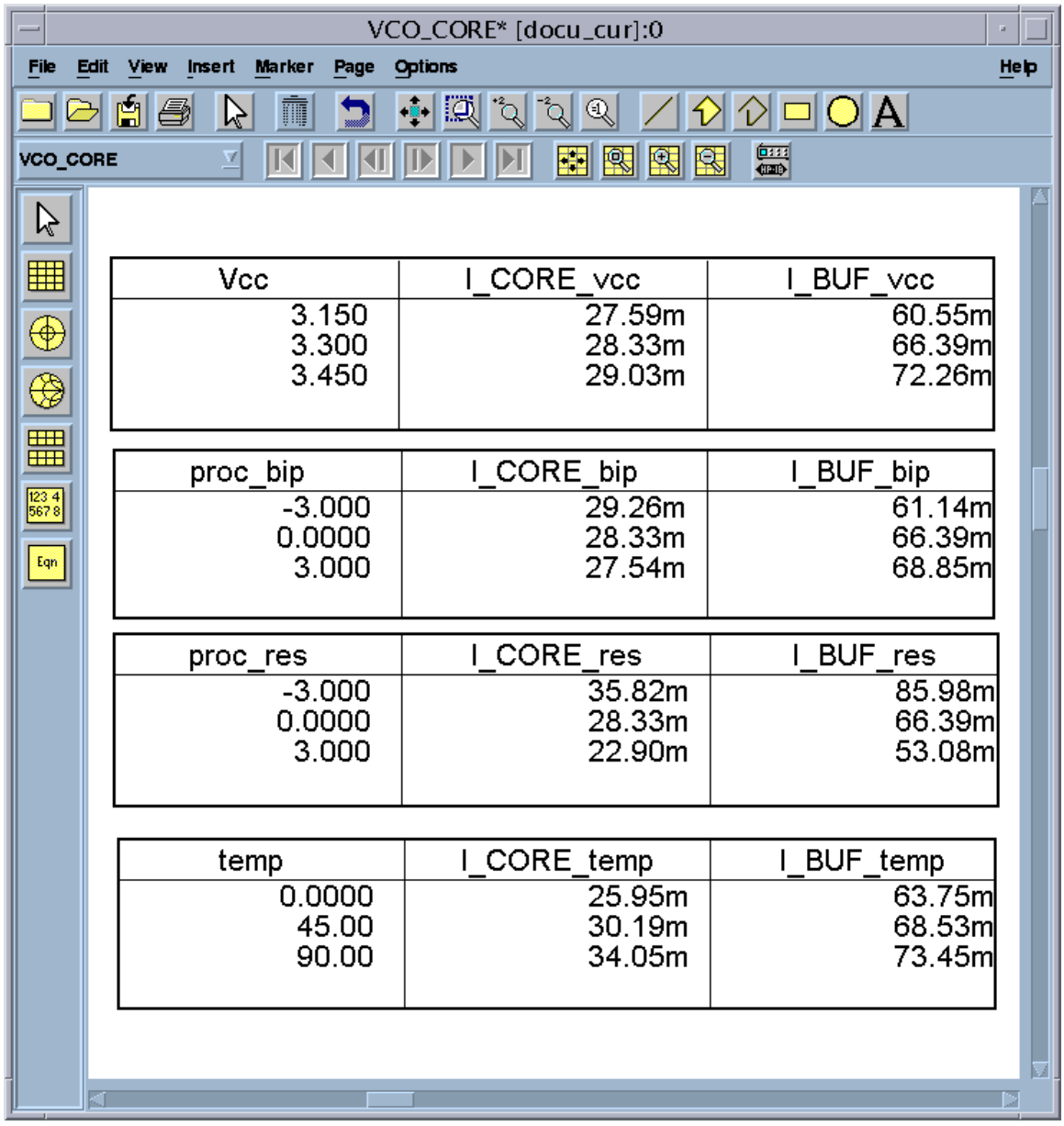
The voltage amplitudes (differential, Vpp) at the output of External Buffer, under variations of process/supply/temperature are shown. The amplitude is >600mVpp differentially, enough to drive external 50Ω transmission line and test instrument for testing. The high amplitude is also sufficient to drive PD, which is in another package, if needed.



The current consumption, under variations of process/supply/temperature is shown shown.

I_CORE_xx is the current consumption of VCO Core, Isolation Buffer and PTAT Current Reference. It is typically 28.33mA.

I_BUF_xx is the current consumption of External Buffer and Simple Current Reference. It is typically 66.39mA. When VCO and PD are integrated into one dice, External Buffer is not required.



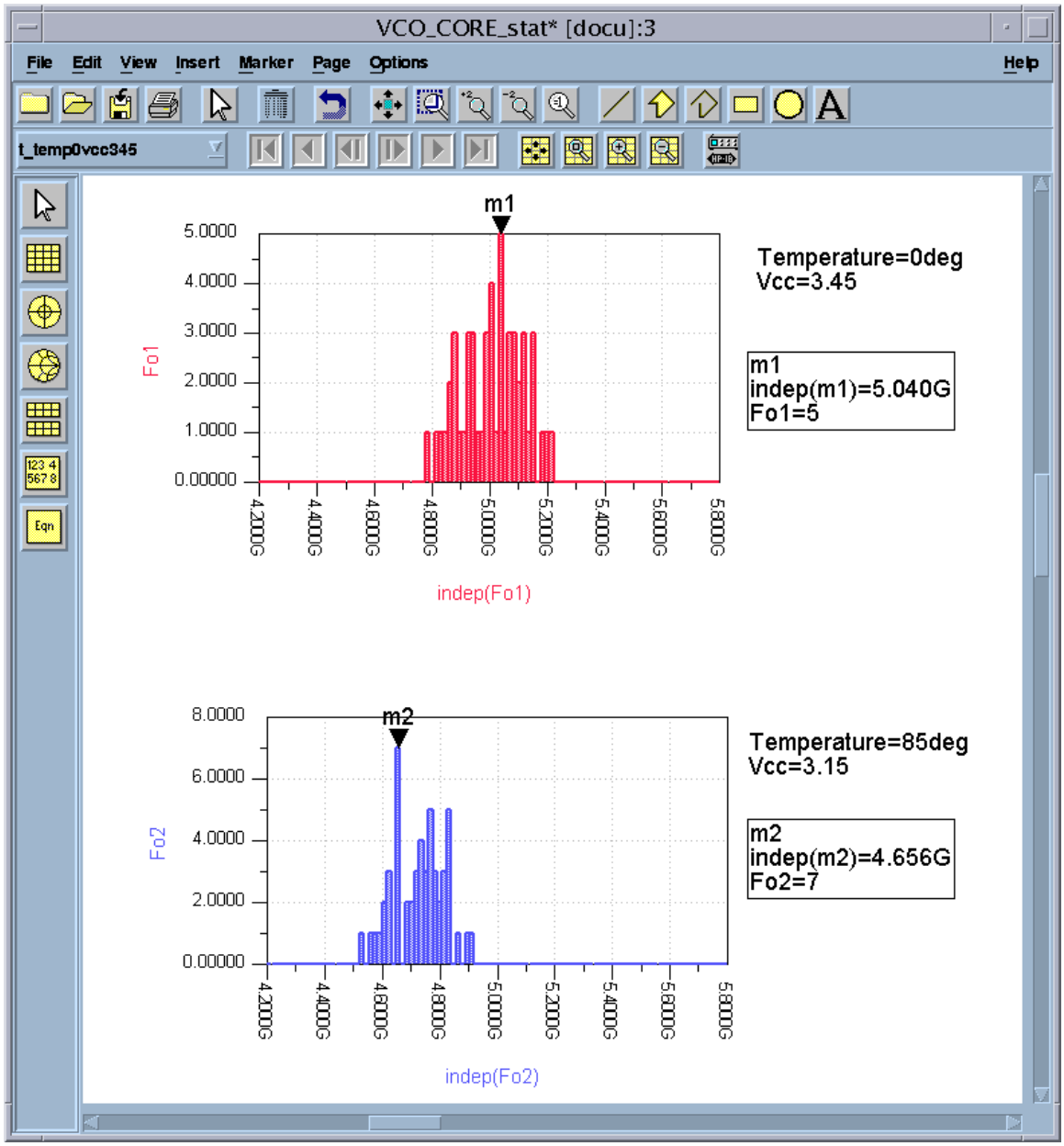
Vcc	I_CORE_vcc	I_BUF_vcc
3.150	27.59m	60.55m
3.300	28.33m	66.39m
3.450	29.03m	72.26m

proc_bip	I_CORE_bip	I_BUF_bip
-3.000	29.26m	61.14m
0.0000	28.33m	66.39m
3.000	27.54m	68.85m

proc_res	I_CORE_res	I_BUF_res
-3.000	35.82m	85.98m
0.0000	28.33m	66.39m
3.000	22.90m	53.08m

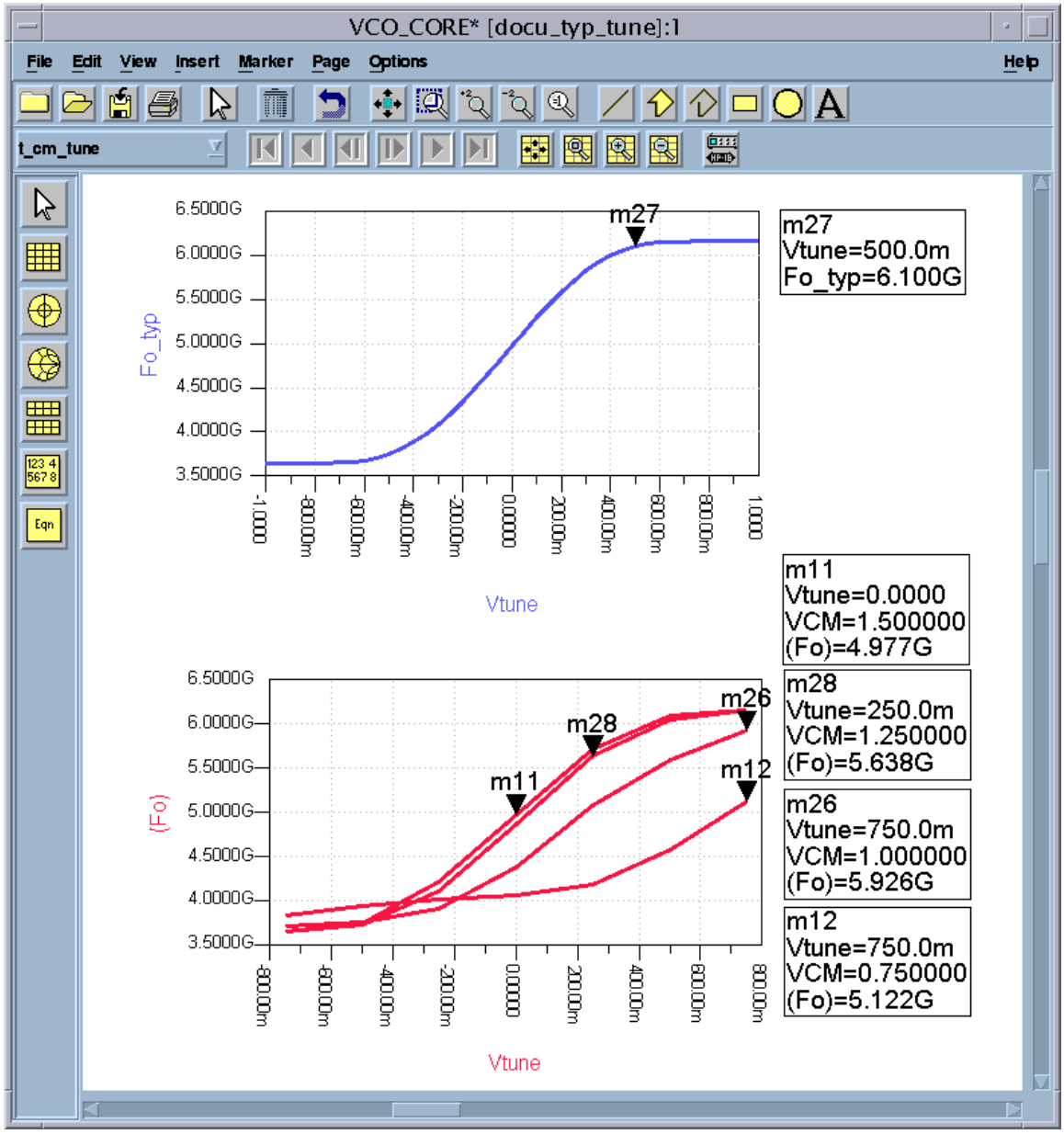
temp	I_CORE_temp	I_BUF_temp
0.0000	25.95m	63.75m
45.00	30.19m	68.53m
90.00	34.05m	73.45m

The following plots show the result of Monte Carlo Analysis. Number of trials run is 50. Temperature of 0°C at Vcc=3.45V and Temperature of 85°C at Vcc=3.15V are simulated. These two conditions represent the two extreme conditions of Fosc due to temperature and supply. As can be seen, the spreads are less than 1GHz and it will be safely covered by the typically 2GHz tuning range.



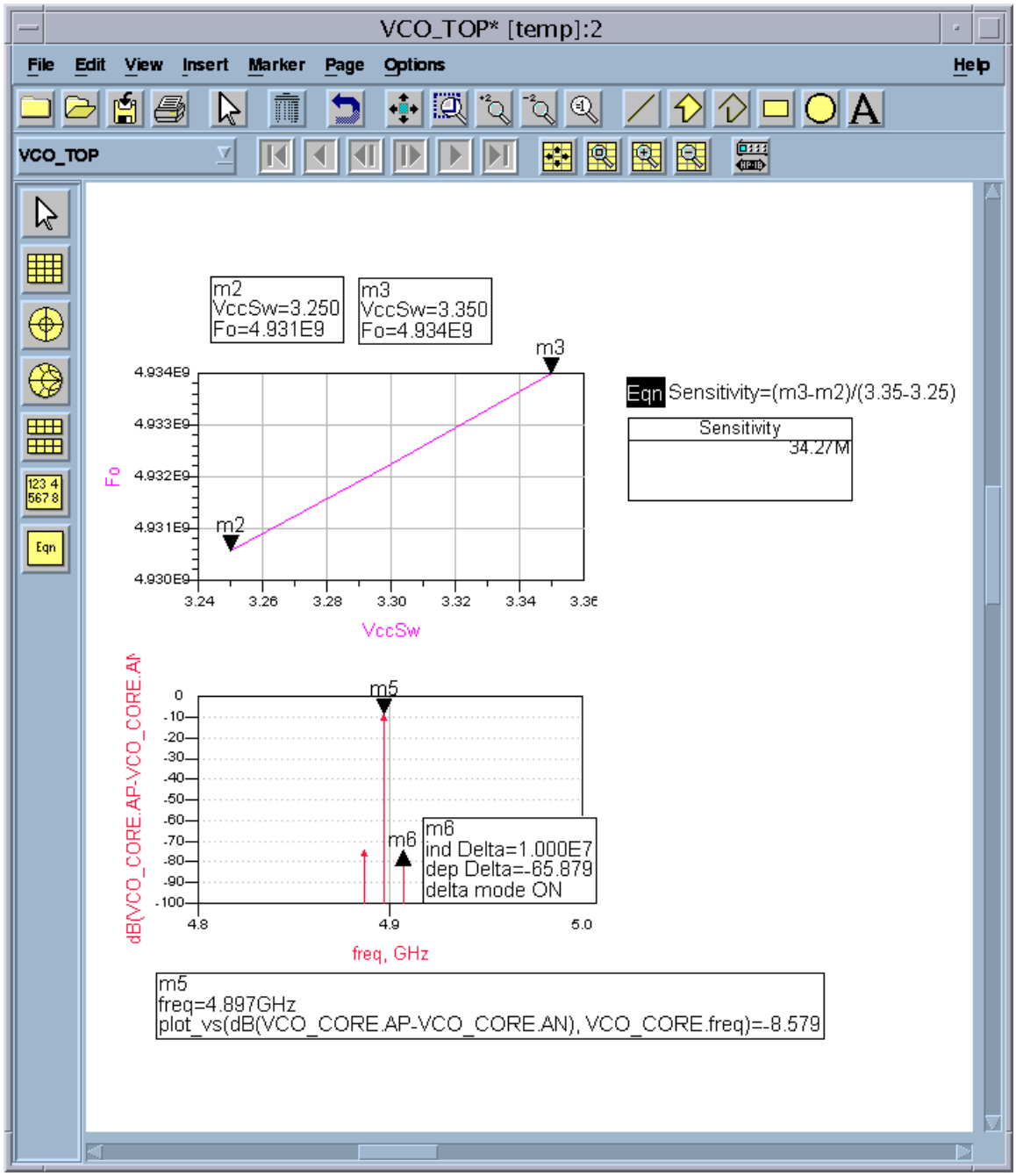
The tuning curve at typical condition is shown. The tuning voltage range is differentially from –1V to +1V. The tuning of VCO is done differentially with two complementary signal – TUNE_UP and TUNE_DN. For example, at marker m27, with common mode voltage of VCM=1.5V, TUNE_UP=2V, TUNE_DN=1V, Fosc=6.1GHz as shown. Hence, differential tuning voltage of +1V will give Fosc=6.1GHz.

The input common mode voltage of Vtune must be >1.5V for correct operation. The Charge Pump has to ensure that under normal operating condition, VCM>1.5V. The four traces in the bottom plot show the effect of VCM on tuning curve.



The power supply of PTAT current reference was varied by 100mV and the sensitivity of Fosc to supply was founded to be about 34MHz/V. This is considered low as compared to the 2GHz/V tuning sensitivity at the tuning port.

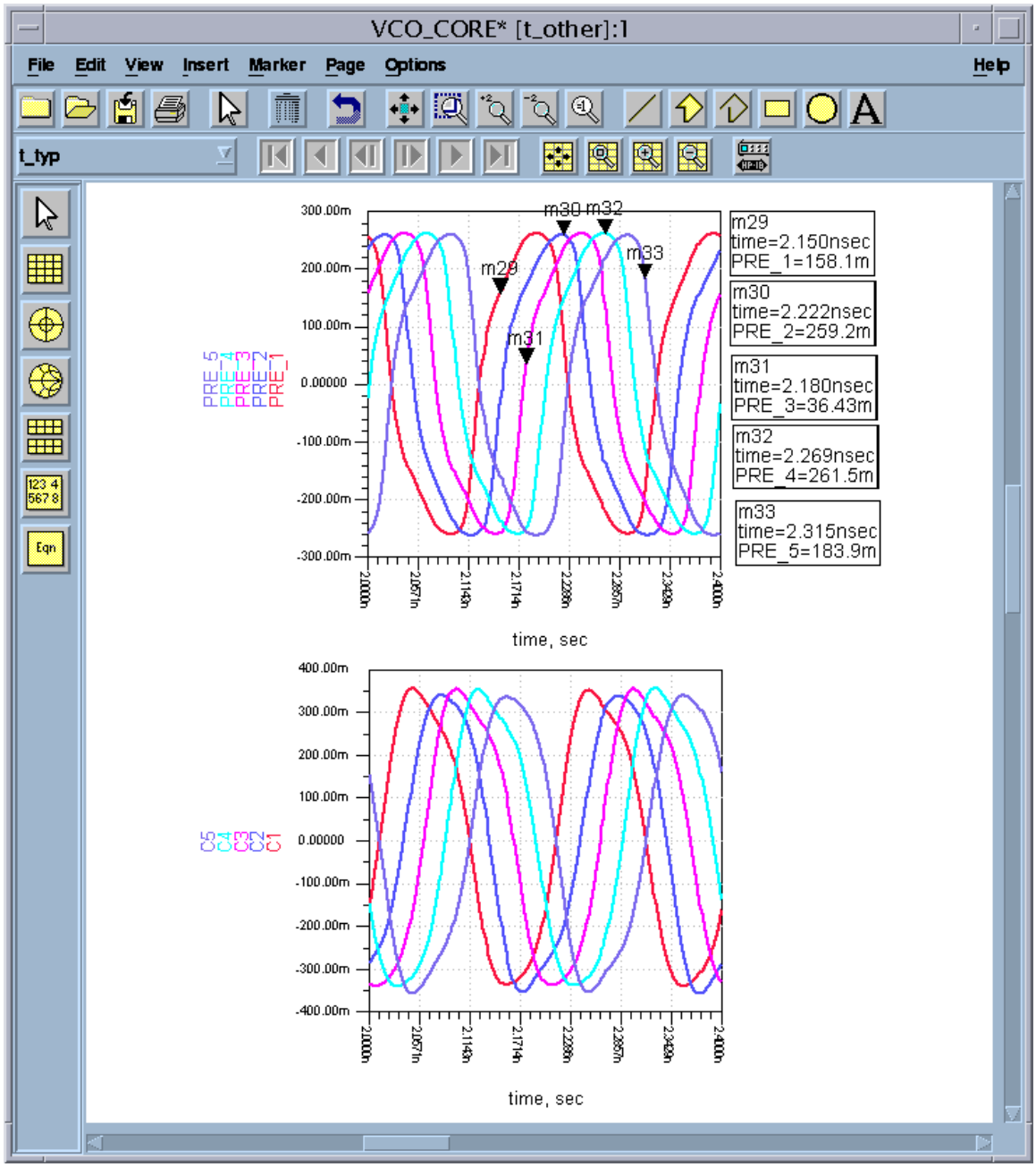
An Harmonic Analysis was also performed by connecting a 10mV, 10MHz sine wave to the power supply of PTAT current reference. As can be seen from the plot, -65dBc of spurious response resulted. This is low enough and it will not affect the noise performance of the CDR. Good decoupling practice on-chip will help prevent supply noise variation from exceeding 10mV. The critical issue is that the noise at tuning port, which has a high sensitivity of 2GHz/V, has to be kept very low.



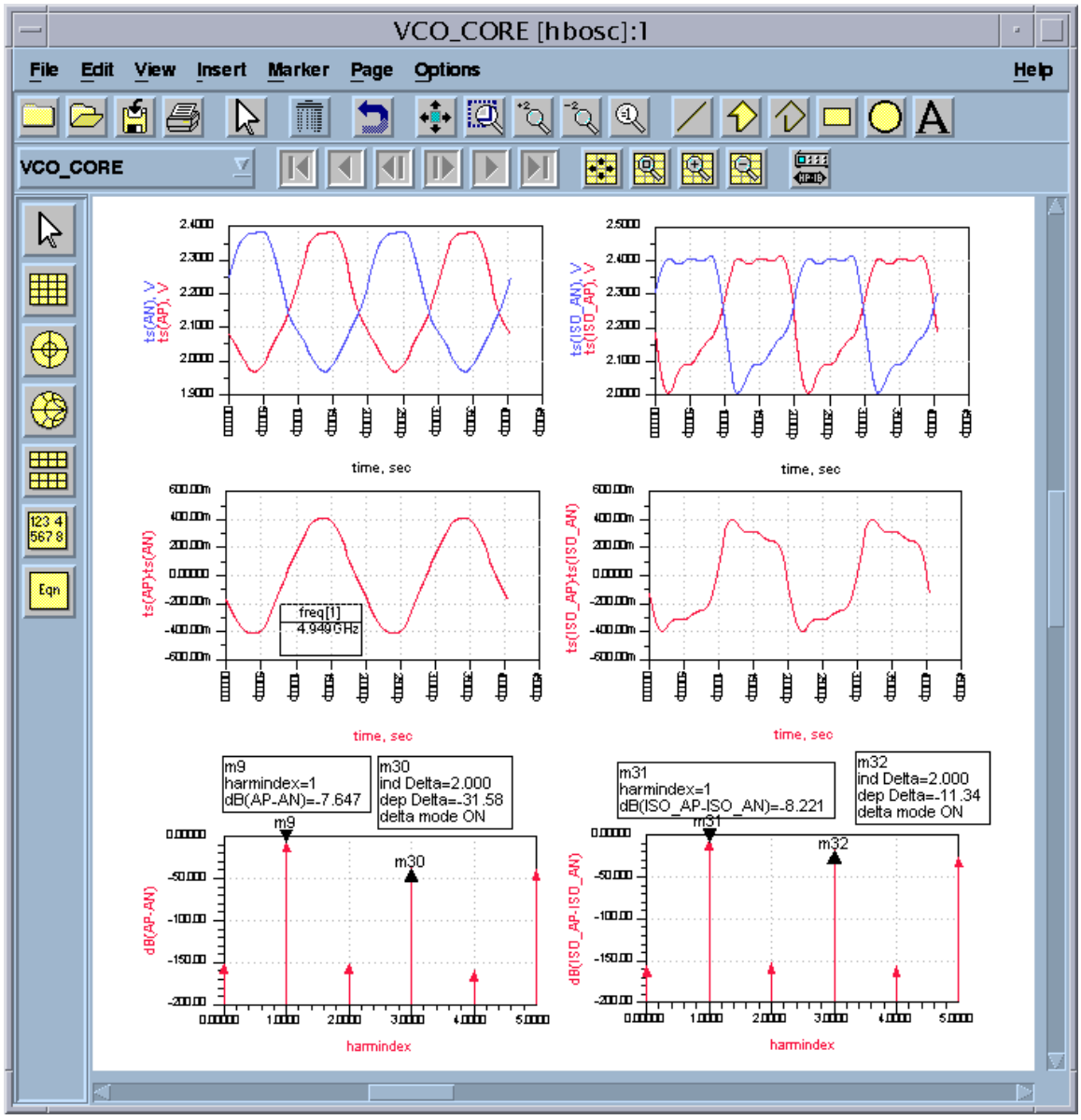
The five clock phases required by the PD are shown.

PRE_1 to PRE_5 are the waveform at the output of Isolation Buffers. C1 to C5 are the waveform at the output of External Buffers.

As shown by the markers, PRE_1 is leading PRE_2 by 45°. In other words, PRE_2 come later than PRE_1.



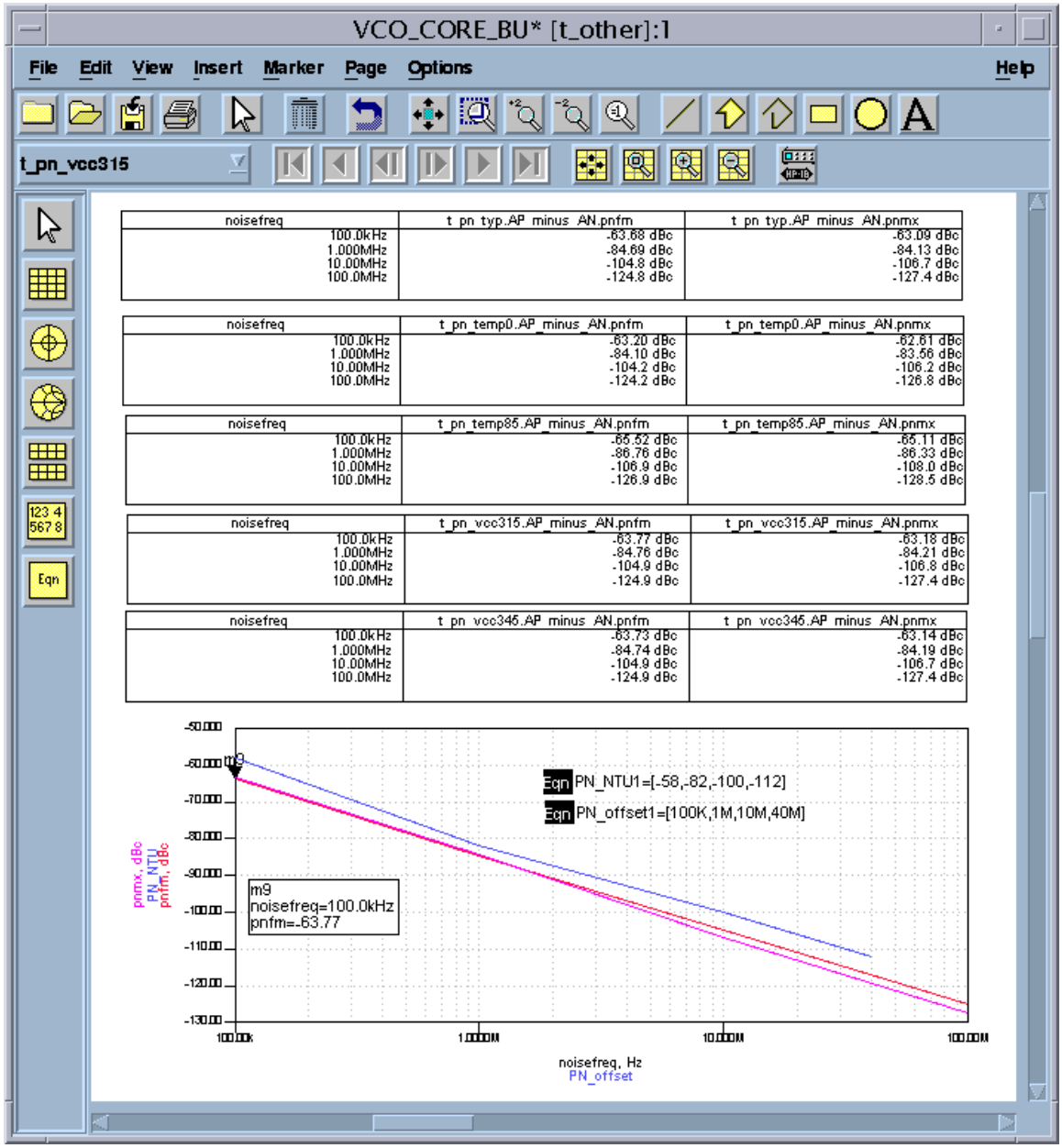
Harmonic Balance is run and the results for a typical operating condition are shown. AP & AN is the waveform at the VCO Core whereas ISO_AP & ISO_AN is the waveform at the Isolation Buffer. Their differential waveforms are also shown. Their 3rd harmonic are –31dBc and –11dBc respectively.



The phase noise performance is shown. Five cases are simulated.

T_pn_typ	Vcc=3.3, Temperature=25
T_pn_temp0	Vcc=3.3, Temperature=0
T_pn_temp85	Vcc=3.3, Temperature=85
T_pn_vcc315	Vcc=3.15, Temperature=25
T_pn_vcc345	Vcc=3.45, Temperature=25

The phase noise should be read by taking the worst of .pnfm and .pnmx at each offset frequency. The phase noise is generally below that specified in NTU report with a margin of about 3 to 6dB.



noisefreq	t_pn_typ.AP_minus_AN.pnfm	t_pn_typ.AP_minus_AN.pnmx
100.0kHz	-63.68 dBc	-63.09 dBc
1.000MHz	-84.69 dBc	-84.13 dBc
10.00MHz	-104.8 dBc	-106.7 dBc
100.0MHz	-124.8 dBc	-127.4 dBc

noisefreq	t_pn_temp0.AP_minus_AN.pnfm	t_pn_temp0.AP_minus_AN.pnmx
100.0kHz	-63.20 dBc	-62.61 dBc
1.000MHz	-84.10 dBc	-83.56 dBc
10.00MHz	-104.2 dBc	-106.2 dBc
100.0MHz	-124.2 dBc	-126.8 dBc

noisefreq	t_pn_temp85.AP_minus_AN.pnfm	t_pn_temp85.AP_minus_AN.pnmx
100.0kHz	-65.52 dBc	-65.11 dBc
1.000MHz	-86.76 dBc	-86.33 dBc
10.00MHz	-106.9 dBc	-108.0 dBc
100.0MHz	-126.9 dBc	-128.5 dBc

noisefreq	t_pn_vcc315.AP_minus_AN.pnfm	t_pn_vcc315.AP_minus_AN.pnmx
100.0kHz	-63.77 dBc	-63.18 dBc
1.000MHz	-84.76 dBc	-84.21 dBc
10.00MHz	-104.9 dBc	-106.8 dBc
100.0MHz	-124.9 dBc	-127.4 dBc

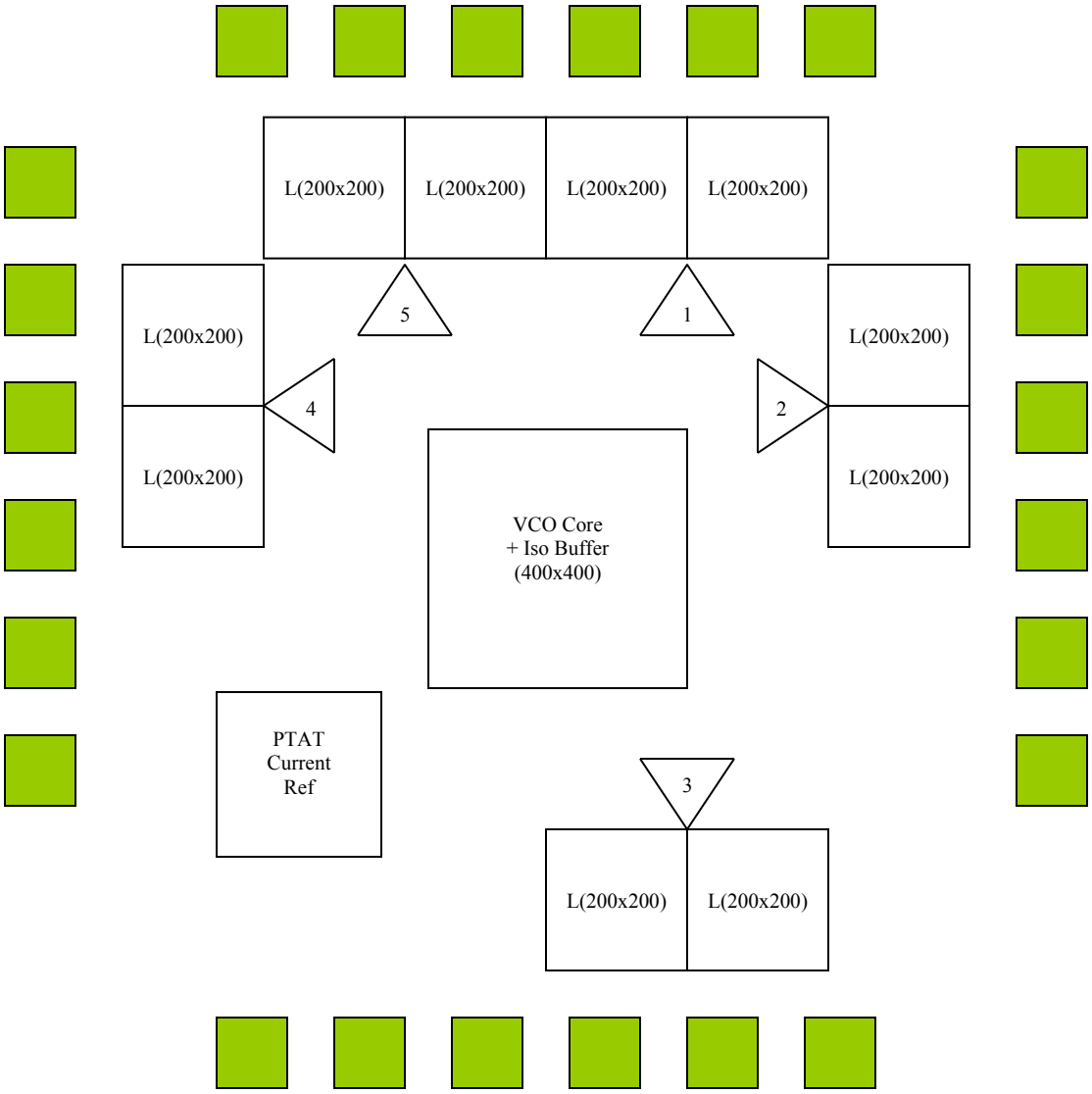
noisefreq	t_pn_vcc345.AP_minus_AN.pnfm	t_pn_vcc345.AP_minus_AN.pnmx
100.0kHz	-63.73 dBc	-63.14 dBc
1.000MHz	-84.74 dBc	-84.19 dBc
10.00MHz	-104.9 dBc	-106.7 dBc
100.0MHz	-124.9 dBc	-127.4 dBc

6 Layout

To maintain the correct 5 phases as required by PD, the layout must be symmetrical. There are a total of 10 inductors used in the final driver for inductive peaking. This enhances the slew rate of VCO signal as required by PD.

The layout of VCO will be inductors limited as each inductor size is about 200um by 200um (included clearance as required for reduction of EMC).

Layout Plan: (1.6mm*1.6mm)



Layout Plan: VCO CORE.