Sigma-Delta Modulators for Fractional-N PLL

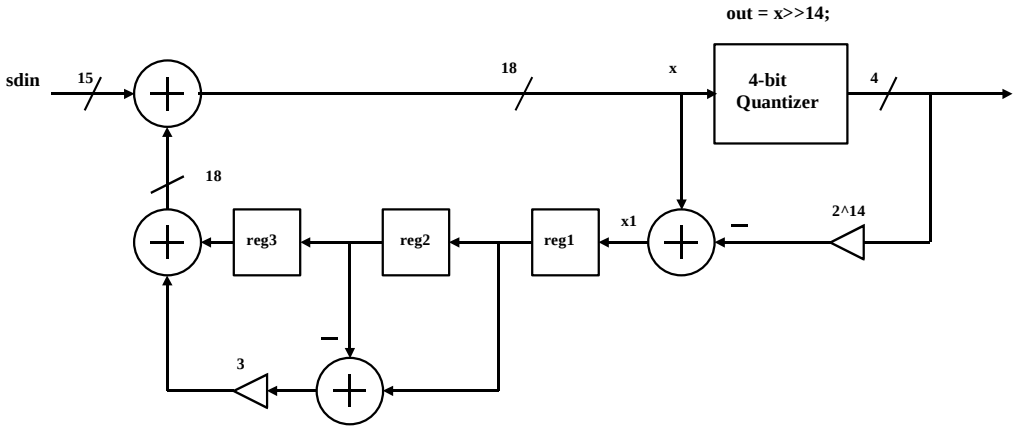
1. The 3rd-order 4-bit Output Sigma-Delta Modulator

1.1. C-code

```
x=sdin+((reg1-reg2)<<1)+(reg1-reg2)+reg3;
sdout=(x>>14);
x1=x-(sdout<<14);
reg3=reg2; reg2=reg1; reg1=x1;
```

Note: All above variables are defined as integer. Modulator input is *sdin*, which is a 15-bit 2's complement number. When it's positive full scale (011 1111 1111 1111), modulator output average is 1.0. When it's negative full scale (100 0000 0000 0000), modulator output average is –1.0. Modulator output is *sdout*.

1.2. Block Diagram



The 3rd-order 4-bit Output Sigma-Delta Modulator

2. The 2nd-order 3-level Output Sigma-Delta Modulator

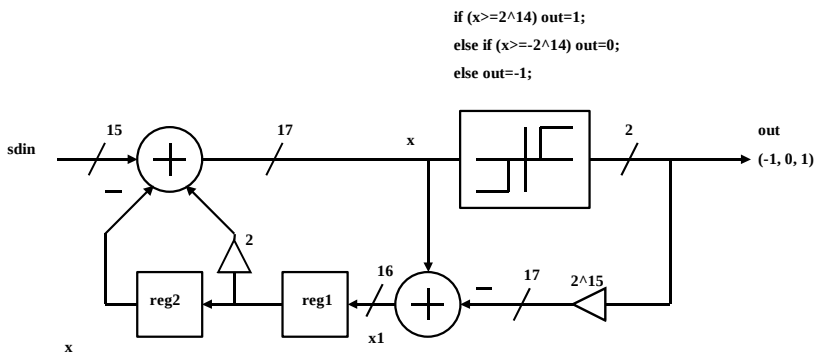
2.1. C-code

```
x=sdin+(reg1<<1)-reg2;
if (x>=(1<<14)) sdout=1;
```

```
else if (x>=-(1<<14)) sdout=0;
else sdout=-1;
x1=x-(sdout<<15);
reg2=reg1; reg1=x1;
```

Note: Modulator input is *sdin*, which is a 15-bit 2's complement number. When it's positive full scale (011 1111 1111 1111), modulator output average is 0.5. When it's negative full scale (100 0000 0000 0000), modulator output average is –0.5. Hence, when it's added with the integer dividing value, the PLL feedback divider can divide the input clock from (*N*-0.5) to (*N*+0.5), where *N* represents the integer dividing value. Modulator output is *sdout*.

2.2. Block Diagram



The 2nd-order 3-Level Output Sigma-Delta Modulator