Photoflash Charger
1st Tape Out
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Introduction

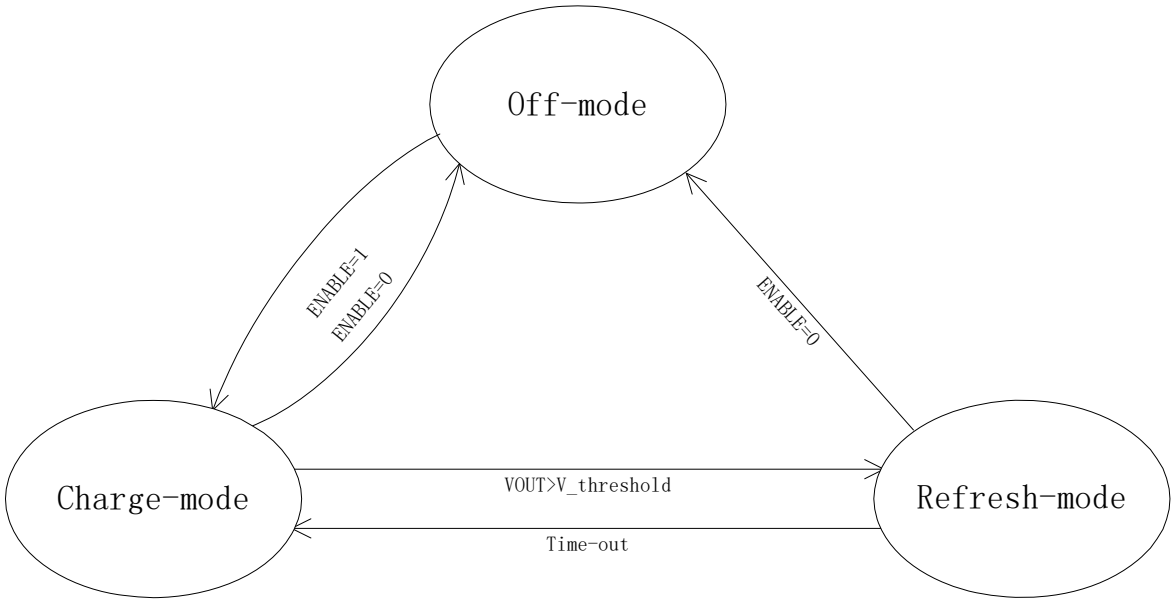
There are three modes of operation for the Photoflash Charger (**PFC**).

Charge Mode, Refresh Mode and Off Mode.

Mode	**ENABLE** (Control signal from DSC)	**READY** (Status signal to DSC)	Remarks
Off-mode	0	0	The PFC is shut-down.
Charge-mode	1	0	Vout < V_threshold. Charging circuit is on.
Refresh-mode	1	1	Timer is on. Charging circuit is off.

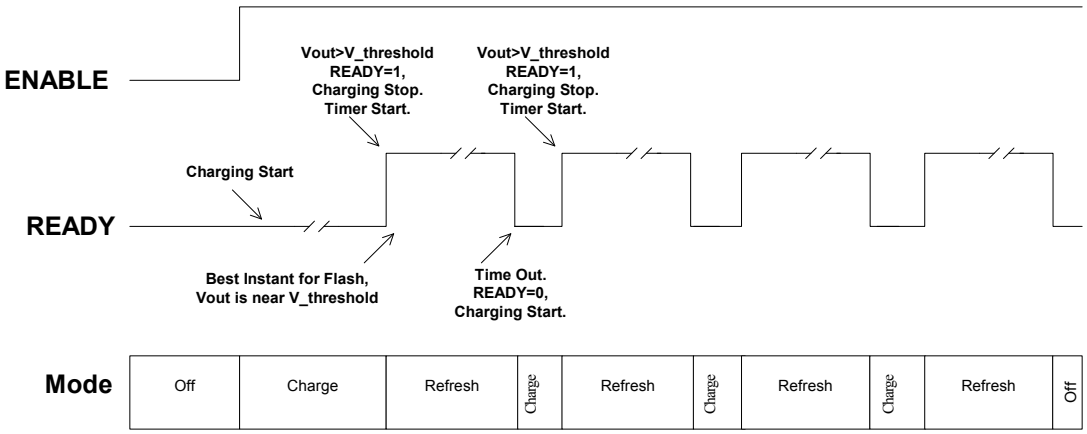
V_threshold is the targeted voltage level of photoflash capacitor.

The state transition diagram is shown.



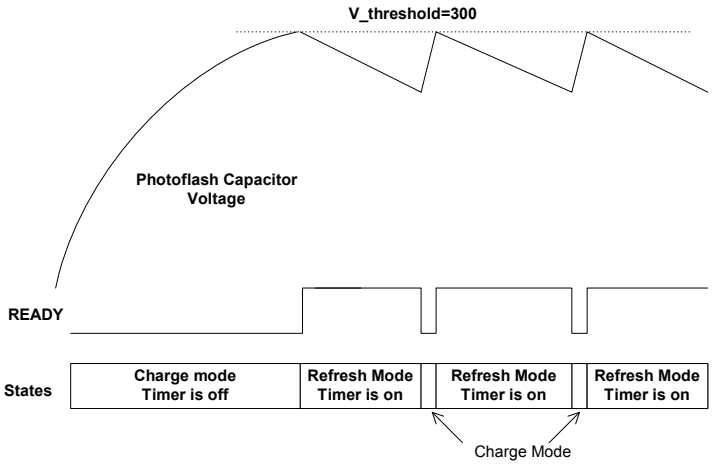
Timing Diagram

The timing diagram of photoflash charger is as shown:

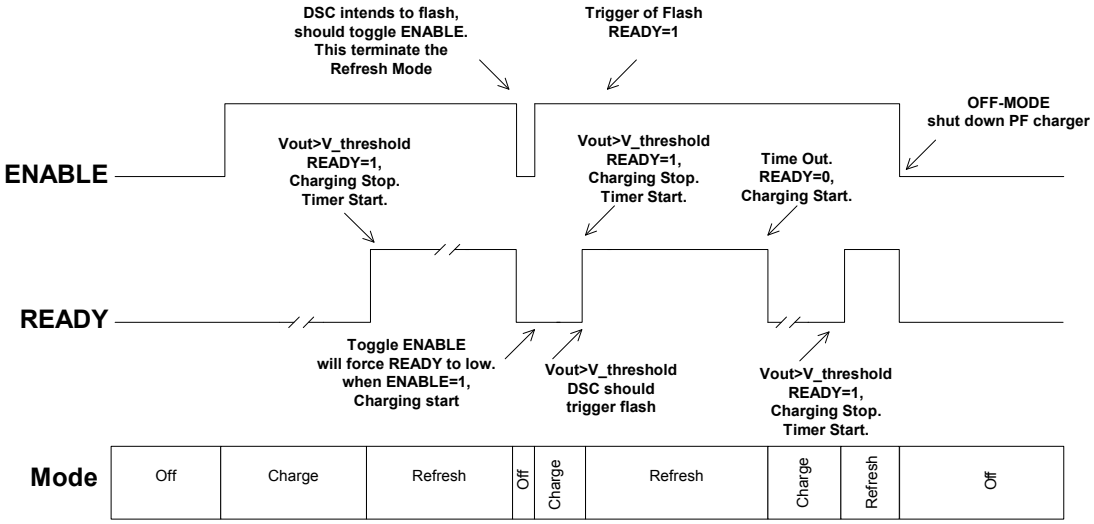


Photoflash Charger in Auto-Refresh Mode

Positive-edge of ENABLE commands PFC to exit Off Mode and enter Charge Mode. The positive-edge of READY means that V_threshold is reached and PFC enters Refresh Mode. In Refresh Mode, there is no charging activity and VOUT will droop due to the leakage of capacitor.



DSC should trigger flash immediately after the positive-edge of READY, before VOUT droops away from V_threshold.



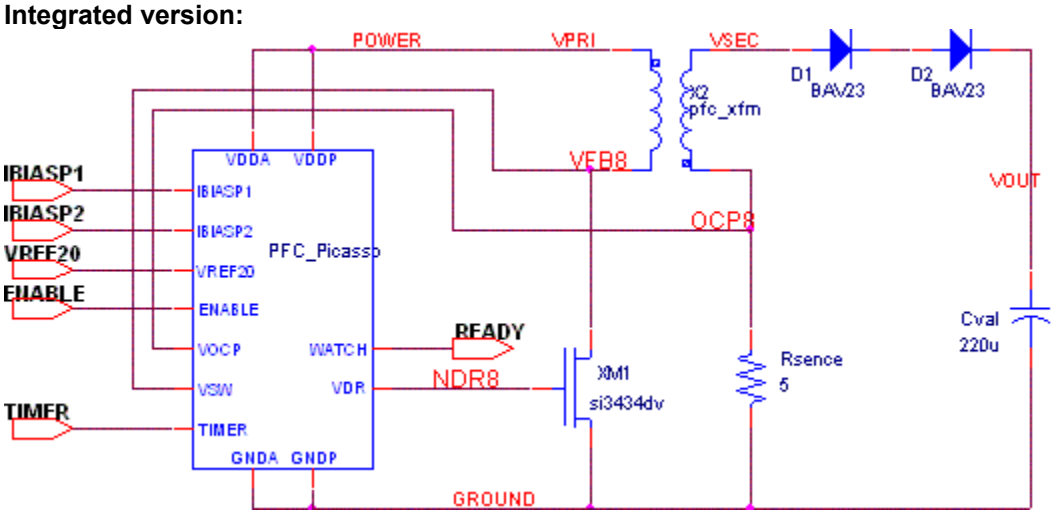
Photoflash Charger in Flash Events

During Refresh Mode, DSC can wait for the next positive-edge of READY to trigger the flash. Alternatively, DSC can toggle ENABLE to force a mode transitions from Refresh Mode → Off Mode → Charge Mode. In Charge-mode, VOUT will be charged towards V_threshold. This will save some time as compared to remain in Refresh Mode and wait for Charge Mode to come.

Application Circuit

The application circuit of PFC is shown:

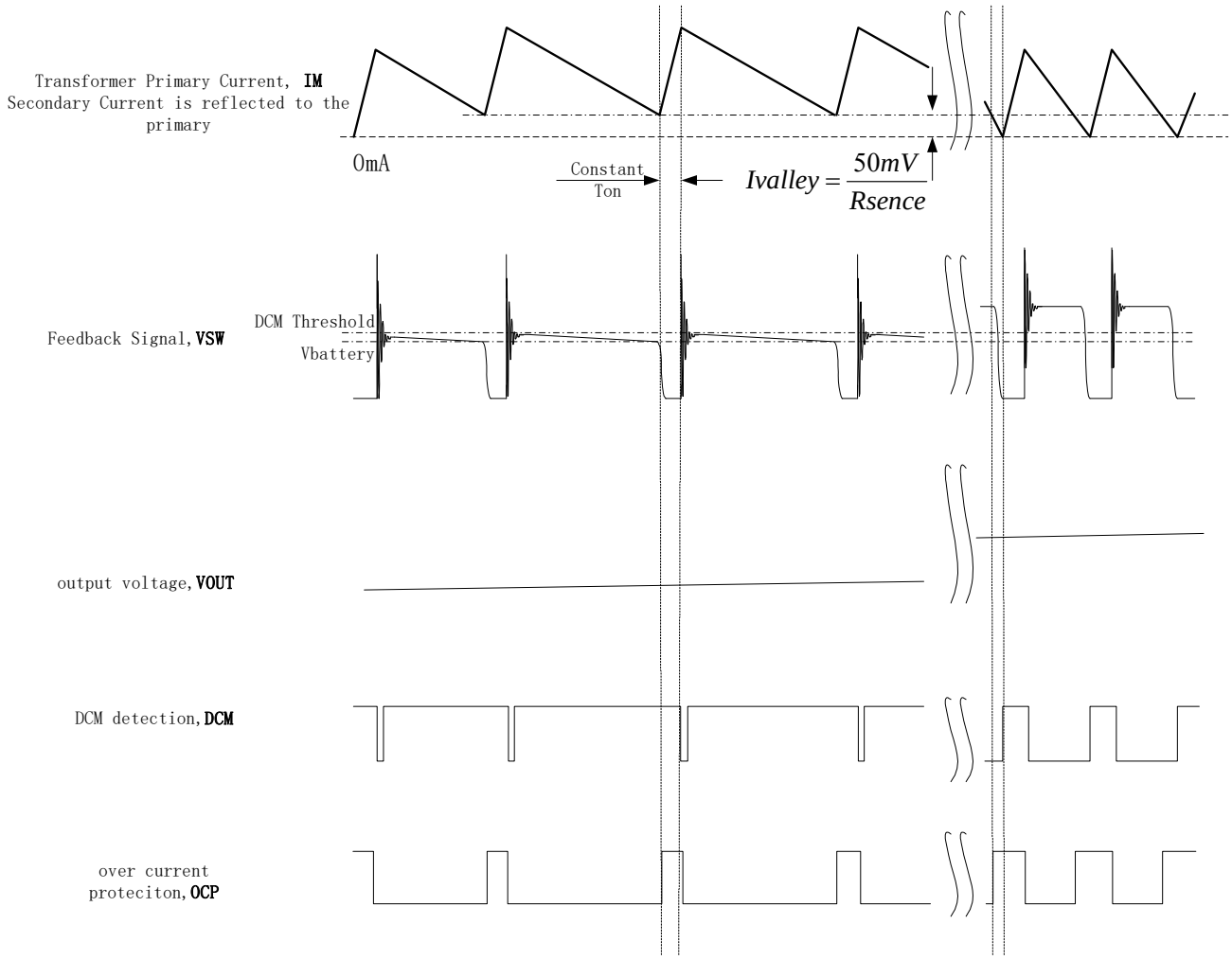
Integrated version:



The targeted photoflash capacitor voltage is designed by using the turn ratio of transformer.

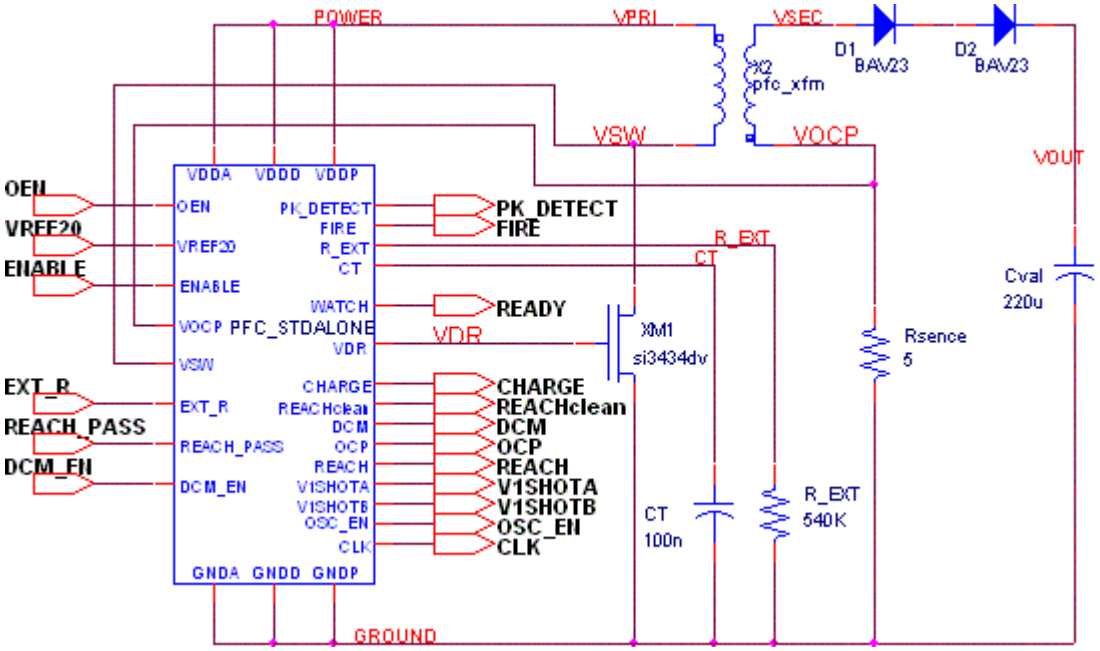
$$N = \frac{Vout}{15}$$

Secondary Sense Resistor:
This resistor is used to detect secondary current. New switching cycle can only begin after the secondary current is less than $\frac{Voffset\_ocp}{Rsence}$. The design Voffset_ocp is about 50mV. The over-current protection is valley type.



In the beginning when VSW is less than DCM Threshold, over current protection is required to limit the current. If the design peak transformer current is Ipeak, then in the beginning, the peak transformer current is Ipeak+Ivallay.

Standalone version:



System Design Equation

$$\text{Ipeak} = \frac{\text{Tset}}{\text{Lmag}}$$

$$\text{Ton} = \frac{\text{Tset}}{\text{Vbat}}$$

Ipeak is the peak current flowing through the primary of transformer and switch. Lmag is the magnetizing inductance of the transformer.

For the Picasso version, internal resistor is used to set the Tset.

$$\text{Tset} = \text{Rint} * \text{C} * \Delta\text{V} = 10us$$

The expected variation is about ±30% (extreme case) according to the simulation.

For the standalone version, external resistor is used to facilitate testing.

$$\text{Tset} = 0.0171n \times (\text{Re}\,xt + 44.4K)$$

$$\text{Re}\,xt = 58.5G \times Tset - 44.4K$$

The expected variation of Tset is about ±5% according to the simulation.

The maximum average current occurs when Vout is near the targeted capacitor voltage, when the duty cycle of switching waveform is at its maximum. The duty cycle of the switching waveform varies proportionally to Vout.

$$\text{I}_{\text{IN\_AVG}} = 0.5 \times \text{Ipeak} \times \frac{\text{Ton}}{\text{Ton} + \text{Toff}}$$

$$= 0.5 \times \text{Ipeak} \times \frac{\text{Vout}}{\text{Vout} + \text{N} \times \text{Vbat}}$$

$$= 0.5 \times \text{Ipeak} \times \frac{\text{Vout}/\text{N}}{\text{Vout}/\text{N} + \text{Vbat}}$$

Vbat	Iin_avg	Pin_avg=Iin_avg*Vbat	Remarks
2.8V	0.421A	1.179W	Assume Ipeak=1A, Vout=300V, N=20
3.7V	0.401A	1.484W	
4.2V	0.390A	1.638W	
2.8V	0.320A	0.896W	Assume Ipeak=1A, Vout=100V, N=20
3.7V	0.287A	1.062W	
4.2V	0.272A	1.142W	
2.8V	0.075A	0.210W	Assume Ipeak=1A, Vout=10V, N=20
3.7V	0.059A	0.218W	
4.2V	0.053A	0.226W	

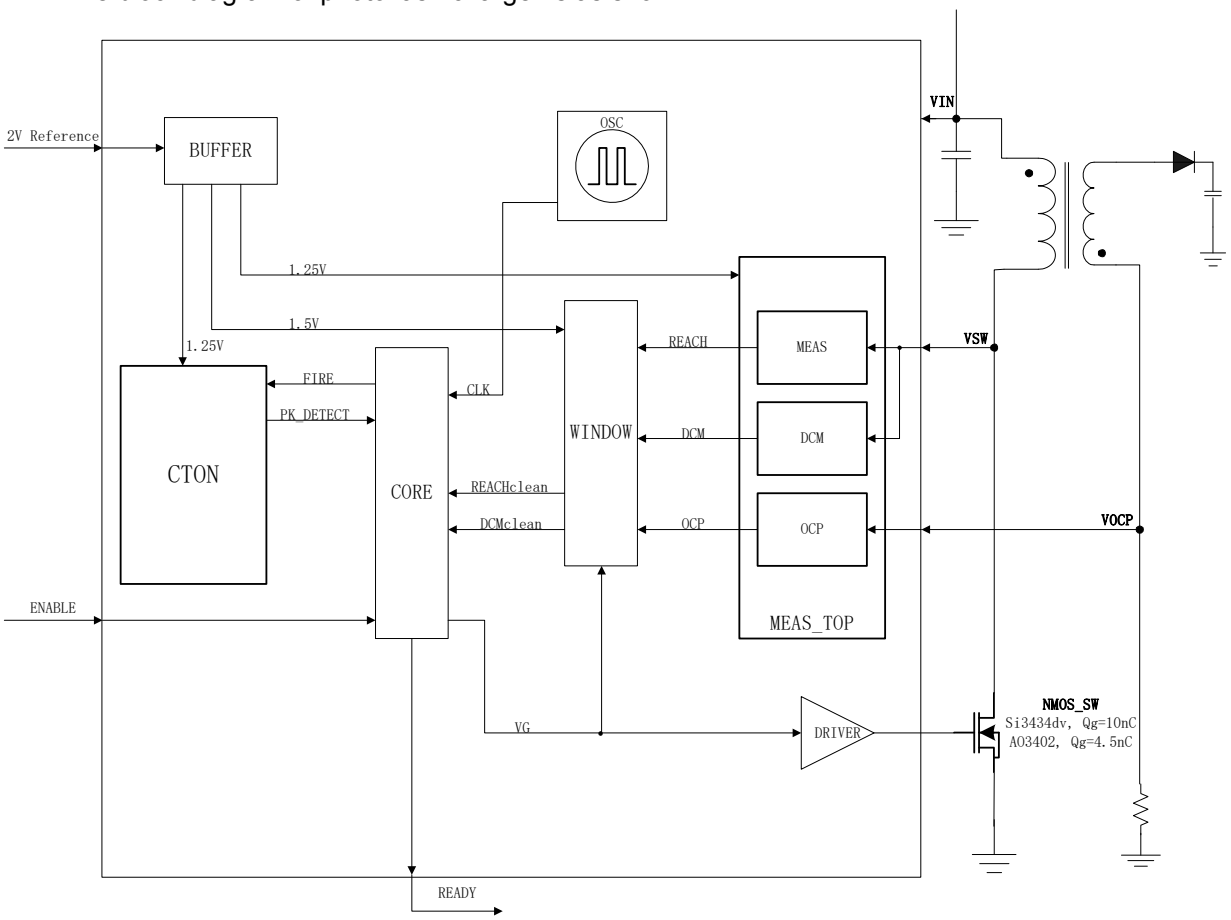
Capacitor for Timer:
This capacitor sets the refresh time.

$Trefresh=1.06Ct \times 10^{6}$

$Ct = 0.945 \times 10^{-6} \times Trefresh$

System Block Diagram

The block diagram of photoflash charger is as shown:



The function of various sub-circuit are explained:

PFC_BUFFER

This block accept an accurate 2V reference from Picasso and distribute various voltage reference required by PFC.

PFC_DRIVER

This is the pre-driver for the external power MOSFET.

PFC_OSC

It is used to generate a delay of about 190 us.

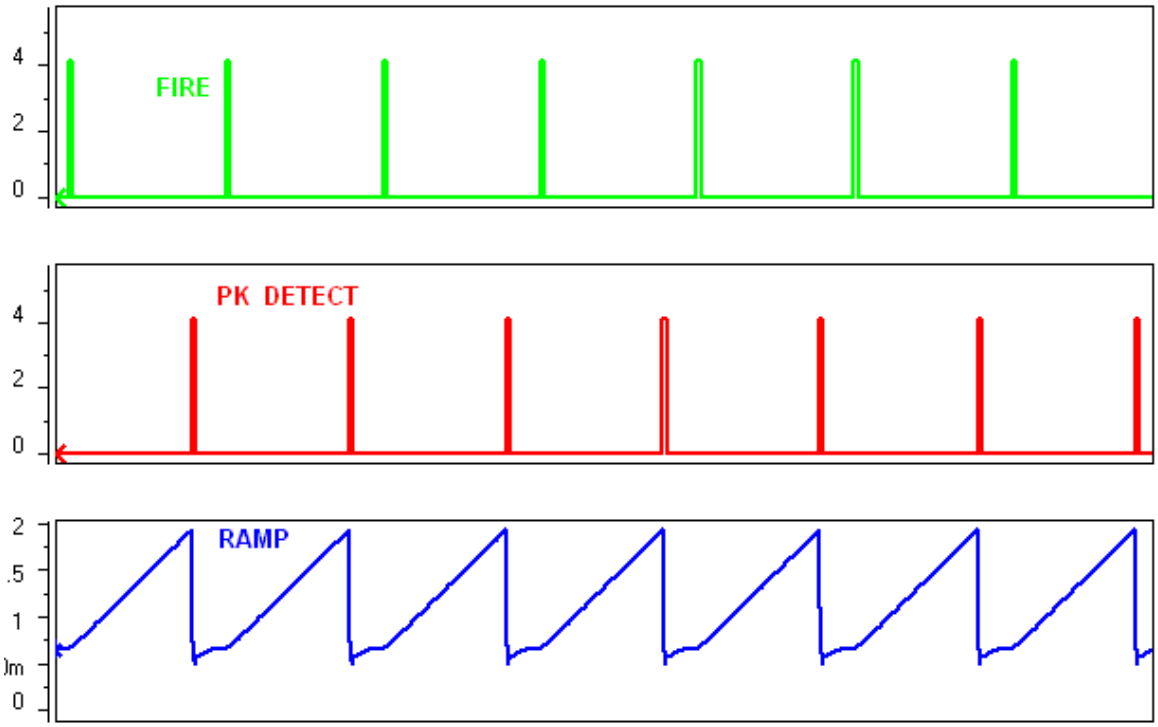
PFC_CTON

It is to produce a Ton pulse base on the following equation.

$$Ton = \frac{Ipeak * Lpri}{Vbattery}$$

Ipeak is the designed peak current flowing through external NMOS switch when it is on. Ipeak should be some margin away from maximum current rating of transistor and transformer. The designed Ipeak will have some tolerance due to variation of Lpri and Ton.

Fire and PK_detect and ramp voltage is shown:



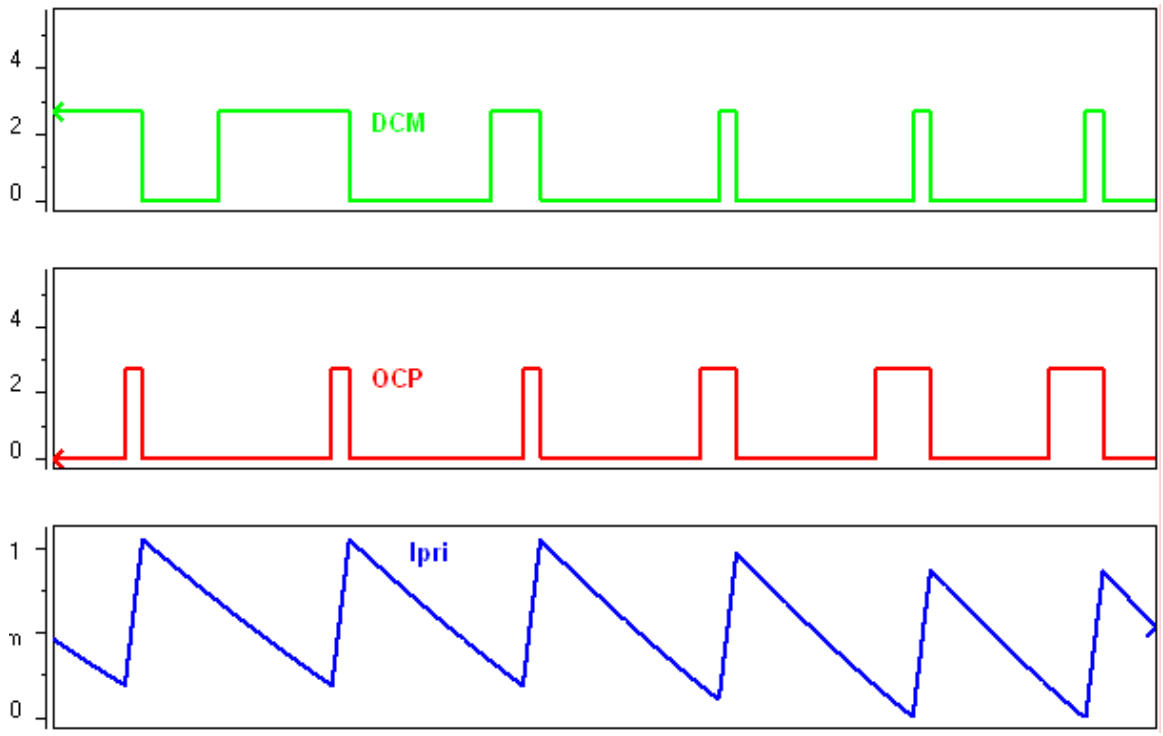
Fire will turn on the switch and PK_DETET will turn off the switch, Interval between FIRE and PK_DETECT is the constant Ton time.

PFC_MEAS_TOP

This block contains three measurement circuits with the following function:

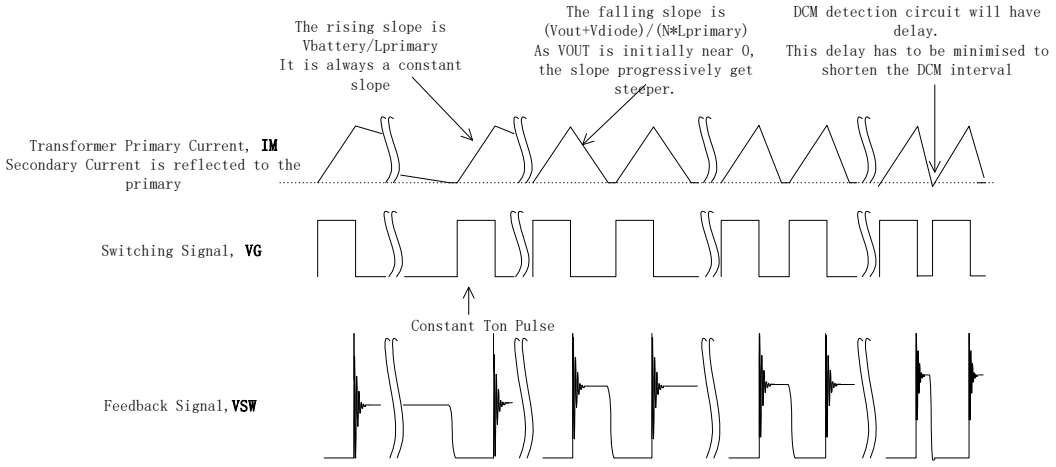
PFC_MEAS
This is to measure the VOUT through the primary coil of transformer. Charging is completed when the flyback voltage is equal to 15V.

PFC_OCP
This is the over-current protection of PFC. When the secondary current is less than certain level, OCP=1.
Rsence = 50mV/Iset_ocp

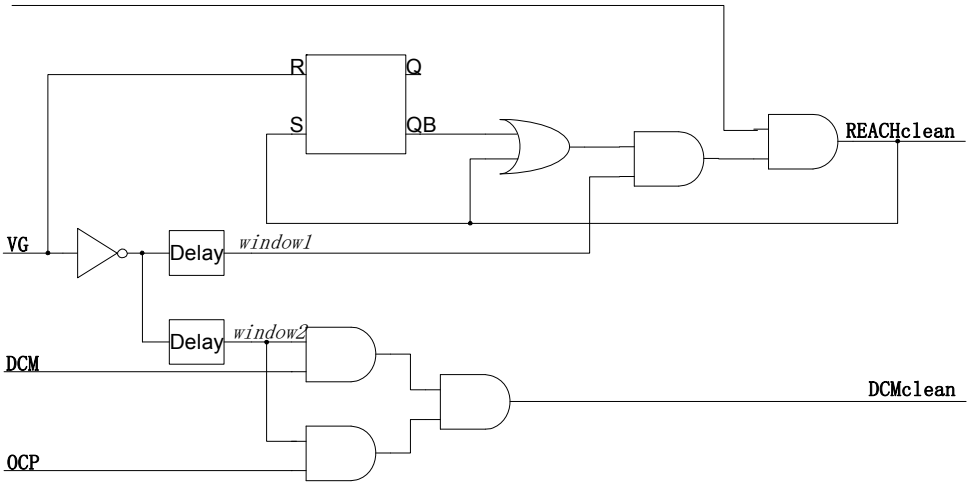


PFC_DCM
This is the DCM detection circuit. When VSW is less than [Vbattery+500mV], DCM is detected. A constant Ton pulse is fired only when DCM is detected and OCP=1.

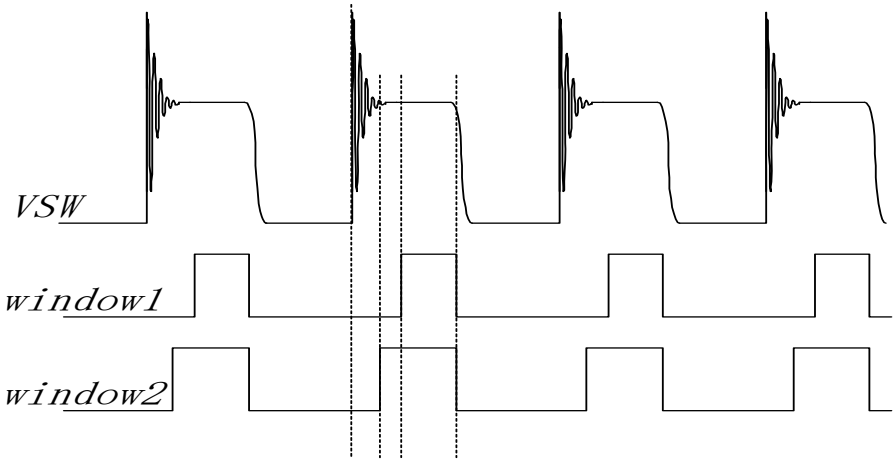
VSW, VG and transformer current are as shown.



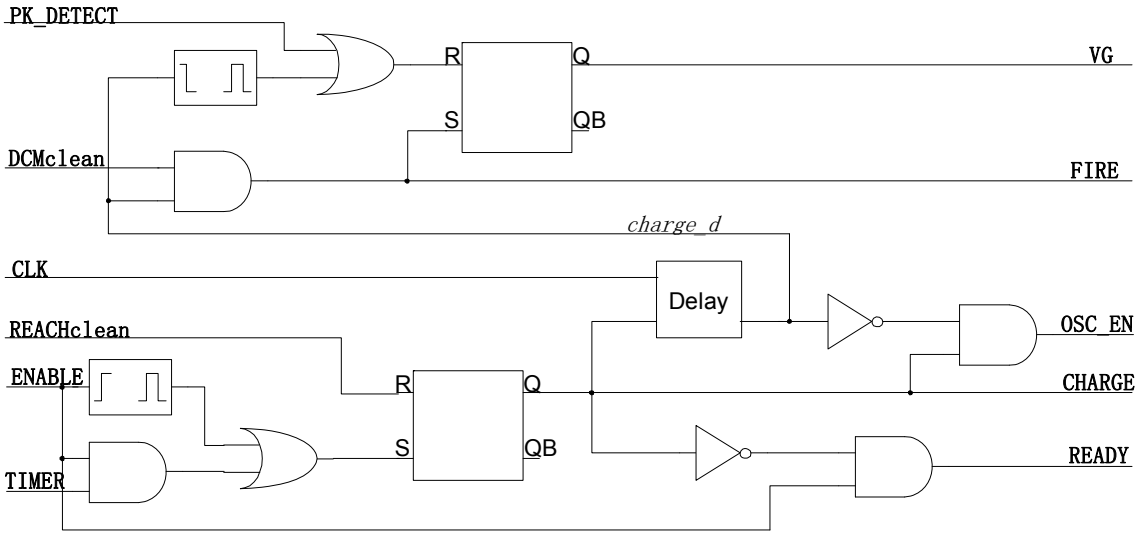
PFC_WINDOW



The circuit provides a blanking interval (timing window) for REACH, DCM and OCP signals. During the time when VSW is ringing, the circuits are inhibited from making measurement.



PFC_CORE



FIRE is the signal to CTON to start a switching cycle. CTON will generate PK_DETECT once the Ton ended.

OSC_EN is the enable signal for oscillator. The oscillator provides the CLK to the Delay circuit. After the delay, charge_d is asserted and OSC_EN goes low to off the oscillator. The Delay circuit consists of oscillator and counters.

On/Off control of Various Block

The on/off of each block in various modes are shown in the table.

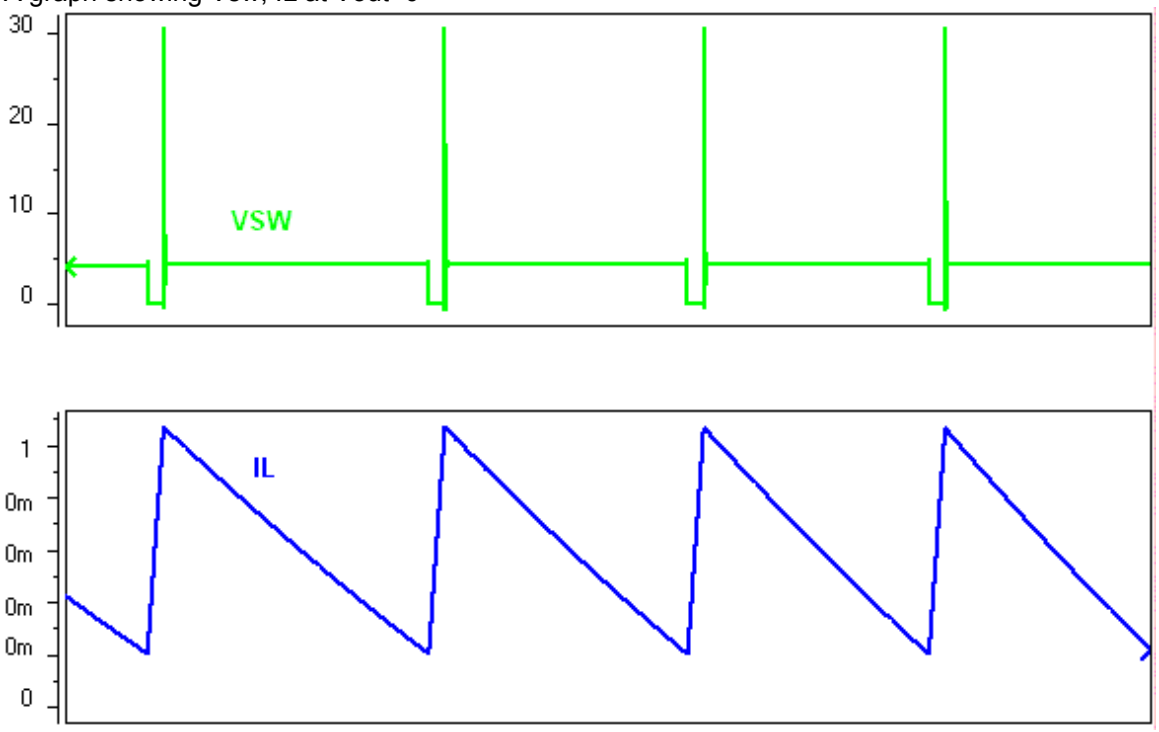
Block/Mode	Off-mode	Charge-mode	Refresh-mode
PFC_CORE	-	-	-
PFC_WINDOW	off	on	off
PFC_MEAS_TOP	off	on	off
PFC_CTON	off	on	off
PFC_OSC	off	*note2	off
TIMER	off	off	on
PFC_BUFFER	off	on	on
PFC_DRIVER	-	-	-

Note1: PFC_CORE and PFC_DRIVER are logic circuit.

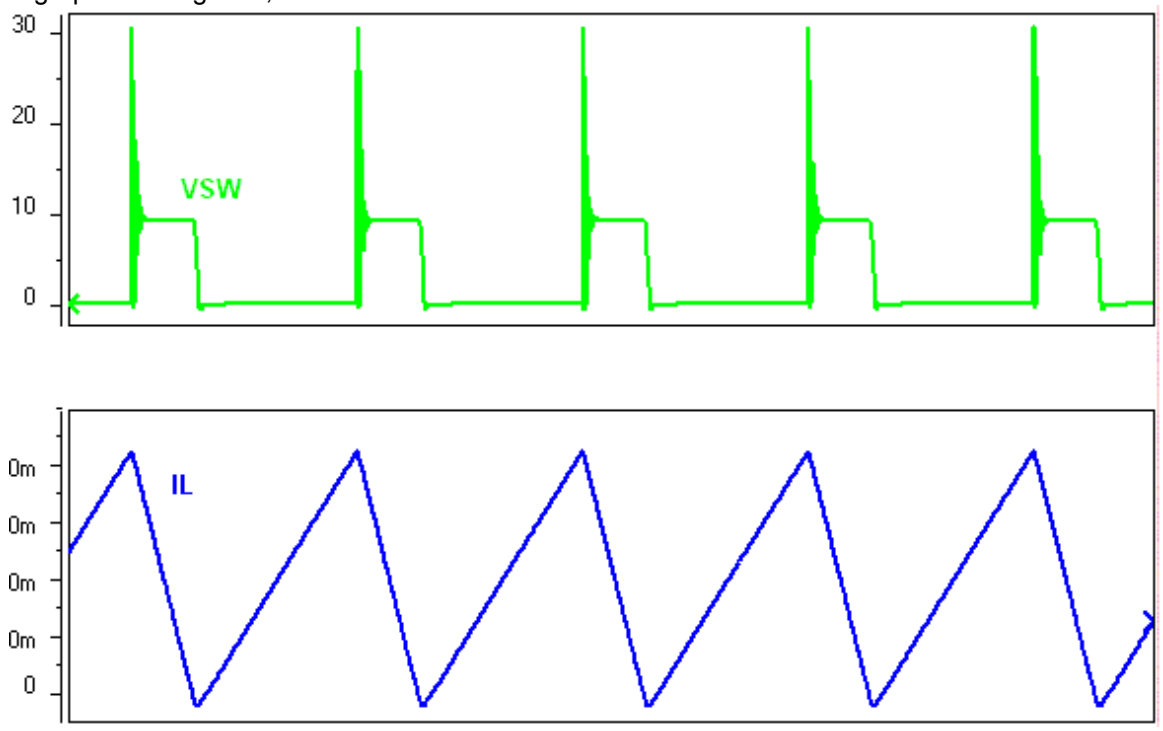
* Note2: oscillator is on only at the beginning of charge-mode.

Simulation Result

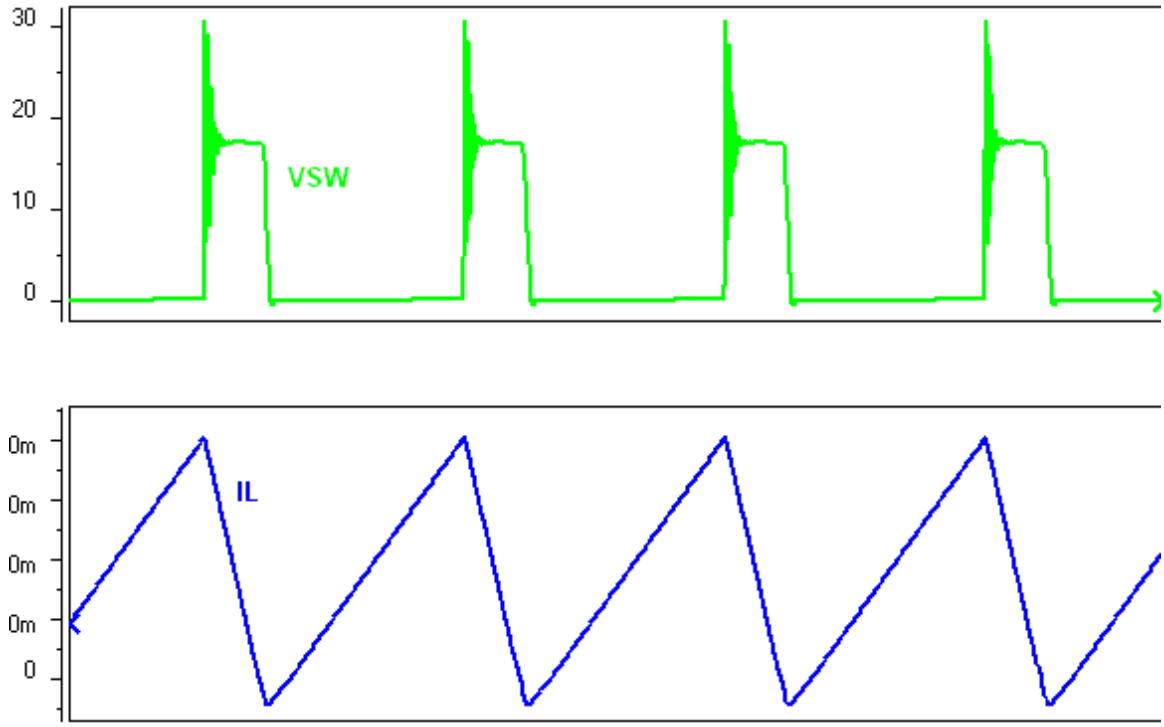
A graph showing Vsw, IL at Vout=0



A graph showing Vsw, IL at Vout=150



A graph showning Vsw, IL at Vout=300.



The simulation results across VDD=2.7 to 5.5V, Temp=-40 to 125 and process corner.

PFC_CTON.

With internal resistor (constant Ton timing) and Lmag=11uH

Signal		Min	Typical	Max
Ton time (us)	2.7V	2.58	3.80	4.93
	5.5V	1.25	1.85	2.40
Peak transform current primary (mA)		603	883	1143
Tset=Ipeak X Lmag=Ipeak X 11uH (us)		6.63	9.73	12.57

With external resistor (constant Ton timing). Rext=540kΩ. Lmag=11uH

Signal		Min	Typical	Max
Ton time (us)	2.7V	3.59	3.72	3.90
	4.1V	2.34	2.43	2.59
	5.5V	1.73	1.80	1.89
Primary coil current (pk-to-pk, mA)		831	868	922
Tset=Ipeak X Lmag=Ipeak X 11uH (us)		9.14	9.55	10.14

PFC_COUNTER (50usDelay)

Signal	Min	Typical	Max
Delay (us)	109	192	235

PFC_OSC

Signal	Min	Typical	Max
Frequency (KHz)	270	330	588

PFC_DELAY_ACC

Signal	Min	Typical	Max
V1SHOTA (ns)	180	240	350
V1SHOTB (ns)	250	390	550

PFC_TIMER

Signal	Min	Typical	Max
Refresh Time (us) (with **100pF** capacitor)	85	105.8	124

PFC_DRIVER

Signal		Min	Typical	Max
Delay Time (ns)	Ton	20	30	60
	Toff	10	18	20

PFC_MEAS_TOP

Transform ratio=23

Signal	Min	Typical	Max
Startup Time for PFC_MEAS_BIAS.VREF2 (us)	8.6	12.8	150.6
Voffset of PFC_DCM (mv). Designed value 25mV.	22.3	25.4	28.6
Error of VSW-VDDA when DCM works (v)	0.231	0.294	0.307
Delay of PFC_DCM (ns)	30	50	161
Voffset of PFC_OCP (mv). Designed value 50mV.	40.1	45.9	53.3
Delay of PFC_MEAS (ns)	52	92	153
Vout when PFC_MEAS=1(v). Designed value 23*15=345v.	343.3	343.7	346
Average current consumption of PFC_MEAS_TOP (uA)	78.9	178	307

PFC (picasso version)

Signal			Min	Typical	Max
Average Current (uA)	Charge-mode	EXCEPT DRIVER	310	413	619
		PFC_DRIVER	939	1914	3548
	Off-mode	EXCEPT DRIVER	3.1	3.5	4.6
		PFC_DRIVER	0	0	0.1
	Refresh-mode	EXCEPT DRIVER	40	43	46
		PFC_DRIVER	0	0	0.1