GPS RF Front-end

FEATURES

- Single-chip GPS L1 Band, RF front-end using 0.18um RF CMOS.
- Extremely low power consumption, <20mA when in operation.
- Extremely low noise figure of <3dB.
- Single conversion, low-IF of 4.092MHz.
- 2-bit ADC for interference rejection.
- Minimum requirement of external components.
- No need of bulky IF SAW or discrete filter.
- 2 integrated low power LDOs to provide 1.8V supply voltages.
- Only a single 3.3V supply voltage is required.
- Operating modes controlled by only 2 pins.
- Small QFN24 package.

GENERAL DESCRIPTION

The H4 is an extremely low power, low noise figure, high performance GPS RF Front-end. Its 2-bit digital output allows easy interface with any existing GPS Baseband IC for optimal interference rejection capability of GPS signal reception.

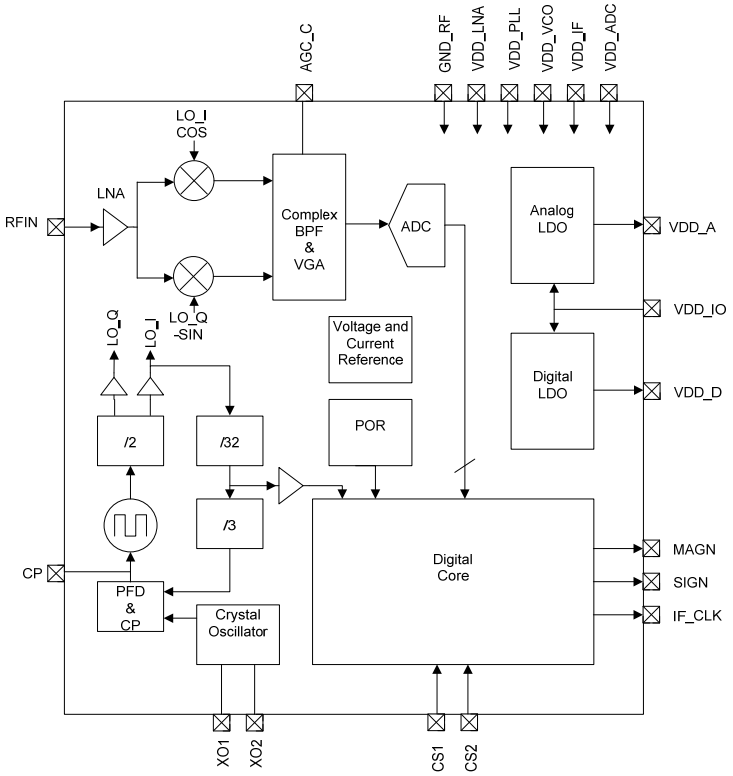
It is a low-IF, single conversion receiver that down-convert GPS L1 signal at RF of 1.575GHz to a low IF of 4.092MHz. This receiver architecture requires minimum amount of external components and thus minimum PCB floor area required.

Its various operating mode allows easy control by the Baseband IC. This facilitates fast shut-down and start-up to enhance the overall performance of GPS devices.

ORDERING INFORMATION

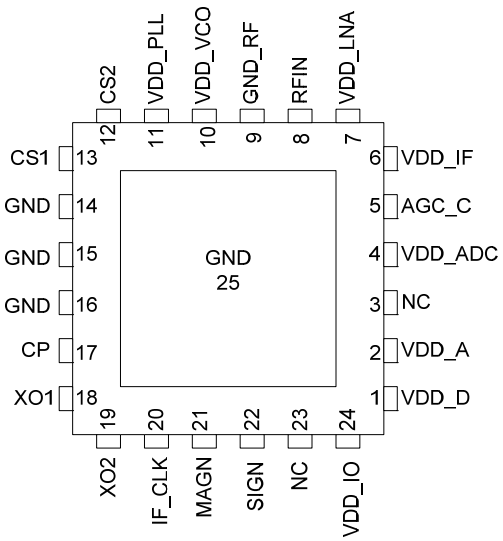
OZ668MS1LN – 24-pin QFN Lead Free

FUNCTIONAL BLOCK DIAGRAM



TERMINAL ASSIGNMENTS

TOP VIEW



Terminal 25 (GND) is the exposed pad on bottom of package

TERMINAL DEFINITIONS

Pin No	Pin Name	Type	Function Description
1	VDD_D	Supply 1.8V	This is digital LDO output meant for internal digital circuit.
2	VDD_A	Supply 1.8V	This is analogue LDO output meant for internal analogue circuit.
3	NC	No Connection	Just leave it floating.
4	VDD_ADC	Supply 1.8V	VDD of ADC.
5	AGC_C	Analog	To external capacitor of AGC. Connect a 10nF capacitor.
6	VDD_IF	Supply 1.8V	VDD of IF circuit.
7	VDD_LNA	Supply 1.8V	VDD of LNA and Mixer.
8	RFIN	Analog	RF input to LNA.
9	GND_RF	Ground	Ground.
10	VDD_VCO	Supply 1.8V	VDD of VCO.
11	VDD_PLL	Supply 1.8V	VDD of PLL.
12	CS2	Digital Input	Control the operating mode of the IC.
13	CS1	Digital Input	Control the operating mode of the IC.
14	GND	Ground	Ground.
15	GND	Ground	Ground.
16	GND	Ground	Ground.
17	CP	Analog	Charge pump of PLL. Connected to loop filter of PLL.
18	XO1	Analog	Crystal Connection.
19	XO2	Analog	Crystal Connection.
20	IF_CLK	Digital Output	Clock to BBIC.
21	MAGN	Digital Output	Data output to BBIC.
22	SIGN	Digital Output	Data output to BBIC.
23	NC	No Connection	Just leave it floating.
24	VDD_IO	Supply 3.3V	Supply voltage of the IC. It is 3.3V.
25	GND	Ground	Pad Paddle of QFN24. Must be connected to Ground.

RFIC OPERATING MODES

Its various operating mode are controlled by CS1 and CS2 according to the table below.

CS1	CS2	Mode	Status
0	0	Illegal	Do not use this state.
0	1	Stand-by	Crystal oscillator and some essential circuit are working. IF_CLK is provided. This allows fast transition into Normal Mode.
1	0	Normal	RFIC is fully operational.
1	1	OSC only	Only crystal oscillator is working and IF_CLK is provided.

FUNCTIONAL DESCRIPTION

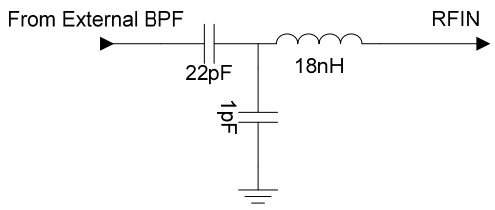
1. Receiver Architecture

A low-IF receiver is adopted for its simplicity in circuit design and reduced need of external components. This will result in lower power consumption which is critical for hand held or portable devices.

The external components needed are mainly for LNA input matching, PLL loop filter and DC decoupling capacitors.

2. Front-end

Three external components are needed for LNA input matching as shown.



For the LNA, traditional Cascode Amplifier is used for its better stability and better reverse isolation. The 18nH acts as the gate inductor to achieve an optimal noise and gain matching for the LNA. To achieve a good NF of less than 1.5dB, it is imperative that S11 or input return loss be trade-off to a poor but acceptable value of about -10dB.

Depending on the PCB trace, slightly different value from the 18nH could be needed. It is possible also to remove the 1pF shunt capacitor without adversely affect the NF and S11 of the LNA.

With a Cascode LNA, it is possible to attain a nominal gain of about 25dB without consuming too much current. With the external gate inductor, it is also possible to attain NF of less than 1.5dB. It is suggested that high Q factor of greater than 60 should be used for this inductor.

An image-rejection active mixer (Gilbert Cell) is used to provide additional 10dB of gain for the front-end. With total nominal gain of 35dB, the noise figures of subsequently stages pose minimal effect to the receiver NF.

3. Filter

With the use of low-IF receiver and image-rejection mixers, not external image rejection filter is needed. Instead, an active complex band pass filter of with bandwidth of 2MHz and center frequency of 4MHz is used.

Biquadratic 2nd order filters are cascaded to form an 8th order Complex Bandpass Filter. This filter rejects the image frequency which is center at negative frequency of -4MHz. It also acts as anti-alising filter for the ADC which is sampled by a clock frequency of 16MHz. Operational Amplifiers are used for the active filter and this results in high linearity and low noise figure. Butterworth Configuration is adopted for its low in-band group delay variation and acceptable out-of-band rejection.

There is automatic self-calibration circuit to tune the filter bandwidth and center frequency to the right value when the circuit is started-up. Thereafter, no calibration is needed as the filter is insensitive to temperature and voltage variation.

4. AGC and ADC

AGC is needed to provide a self-adaptive gain to the receiver. Since the bandwidth of the receiver, which is 2MHz, is decided by the IF Complex Band Pass Filter, the input referred noise at LNA's input is -174dBm+63dB=-111dBm. A gain of about 100dB is needed to provide enough signal level at ADC's input for it to operate properly.

AGC will automatically reduce or increase the IF gain to maintain a pre-determined signal level at the input of ADC. This is necessary as the gains of various circuits in the receiver chain are depending on factors such as process variation, voltage variation and temperature variation. Moreover, input matching of LNA's input, or the addition of external LNA for enhanced system NF, will also affect the gain of the receiver.

An external 10nF is needed for the AGC circuit. This will set a time constant of about 10ms, which is generally optimal for BBIC.

ADC, which is 2 bits, converts the analogue output signal of VGA into 2 digital signals, SIGN and MAGN. SIGN and MAGN represent the MSB and LSB of the digitalized output respectively. The 4 levels signal representation is shown here.

SIGN	MAGN	Coded Value
0	1	+3
0	0	+1
1	0	-1
1	1	-3

The MAGN bit is maintained to be active (high) for 33% of the time. This provides the best interference rejection for Spread Spectrum De-correlation.

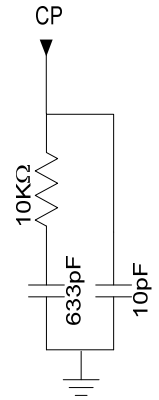
The SIGN and MAGN signal are latched by the falling edge of IF_CLK. Hence, the latch of BBIC should use the rising edge of IF_CLK to latch in the SIGN and MAGN. Please refer to 'Digital Output Timing Diagram'.

5. PLL

An integer-N phase lock loop is used as the frequency synthesizer. It requires a 16.368MHz reference source either from an internal crystal oscillator, which requires an external crystal or an external TCXO. TCXO is suggested for high performance GPS device.

The PLL uses an internal VCO, with 64 band of tuning curve. During start-up of RFIC, one of the bands will be automatically selected. This ensures the tuning sensitivity of VCO is controlled within 100MHz/V to improve the overall phase noise of PLL and NF of the receiver.

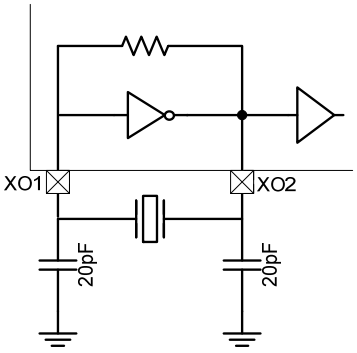
For optimal NF performance, the loop BW can be designed at 100KHz. This ensure the poorer phase noise of VCO at 10KHz offset, mainly due to up-converted low frequency flicker noise, will be rejected by the PLL's loop bandwidth.



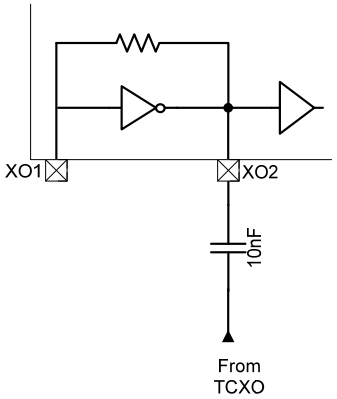
The above shows the PLL loop filter. To further save the external components, the 10pF can be omitted without severely affect the PLL's performance.

6. Crystal Oscillator

A self-bias inverter, with the external crystal, is configured as Pierce Oscillator. The crystal oscillator draws it supply directly from 3.3V. An internal amplitude control circuit ensures that the voltage swing at the two terminals of crystal is not excessive to prolong the lifetime of the crystal.



If an external TCXO is used, a DC coupling of value about 10nF is required. Terminal XO1 can be left floating.



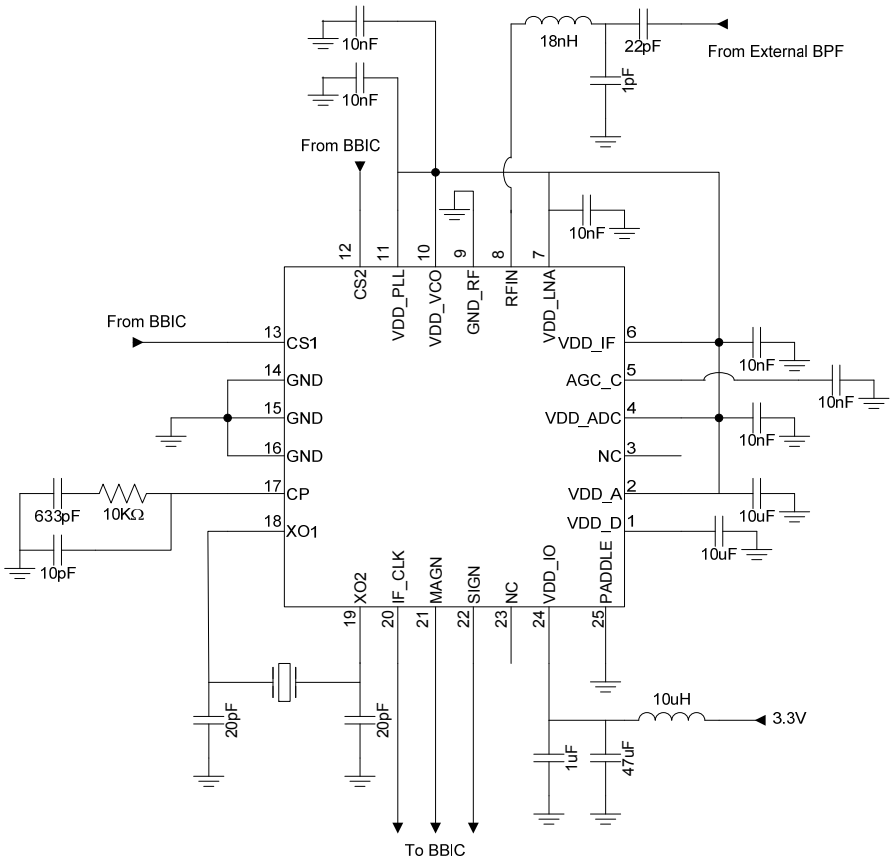
7. LDO

There are 2 on-chip LDOs: Digital LDO and Analogue LDO. Both accept input supply voltage of 3.3V and provide output supply voltage of 1.8V.

They are able to supply up to 20mA of output current. An external Tantalum Capacitor of 5uF to 10uF is needed for stable operation.

The Analogue LDO is especially designed for low-noise operation. It is used to provide 1.8V supply for various blocks of the RFIC.

TYPICAL APPLICATION



- Only a 3.3V supply is needed. The output of analogue LDO, VDD_A is used to provide 1.8V supply voltage to various circuit of the RFIC.
- BBIC will control the operating mode of RFIC via CS1 and CS2.
- Three external components are needed to provide input matching for the internal LNA. The 1pF shunt capacitor can be omitted if its effect on the S11 is minimal.
- Likewise, the 10pF shunt capacitor of PLL loop filter can also be omitted if its impact on NF is minimal.

AC Electrical Characteristics, Receiver

Parameter	Condition	Min	Typ	Max	Unit
Operating Voltage		1.7	1.8	1.9V	V
Operating Temperature		-40		85	°C
IIP3	Inband		-65		dBm
Input Compression Point			-75		dBm
Total NF			3	5	dB
Image Rejection		20	25		dB
Total Gain	Voltage gain		100		dB
LO leakage at RF port			-70		dBm
Current Consumption	At 1.8V, typical condition.		18	20	mA

AC Electrical Characteristics, Front-end

Parameter	Condition	Min	Typ	Max	Unit
Voltage Gain		32	35	38	dB
NF			2	2.5	dB
IIP3, Input IP3			-30		dBm

AC Electrical Characteristics, PLL

Parameter	Condition	Min	Typ	Max	Unit
Fout. Output Frequency.	IF=4.092MHz		1571.4		MHz
Frequency Reference.			16.368		MHz
Loop BW			100		KHz
Reference Spurious				-50	dBc
Phase Noise	@100KHz @1MHz		-96 -119		dBc/Hz
Charge Pump Current			100		uA

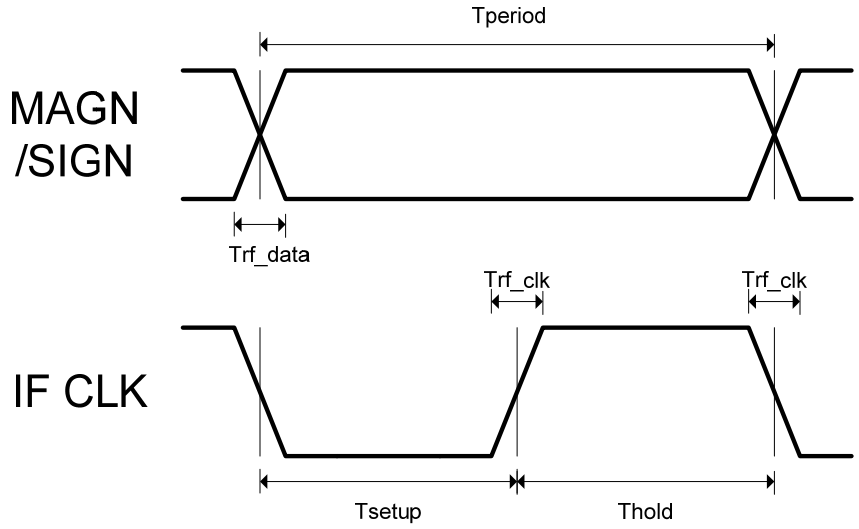
AC Electrical Characteristics, VCO

Parameter	Condition	Min	Typ	Max	Unit
Fout. Output Frequency Tuning Range.		3142.8 -200	3142.8	3142.8 +200	MHz
Tuning Range	From Vtune=0.25V to (VDD-0.25V).		±200		MHz
Tuning Sensitivity.			100		MHz/V
Phase Noise	@100KHz @1MHz		-90 -110		dBc/Hz

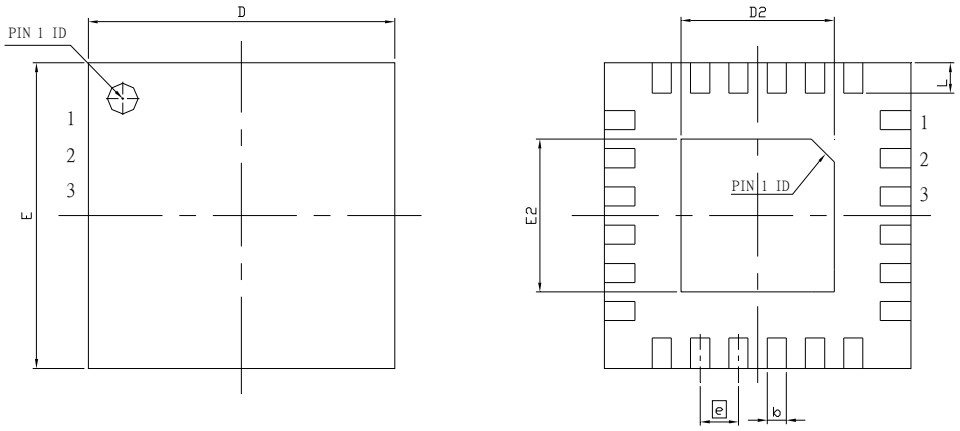
Digital Output (MAGN, SIGN, IF_CLK) Timing Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Tperiod			61.1		ns
Trf_data	Rise or fall time (10% and 90%) of MAGN or SIGN. Cload<10pF	6	9	12	ns
Trf_clk	Rise or fall time (10% and 90%) of IF_CLK. Cload<10pF	6	9	12	ns
Tsetup	Setup time of IF_CLK	20	30	40	ns
Thold	Hold time of IF_CLK	20	30	40	ns

Digital Output (MAGN, SIGN, IF_CLK) Timing Diagram



PACKAGE INFORMATION – 24-pin QFN



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.203 REF		
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	1.90	2.00	2.10
E	3.90	4.00	4.10
E2	1.90	2.00	2.10
e	0.50 BSC		
L	0.30	0.40	0.50

Notes:
1. ALL DIMENSIONS ARE IN MILLIMETER.

Exposed pad at bottom is GND (pin 25) and must be fully soldered to PCB

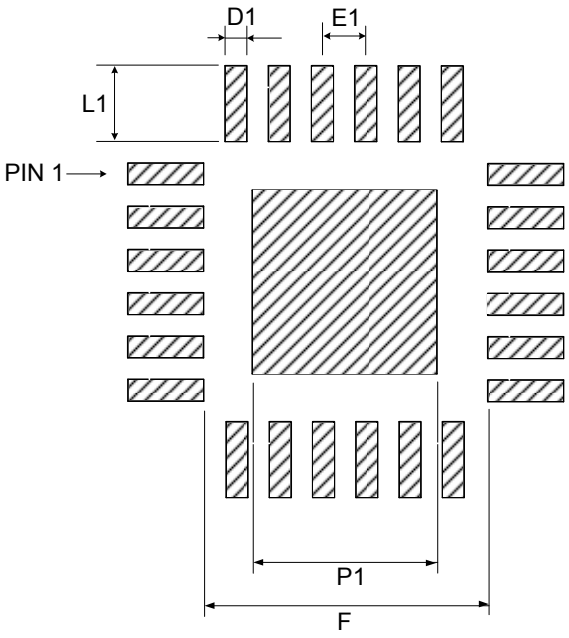
Rth j-a (QFN-24 4x4mm package) = 38ºC/W
Rth j-c (QFN-24 4x4mm package) = 4.8ºC/W

DIMENSIPN TABLE

SYMBPL	SPECIFICATIPN
	24L QFN 4X4 BPXY
X1	0.25
E1	0.50
L1	0.80
P1	2.50
F	3.20

All dimensions are given in millimeters.

RECOMMENDED LANDING PATTERN



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