This report serves as a comparison between FD (Frequency Divider) and MMD. All circuits presented below is designed and simulated in ADS 2005A.

# 1. Fundamental Structure of the FD

The frequency divider in this report is composed of one div-by-2 circuit, one div-by-8/9 prescaler, two 5-bit program counters, and some other logic circuits, as shown in Fig. 1.1.

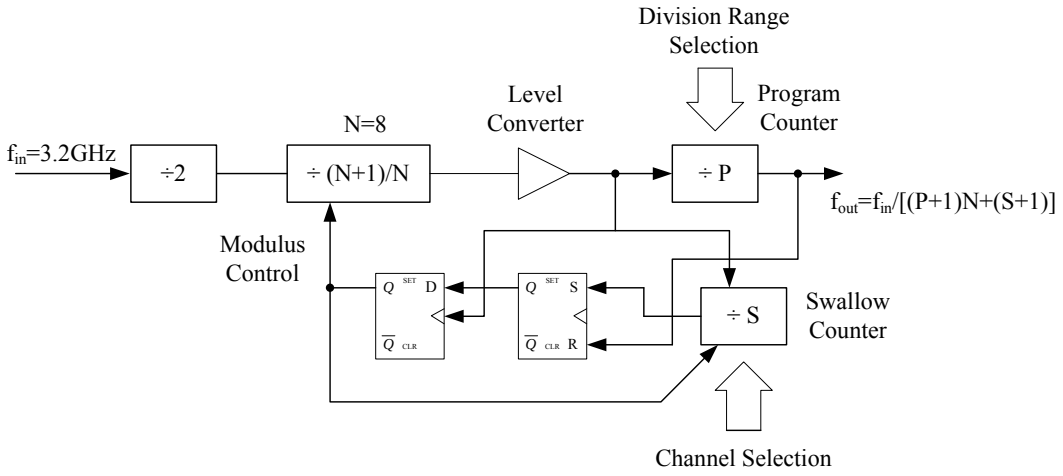


Fig. 1.1: Basic Divider Structure

There are several important aspects of the divider (excluding the first div-by-2 circuit):

1. When they are full, both of the two program counters (P and S) are reset synchronously, so the overall division ratio of the divider is (P+1)N+(S+1).
2. The dual modulus prescaler in Fig. 1.1 is realized by CML logic, and the remainder of the circuits incorporates standard CMOS logic.
3. N is selected to be eight to relieve the delay requirement in the control paths.
4. To achieve a continuous division range, two conditions must be satisfied: $P \geq 9$ & $0<S<P$. The continuous division ratio ranges from 82 to 287.
5. With any selected P, the division ratio ranges from (P+1)N+2 to (P+1)N+P. The division ratios with different values of P are presented in Table 1.1.

Table 1.1: Division Ratios with Different P Value

| P | Minimum Division Ratio | Maximum Division Ratio |
|---|---|---|
| 9 | 82 | 89 |
| 10 | 90 | 98 |
| 11 | 98 | 107 |
| 12 | 106 | 116 |
| 13 | 114 | 125 |
| 14 | 122 | 134 |
| 15 | 130 | 143 |
| 16 | 138 | 152 |
| 17 | 146 | 161 |
| 18 | 154 | 170 |
| 19 | 162 | 179 |
| 20 | 170 | 188 |
| 21 | 178 | 197 |
| 22 | 186 | 206 |
| 23 | 194 | 215 |
| 24 | 202 | 224 |
| 25 | 210 | 233 |
| 26 | 218 | 242 |
| 27 | 226 | 251 |
| 28 | 234 | 260 |
| 29 | 242 | 269 |
| 30 | 250 | 278 |
| 31 | 258 | 287 |

# 2. Divide by 8/9 Prescaler Design

## 2.1 Block Diagram

The basic structure of the divide-by-8/9 circuit is shown in Fig. 2.1(a). It is composed of one divide-by-2/3 circuit and two divide-by-2 circuits. All these dividers are designed to be falling edge triggered. When MC=1, the prescaler ÷8; when MC=0, the prescaler ÷9. The functional waveform of the prescaler is shown in Fig. 2.1(b) & (c).

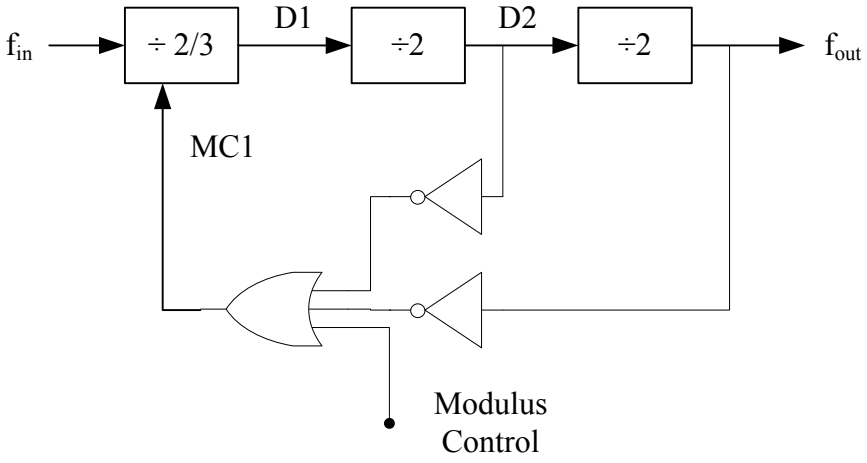


Fig. 2.1(a): Divide-by-8/9 Prescaler

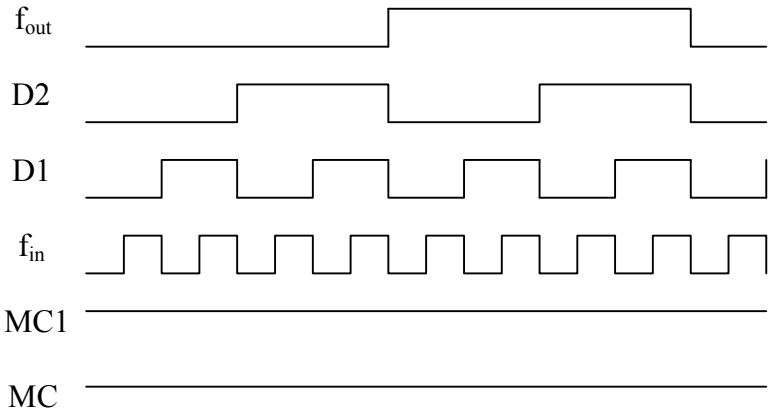


Fig. 2.1(b): The Functional Waveform of the Div-by-8/9 Prescaler (÷8)

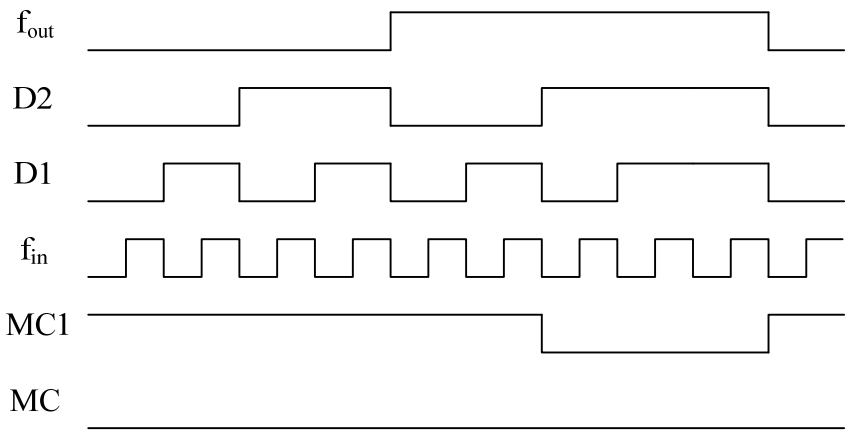


Fig. 2.1(c): The Functional Waveform of the Div-by-8/9 Prescaler (÷9)

The Div-by-2/3 circuit is shown in Fig. 2.2(a), which consists of two falling-edge-triggered Master-Slave Flip-Flops, two OR gates and one output buffer. When MC1=1, the Div-by-2/3 circuit ÷2; when MC1=0, it ÷3.

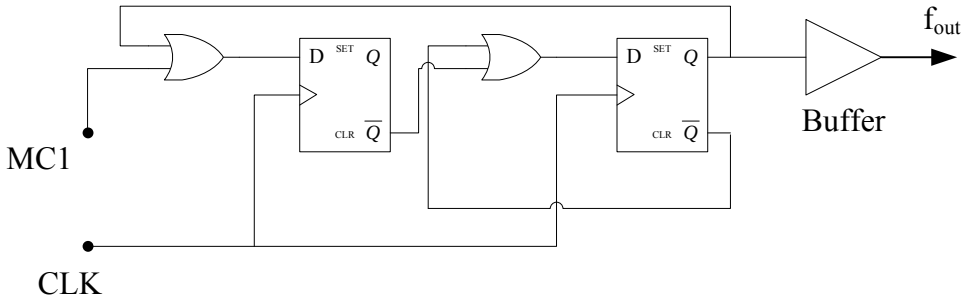


Fig. 2.2(a): Div-by-2/3 Circuit

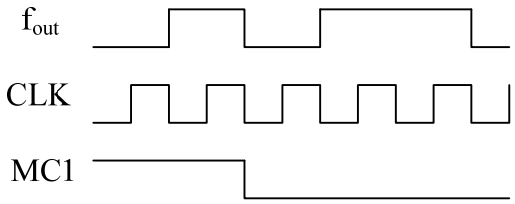


Fig. 2.2(b): Functional waveform of the Div-by-2/3 circuit

## 2.2 Circuit Design

Since the Div-by-8/9 prescaler operates at the highest frequency of the whole divider, all latches and logic gates in the prescaler are realized by CML logics instead of normal digital logics.

Fig. 2.3 presents the detailed design of the Div-by-8/9 prescaler in ADS.

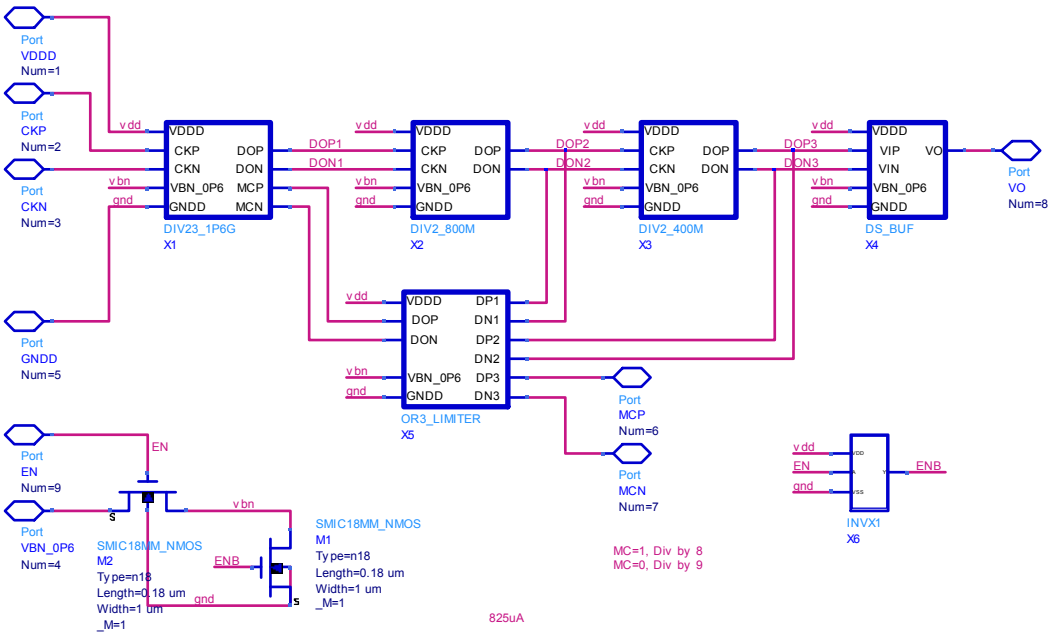


Fig. 2.3: The Div-by-8/9 prescaler design in ADS

Both the div-by-2/3 circuit and the div-by-2 circuits in Fig. 2.3 are realized by CML logics. The designs of them are shown in Fig. 2.4 and Fig. 2.5. Fig. 2.6 illustrates the structure of the CML logic. All CML latches in the prescaler employs the same kind of structure. The only difference between them is their current consumption, which is scaled down with their operating frequencies. The OR gates in Fig. 2.2 are combined with the flip-flops to avoid using CMOS digital logic as shown in Fig. 2.7.

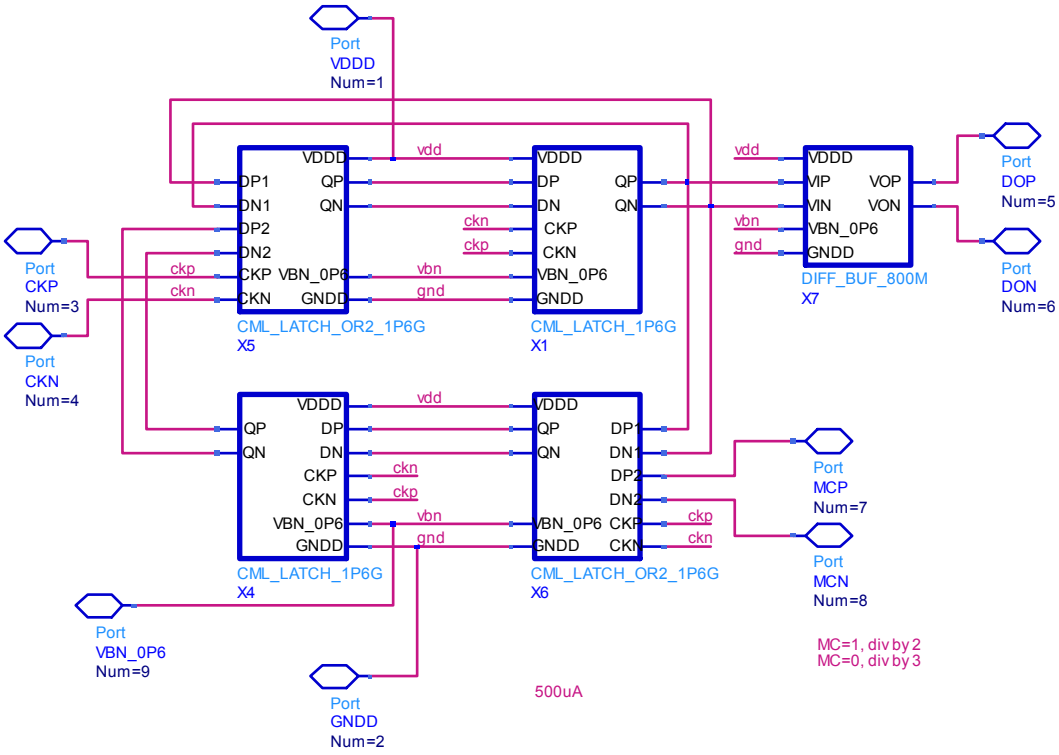


Fig. 2.4: Div-by-2/3 Circuit

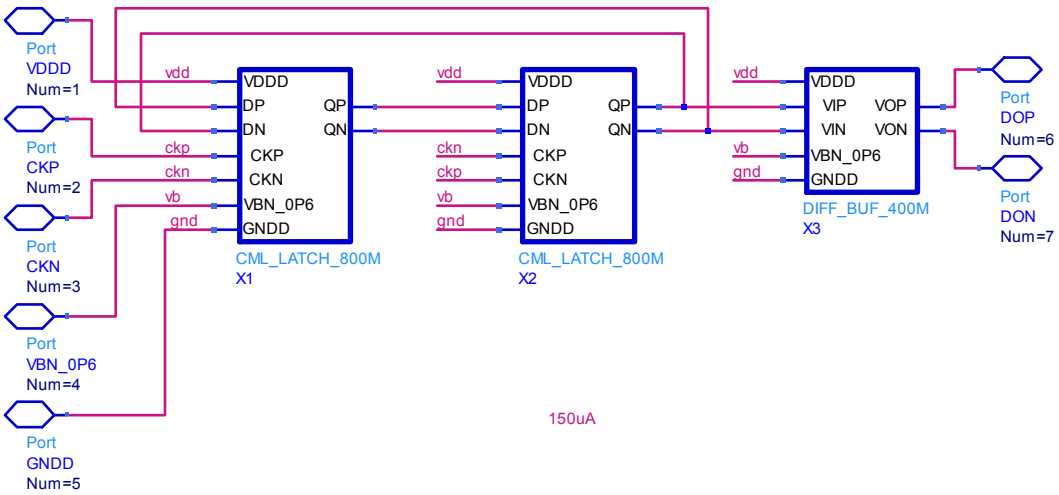


Fig. 2.5: Div-by-2 Circuit

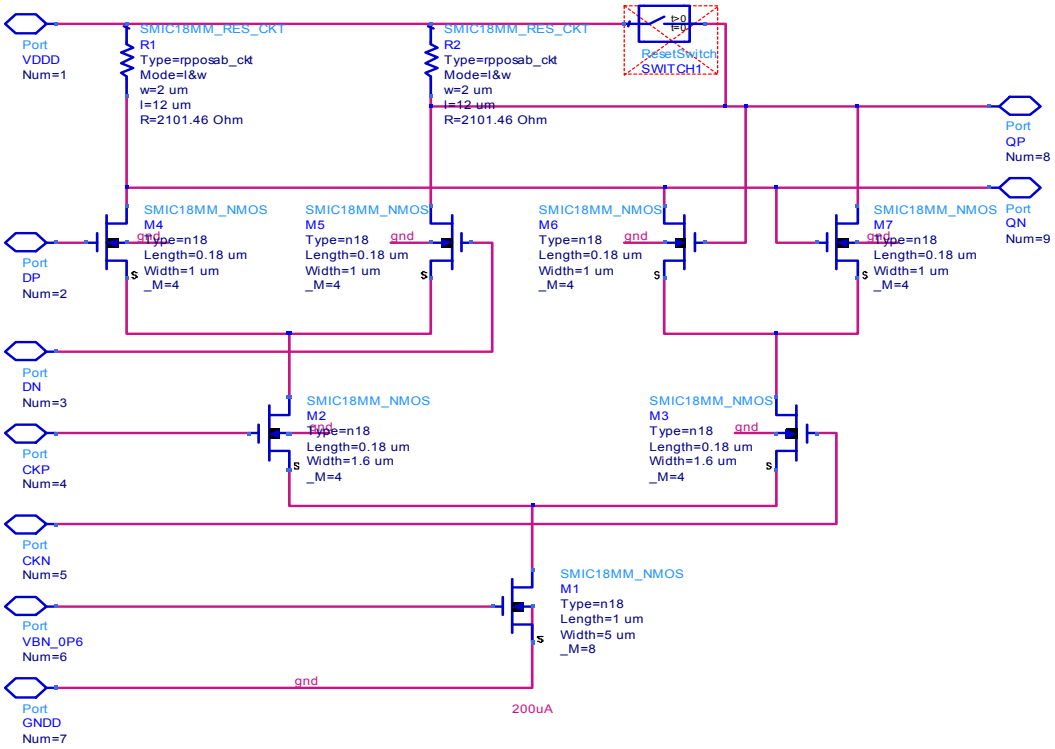


Fig. 2.6: CML Latch Design

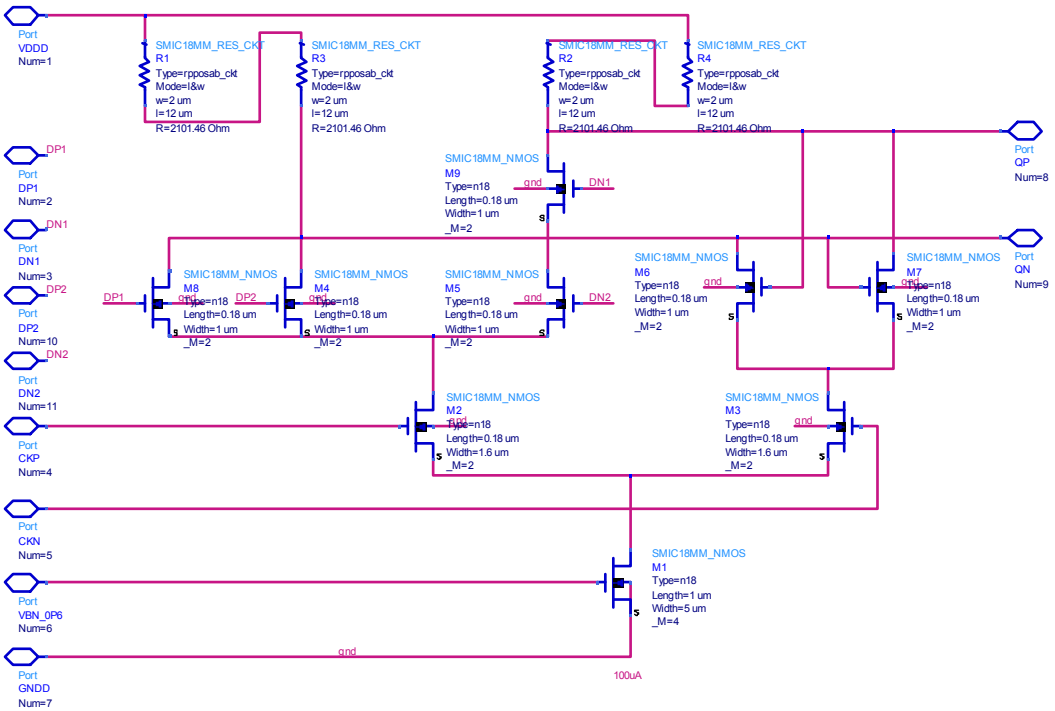


Fig. 2.7: OR Gate Combined CML Latch Design

Since the div-by-2/3 circuit and the div-by-2 circuits are realized by CML logics with limited output swings, the OR gate in the div-by-8/9 prescaler cannot incorporate normal digital logic, and it is very difficult to combine it with some CML latch, since it has three inputs. Too many transistors stacked in one branch may cause logic error, when the amplitude of the differential inputs is not large enough. In this design, it is also realized by current-steering-logic, as shown in Fig. 2.8.

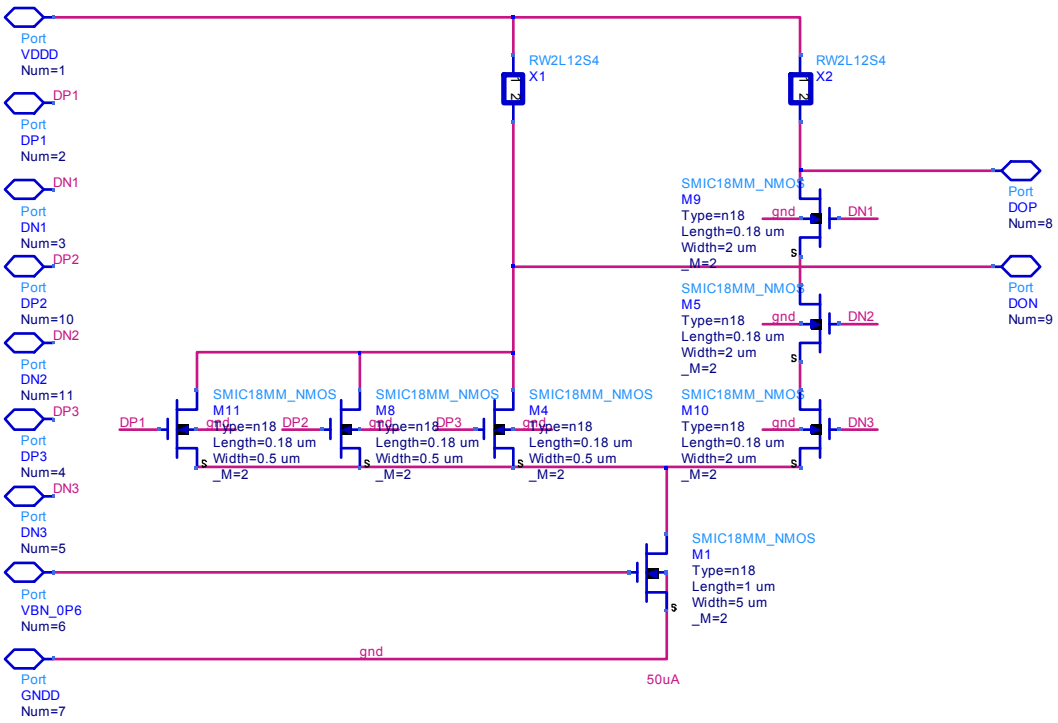


Fig. 2.8: The differential OR gate in the Div-by-8/9 Prescaler

Compared Fig. 2.3 to the block diagram shown in Fig. 2.1, a Differential-to-Single-ended buffer is implemented at the output of the div-by-8/9 circuit to convert the prescaler differential outputs to a single-ended rail-to-rail signal. The design of the D-to-S buffer is shown in Fig. 2.9.

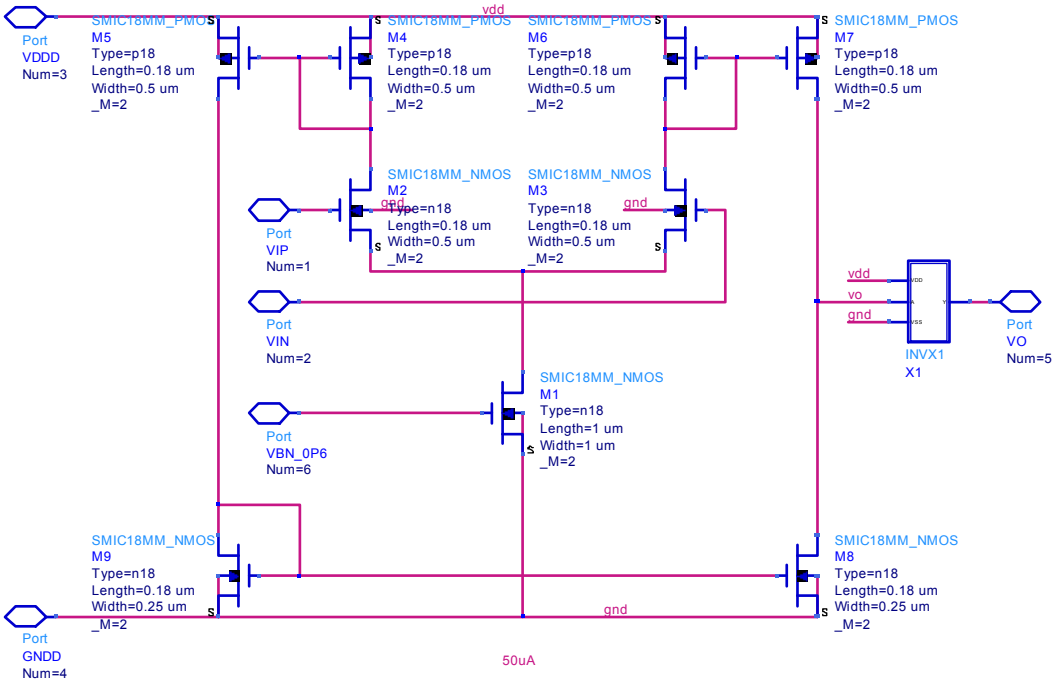


Fig. 2.9: D-to-S Buffer

# 3. Programmable Counter Design

## 3.1 Block Diagram

The programmable counter in this divider is a 5-bit asynchronous counter [1]. It consists of five falling-edge-triggered div-by-2 circuits and some control gates, as shown in Fig. 3.1.

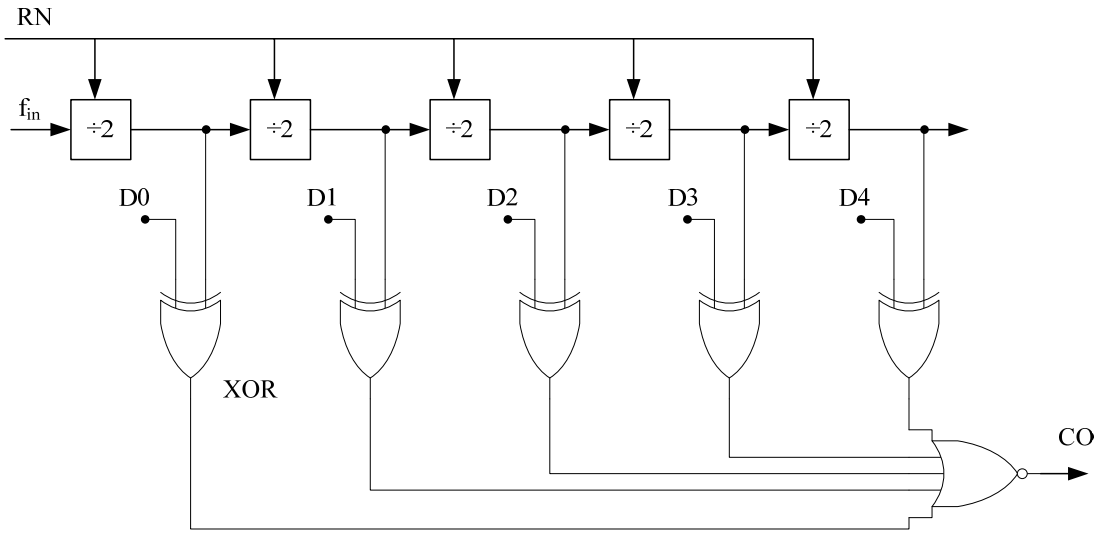


Fig. 3.1: Programmable Counter

The counters functions as following:

When RN=1, the counter will count the input cycles until it reaches the preset D[4:0], then the CO will rise to 1 to indicate the counter is full; Whenever RN=0, the counter will be cleared to 0 immediately, and it will keep the 0 until RN rise to 1 again.

Considering the input frequency has been scaled down to about 200MHz (3.2G/8), this counter is realized by normal CMOS logics. The div-by-2 circuits in this counter are realized by normal rising-edge-triggered DFFs, as shown in Fig. 3.2.

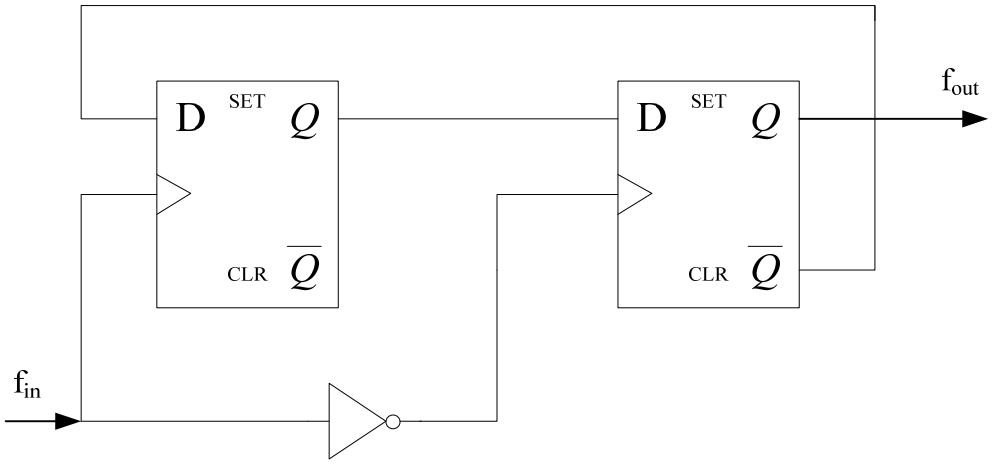


Fig. 3.2: Digital Div-by-2 Circuit

## 3.2 Circuit Design

The schematic design of the programmable counter is shown in Fig. 3.3.

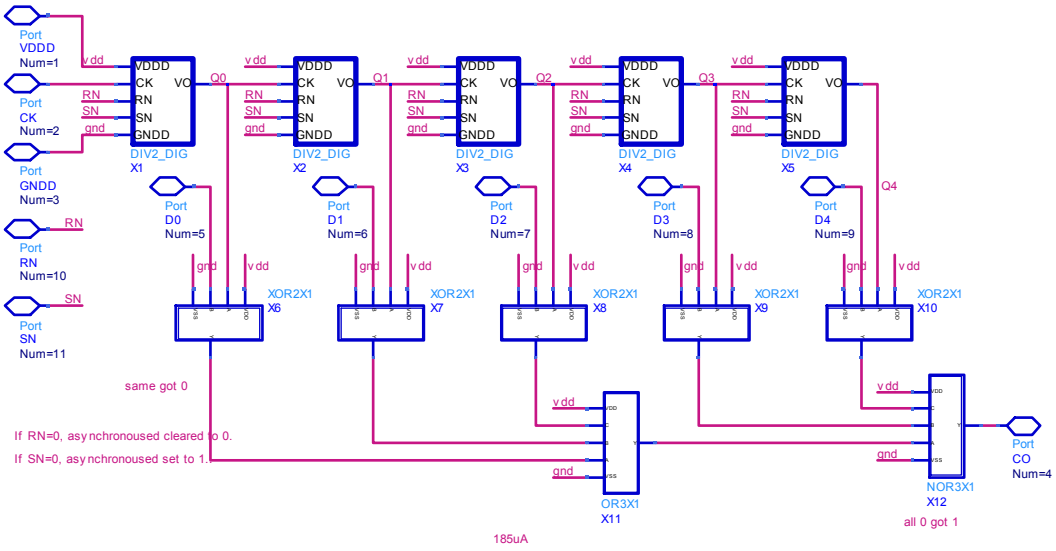


Fig. 3.3: 5-bit Programmable Counter

# 4. Frequency Divider Design

## 4.1 Block Diagram

The block diagram of the whole frequency divider is shown in Fig. 4.1(a). The FD also includes the first stage of the div-by-2 prescaler, which generates the four branches of I/Q signals. A level converter is implemented between the div-by-8/9 circuit and the programmed counters to amplify the signal swing to rail-to-rail. The functional waveform of the FD is shown in Fig. 4.1(b).

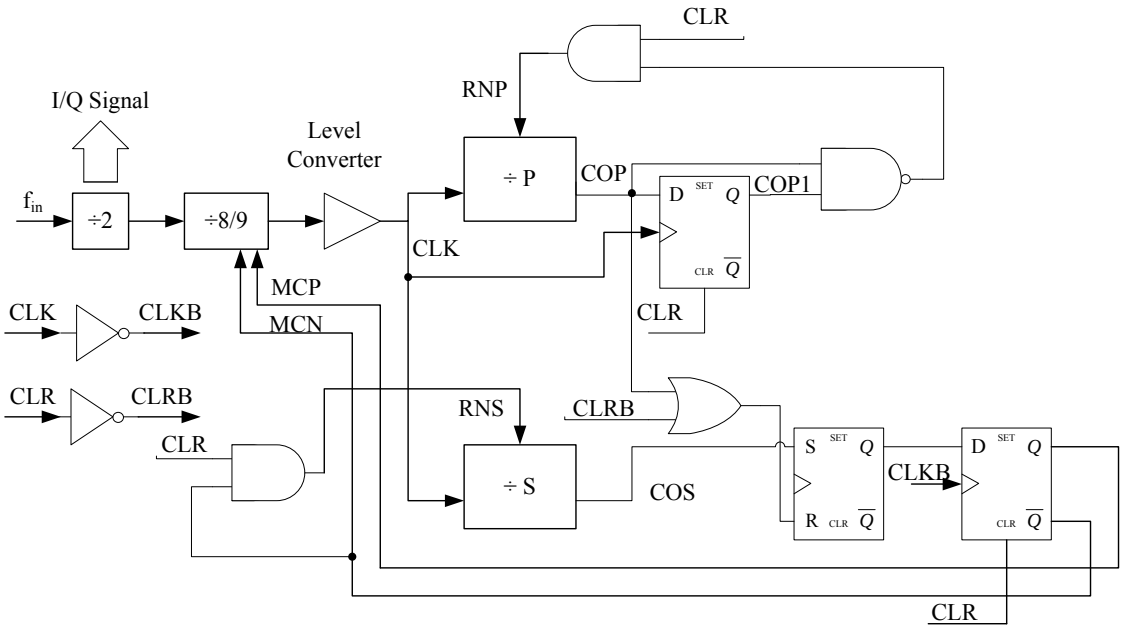


Fig. 4.1(a): The Dual-Modulus Divider

*Note: All counters and prescalers in Fig. 4.1(a) are falling-edge-triggered, but all DFFs are rising-edge-triggered.*

The frequency divider functions as following:

1. When CLR=0, all the registers and counters in the divider is reset to 0.
2. When CLR=1, the div-by-8/9 circuit will start to divide by 9, and the counters will start counting.
3. When Counter S counters S input cycles, COS will become 1. After one more cycle, MC will set the div-by-8/9 circuit to divide by 8.
4. Counter P will continue counting CLK, until it is full. Then COP will be stored as COP1 after a half cycle. Then COP and COP1 will reset Counter P to 0.

5. After another half cycle, COP will enable counting of Counter S and set the div-by-8/9 circuit to divide by 9. Then a new period starts.

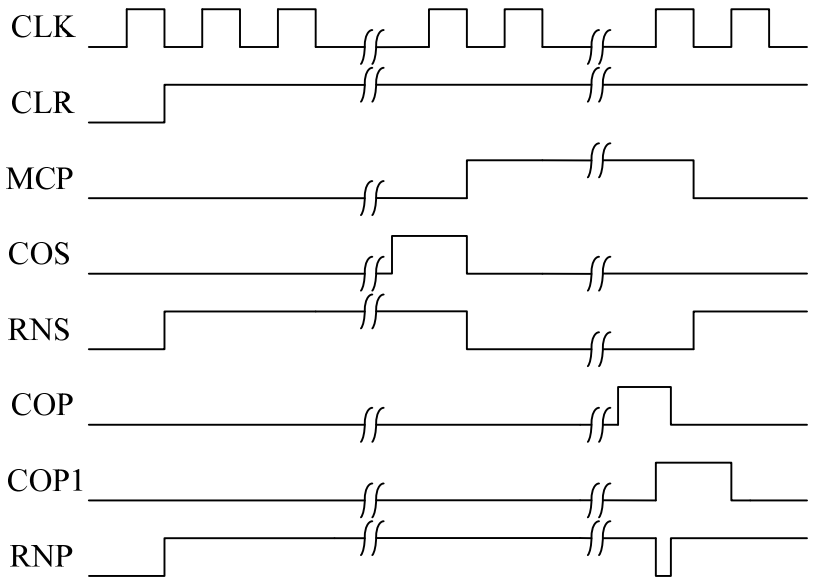


Fig. 4.1(b): Functional Waveform of the Frequency Divider.

The signal shown in Fig. 4.1(b) is explained as following:

CLK: Input clock for programmable counters

CLR: Reset signal for the whole FD (0 to reset)

MCP: Modulus control for the div-by-8/9 prescaler (0→÷9, 1→÷8)

COS: Overflow signal for Counter S (1, when full)

RNS: Reset signal for Counter S (0 to reset)

COP: Overflow signal for Counter P (1, when full)

COP1: Delay COP by a half cycle and hold for 1 cycle.

RNP: Reset signal for Counter P (0 to reset)

## 4.2 Schematic Design

The schematic design of the frequency divider (FD) is shown in Fig. 4.2. There are two more latches used to synchronize the data input of the programmable counters. The two latches are designed to be clocked by the rising edge of RNS, so the ΣΔ-Modulator outside the divider should be clocked by the falling edge of COP1 (refer to Fig. 4.1(b)).

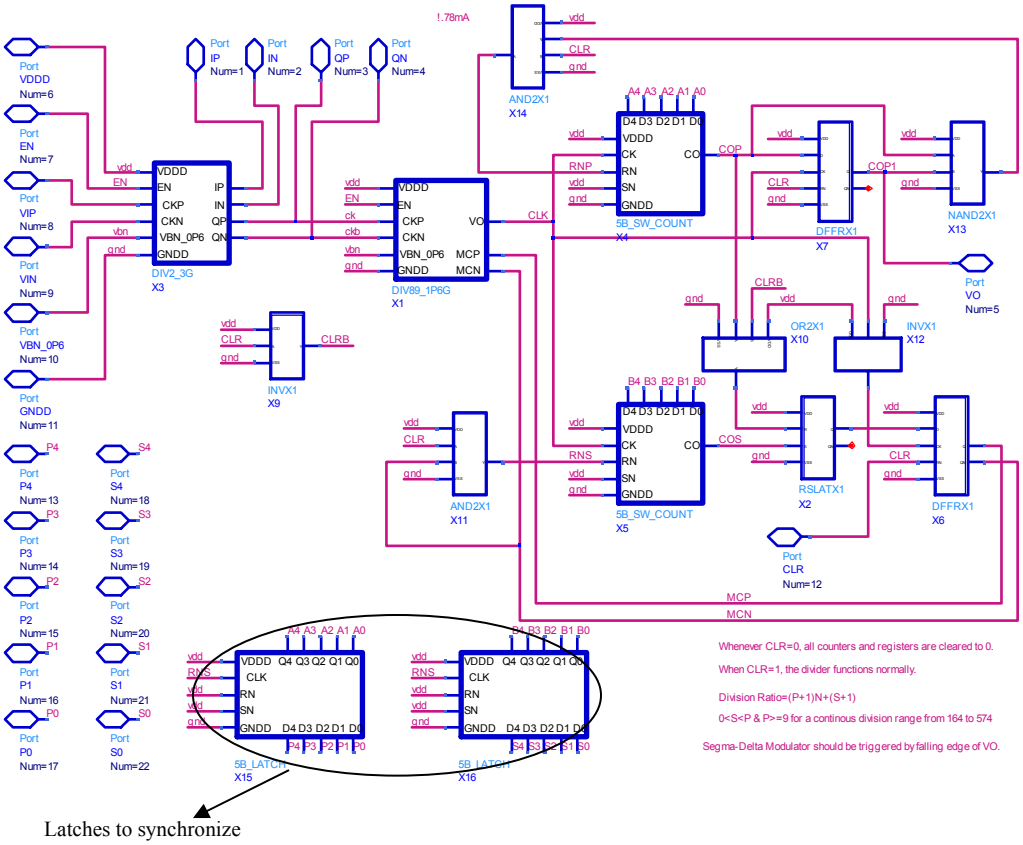


Fig. 4.2: The Frequency Divider Design

# 5. Simulation Results Comparison

Division ratio range of the FD: 164 to 574

Division ratio range of the MMD: 128 to 510

To make a reasonable comparison between the FD and the MMD, the dividers are simulated at three division ratio: 164, 192 and 510.

164 is the minimum division range of the FD.

510 is the maximum division ratio of the MMD.

192 is the division ratio required in our application. (With 16MHz Crystal)

The test bench of the FD and MMD is shown in Fig. 5.1 and Fig. 5.2 respectively. The input frequency is 3.2GHz. A five-output-cycles transient simulation will be launched. The simulation Results will be produced in both time and frequency domain (FFT).

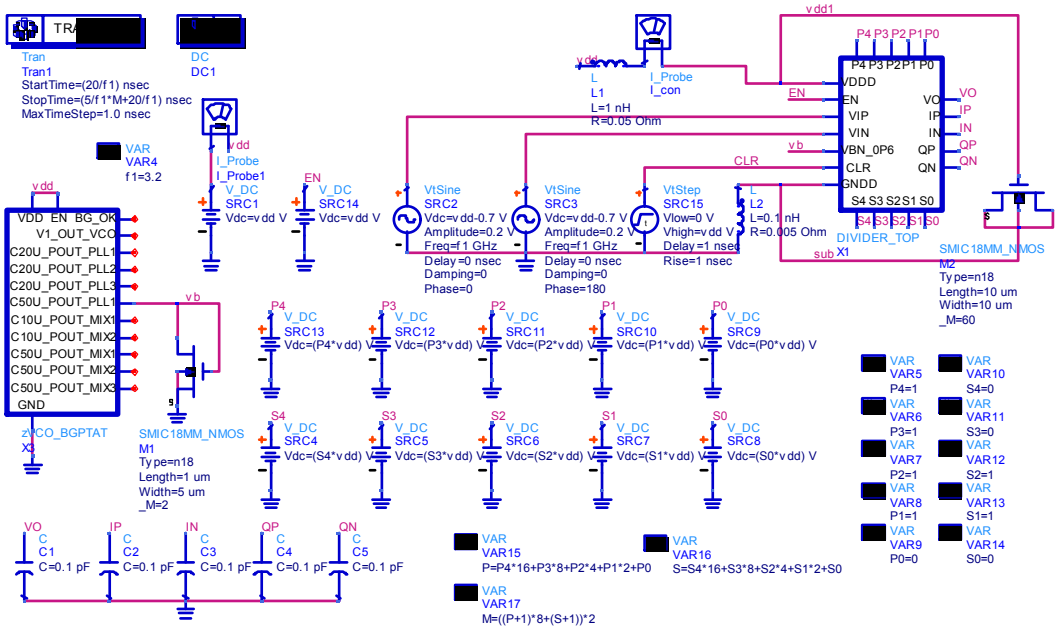


Fig. 5.1: Test Bench of the FD

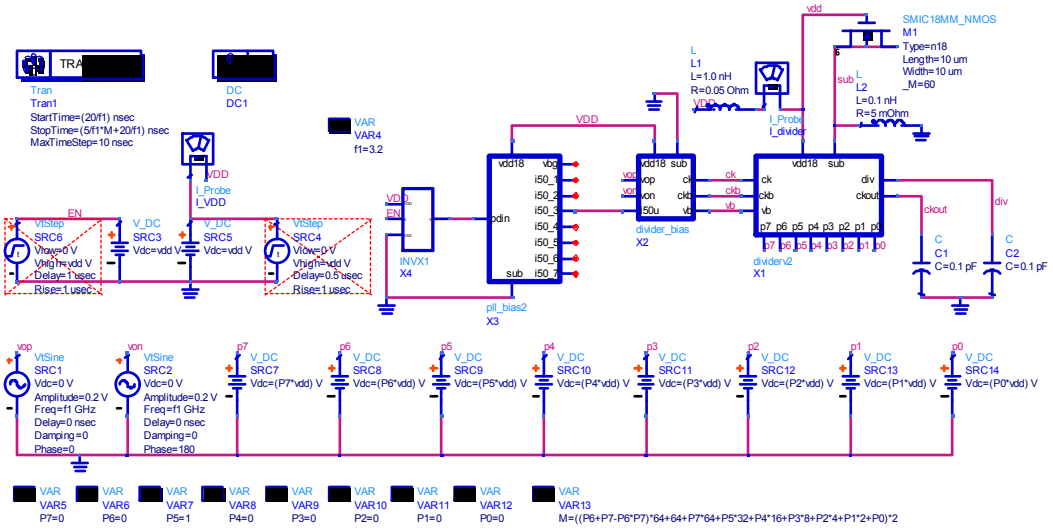


Fig. 5.2: Test Bench of the MMD

## 5.1 Division Ratio = 164

### 5.1.1. Current Consumption

Table 5.1 summarizes the current consumption of the FD and MMD in different corners and their maximum operation frequency at TT.

Table 5.1: Current Consumption of the Dividers (/164)

| | SS | TT | FF | Variation | Max. Operation Frequency |
|---|---|---|---|---|---|
| FD | 1.49mA | 1.72mA | 2.03mA | -13.4% ~ +18.0% | 5.4GHz |
| MMD | 3.13mA | 4.08mA | 4.80mA | -23.3% ~ +17.6% | 4.3GHz |

The results in Table 5.1 may not be very accurate, because the LO buffer of FD is designed based on an uncertain loading of 0.1pF, while the MMD includes no LO buffer at all. However, from these results it is still obvious that the FD can save lots of power compared to the MMD. There are basically three reasons:

First, at higher frequency (>200MHz in this design), each cell of the MMD is a div-by-2/3 circuit, including four CML latches; while the FD only has one div-by-2/3 circuit, others are normal div-by-2 circuit, including only two CML latches.

Second, the MMD employs CML all along its signal path even at very low frequency, while the FD employs only digital logics when frequency goes down to below 200MHz.

Third, the MMD may not be optimized adequately. Its current consumption may be able to be further reduced.

### 5.1.2. Time domain Results:

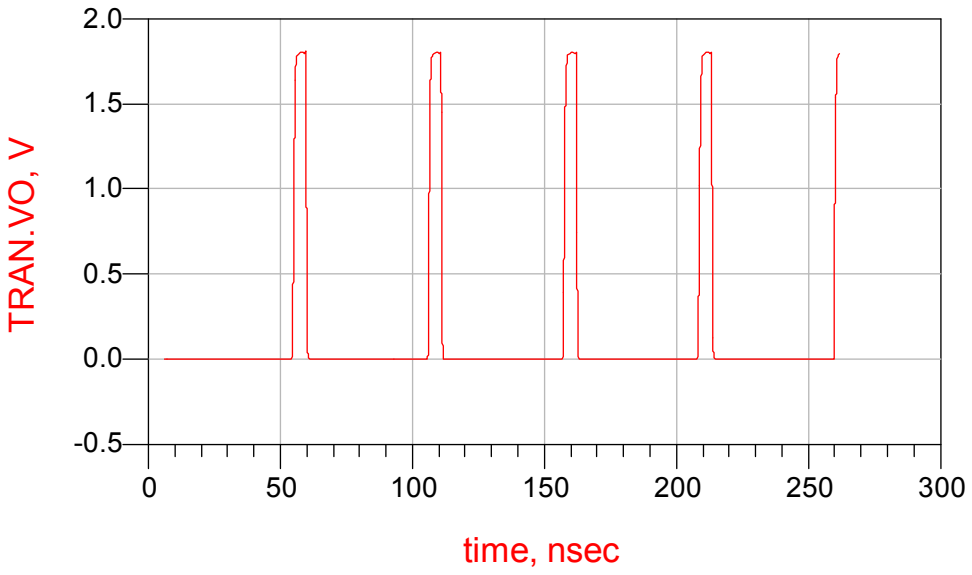


Fig. 5.3: Output Signal of the FD in Time Domain (/164, TT)

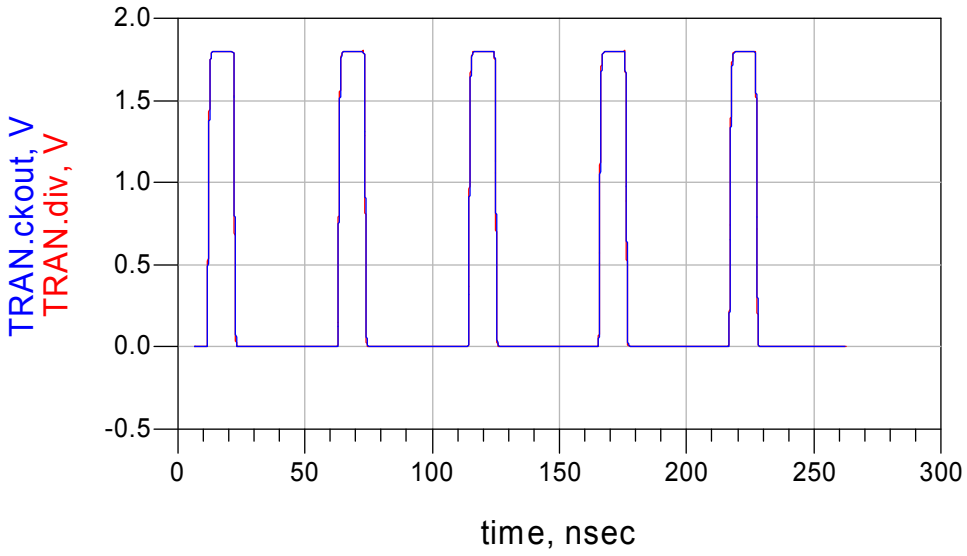


Fig. 5.4: Output Signal of the MMD in Time Domain (/164, TT)

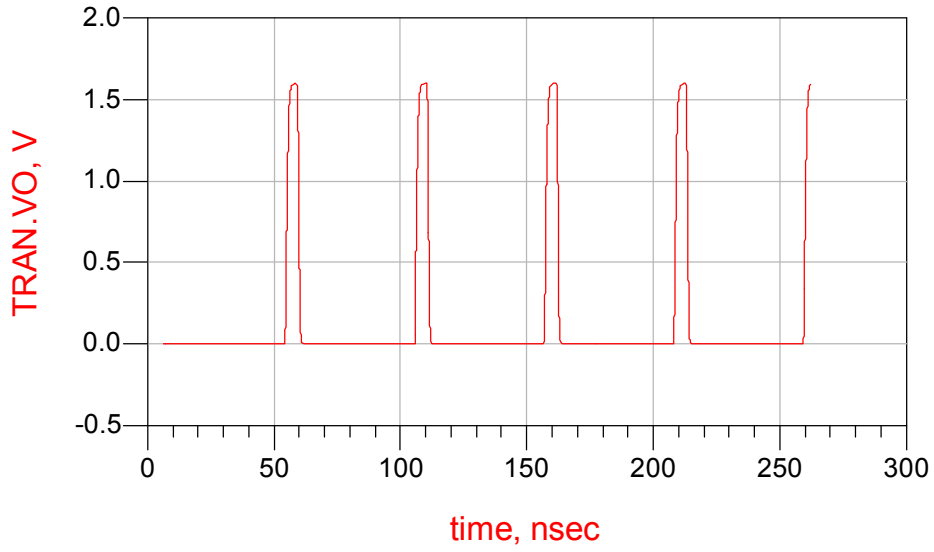


Fig. 5.5: Output Signal of the FD in Time Domain (/164, SS)

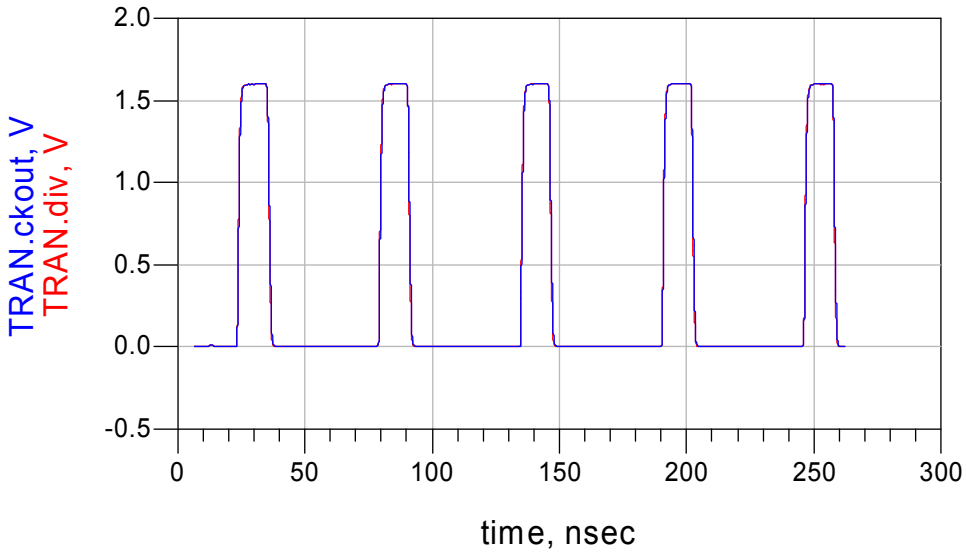


Fig. 5.6: Output Signal of the MMD in Time Domain (/164, SS)

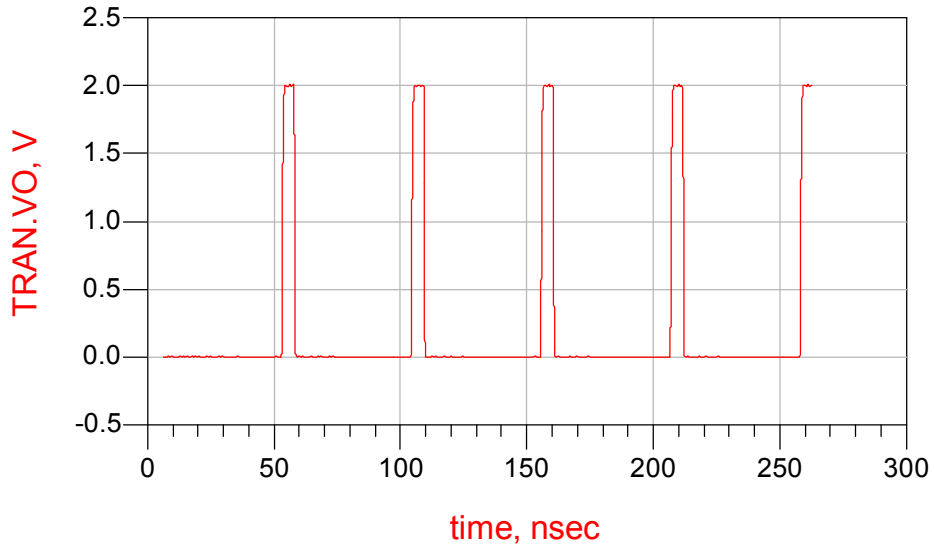


Fig. 5.7: Output Signal of the FD in Time Domain (/164, FF)

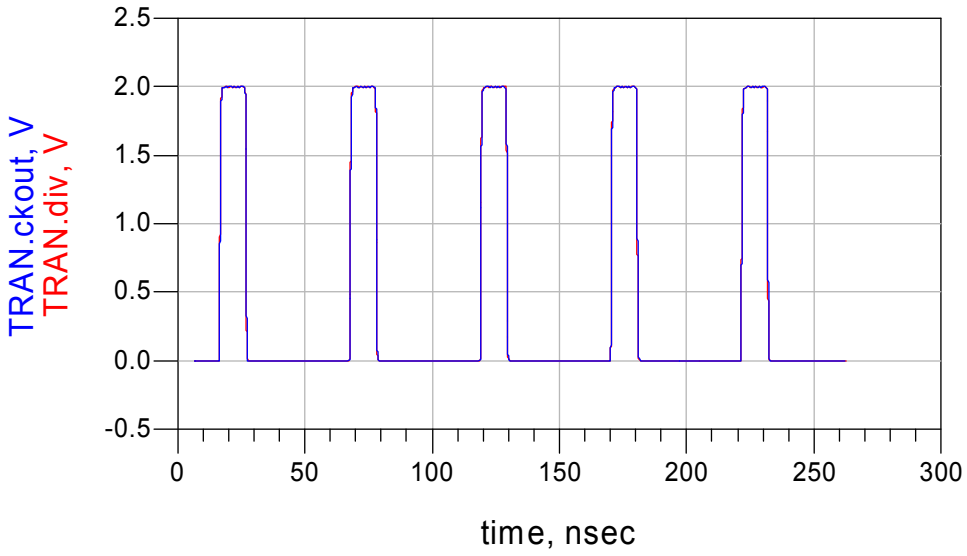


Fig. 5.8: Output Signal of the MMD in Time Domain (/164, FF)

The above results show the time domain output signals (/164) of the FD and MMD in different corners. It is obvious they have different duty cycles:

FD: 7.97%

MMD: 17.74%

Assuming M is the overall division range of the divider, the duty cycle of the FD can be written as:

$$\frac{\frac{1}{f_{in}/8}\times\frac{1}{2}}{\frac{1}{f_{in}/M}}=\frac{4}{M}, \qquad (1)$$

While the duty cycle of the MMD roughly equals: (the actual value depending on its actual structure)

$$\frac{\frac{1}{f_{in}/M'}}{\frac{1}{f_{in}/M}} = \frac{M'}{M}. \qquad (2)$$

Here, M' is the overall division ratio of the stages before the outputs.

From Eq. (1) and (2), it's easy to see the MMD will have a larger duty cycle than the FD, as long as M' is selected to be >4. Of course, the maximum M' available in MMD is determined by the minimum division ratio required.

The duty cycle is not important in the PLL integration, as long as the frequency detector of the PLL is edge-triggered.

**5.1.3. Frequency domain Results:**

To achieve the frequency domain results, an FFT analysis has been done to the transient results shown in Section 5.1.2. They are shown from Fig. 5.9 to Fig. 5.14. As stated in Section 5.1.2, in this design, the time domain output of the MMD has larger duty cycle than that of the FD, so in frequency domain, the output of the MMD has lower harmonic power. Frequency domain results also show us than the MMD generate much lower noise floor: more than -40dBc in TT compared to the about -20dBc noise floor of the FD. That is because MMD are constructed by only CML latches, the current of which is strictly constrained by the current sources, while the FD consists of CML latches as well as digital counters. The latter generate lots of glitches in transition, which increase the noise floor of the FD output.

Fig. 5.12 doesn't give out a clear spectrum output, because the MMD fails to function properly in SS condition with 3.2GHz input, which has been explained in another report on the MMD.

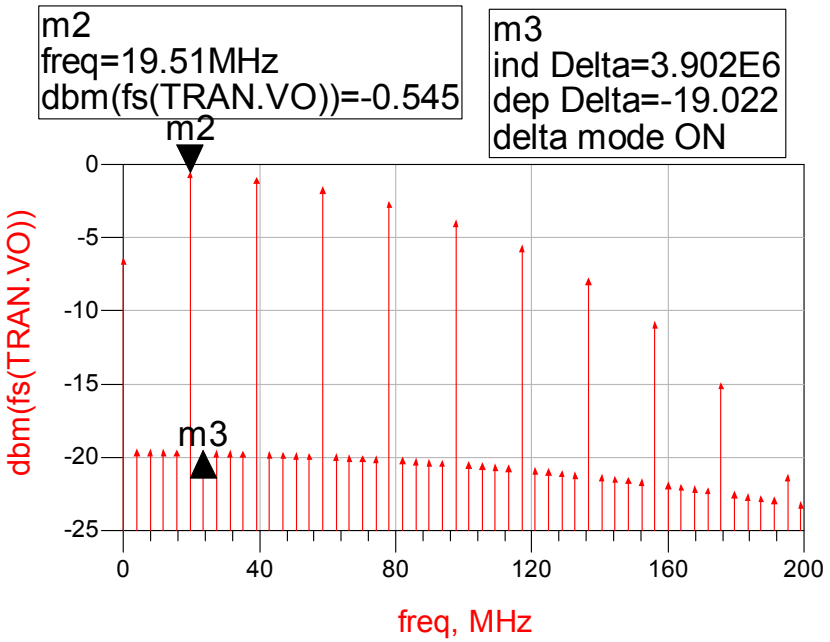


Fig. 5.9: Output Signal of the FD in Frequency Domain (/164, TT)

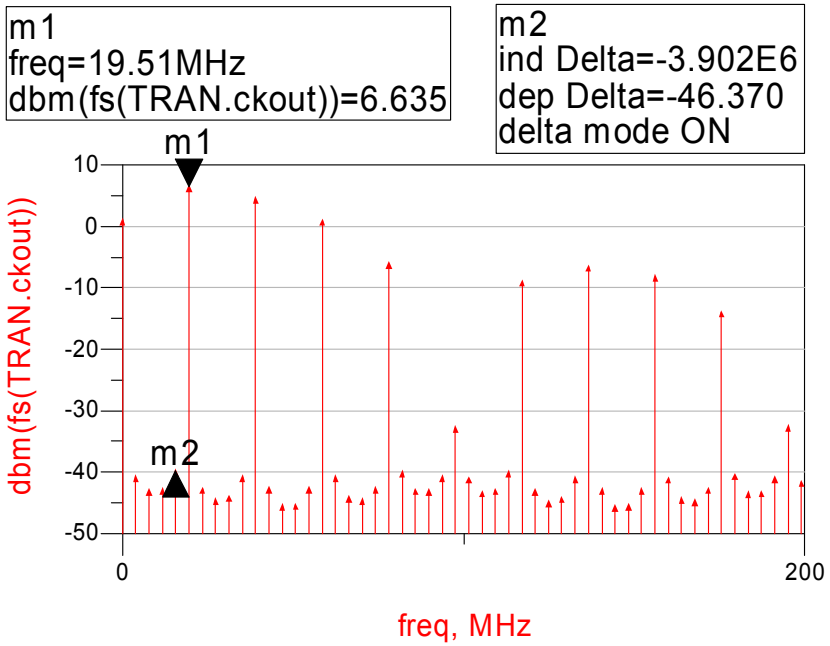


Fig. 5.10: Output Signal of the MMD in Frequency Domain (/164, TT)

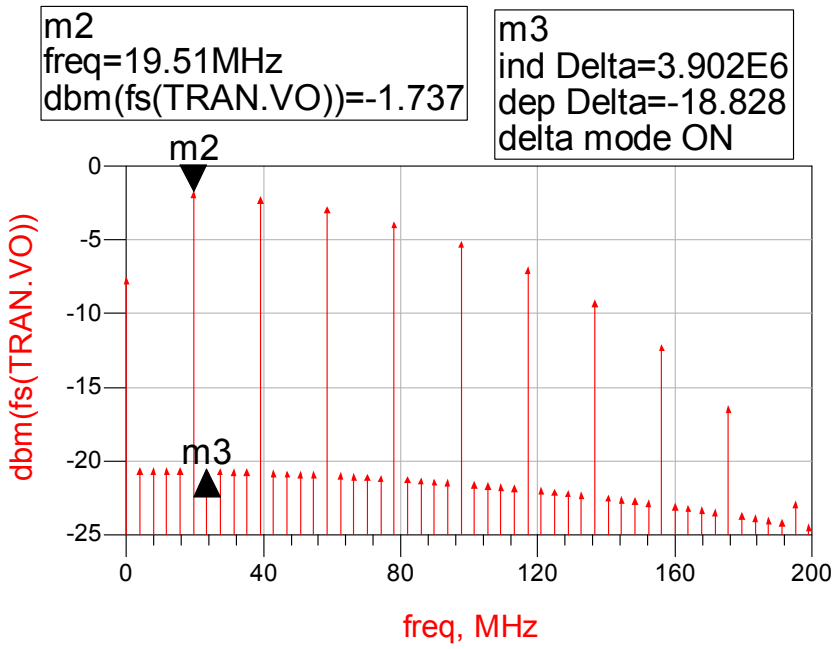


Fig. 5.11: Output Signal of the FD in Frequency Domain (/164, SS)

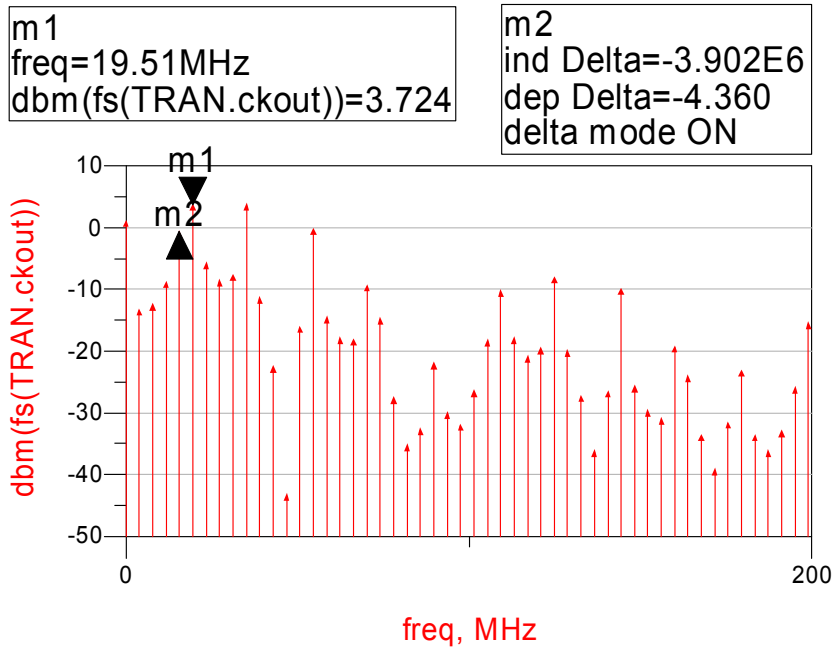


Fig. 5.12: Output Signal of the MMD in Frequency Domain (/164, SS)

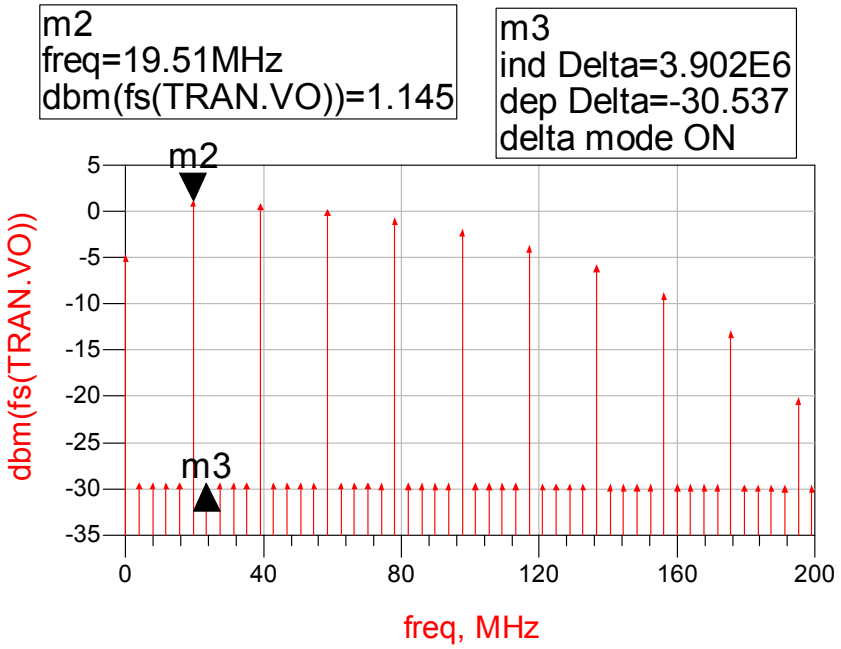


Fig. 5.13: Output Signal of the FD in Frequency Domain (/164, FF)

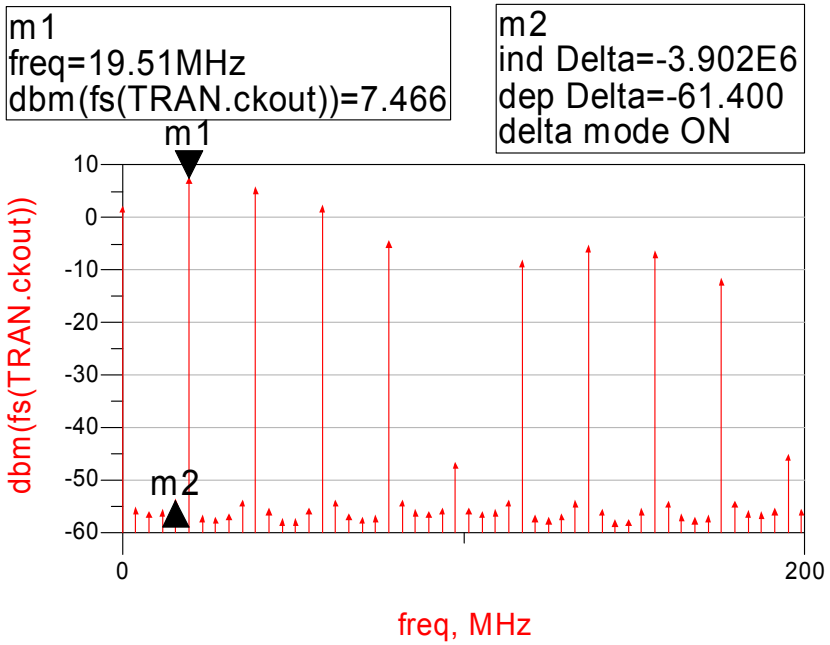


Fig. 5.14: Output Signal of the MMD in Frequency Domain (/164, FF)

## 5.2 Division Ratio = 192

### 5.2.1 Current Consumption

Table 5.2: Current Consumption of the Dividers (/192)

| | SS | TT | FF | Variation |
|---|---|---|---|---|
| FD | 1.50mA | 1.73mA | 2.04mA | -13.3% ~ +17.9% |
| MMD | 3.12mA | 4.07mA | 4.79mA | -23.3% ~ +17.7% |

The current consumption of the FD and MMD in Table 5.1 are almost the same as the results in Table 5.1.

### 5.2.2 Time Domain Results

The time domain results of division ratio = 192 is presented from Fig. 5.15 to Fig. 5.20. From these results, same conclusions can be drawn as in Section 5.1.

Duty cycles:

FD: 6.78%

MMD: 15.2%

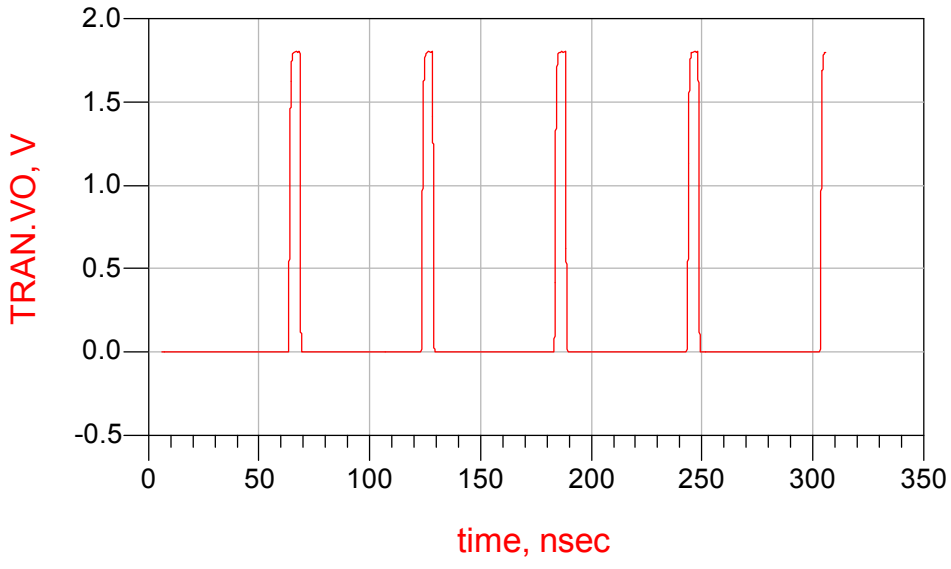


Fig. 5.15: Output Signal of the FD in Time Domain (/192, TT)

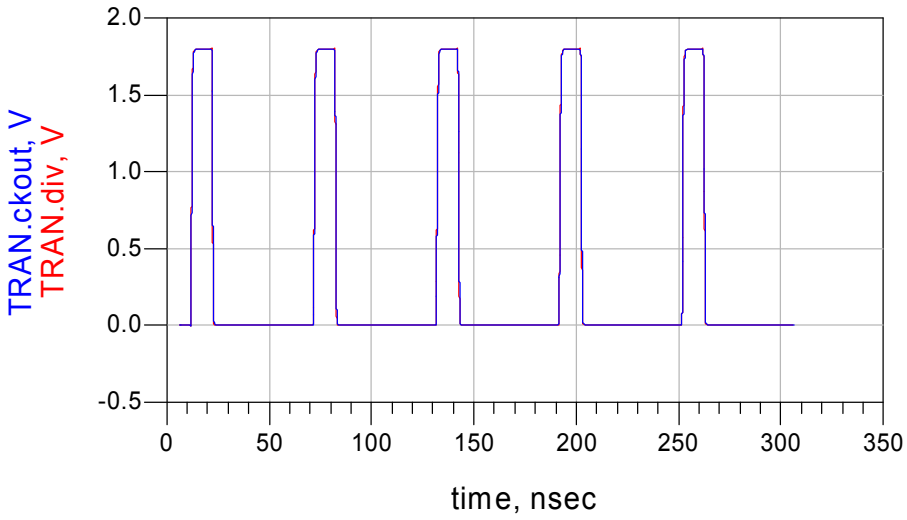


Fig. 5.16: Output Signal of the MMD in Time Domain (/192, TT)

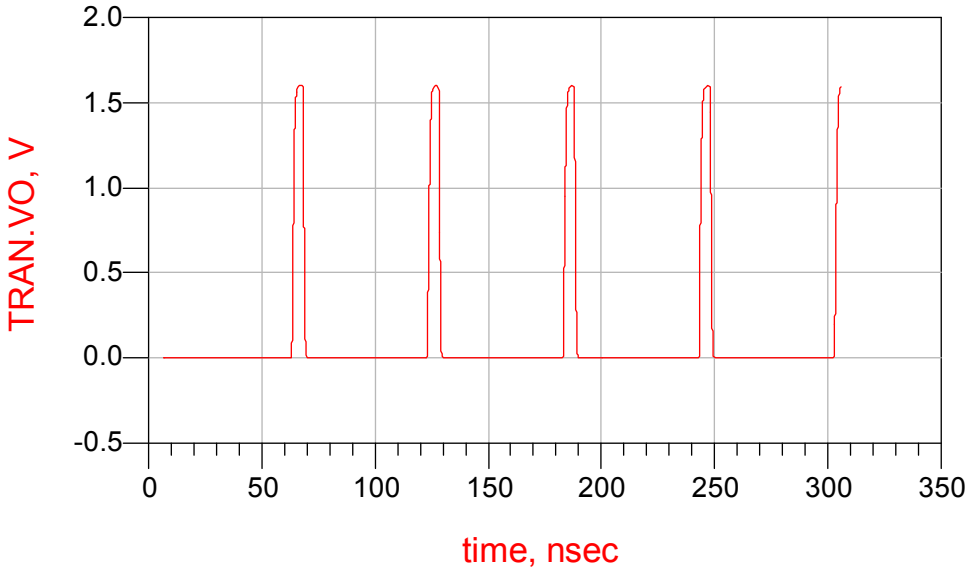


Fig. 5.17: Output Signal of the FD in Time Domain (/192, SS)

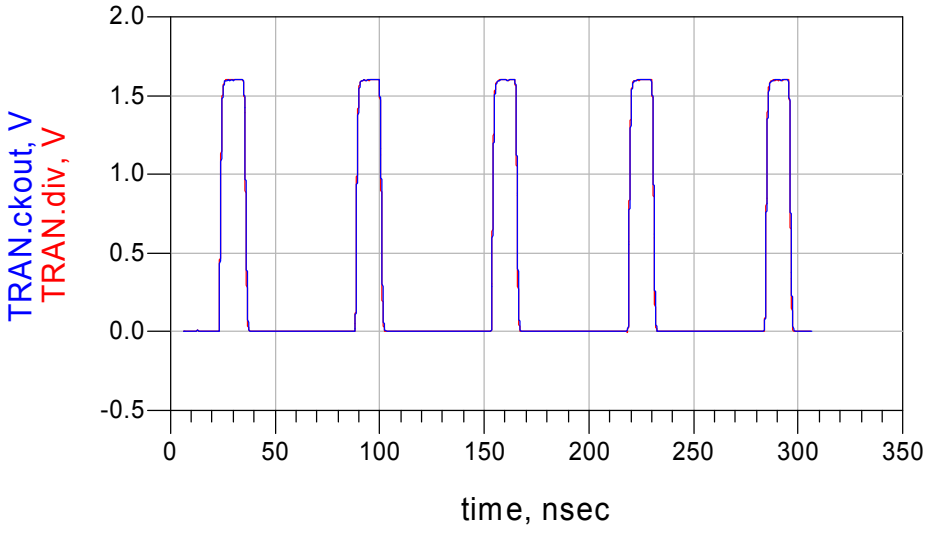


Fig. 5.18: Output Signal of the MMD in Time Domain (/192, SS)

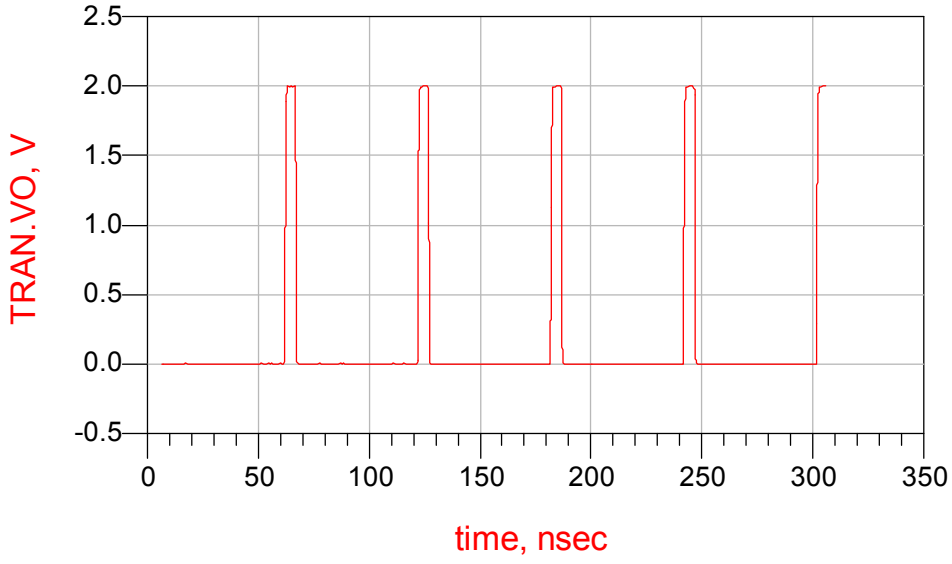


Fig. 5.19: Output Signal of the FD in Time Domain (/192, FF)

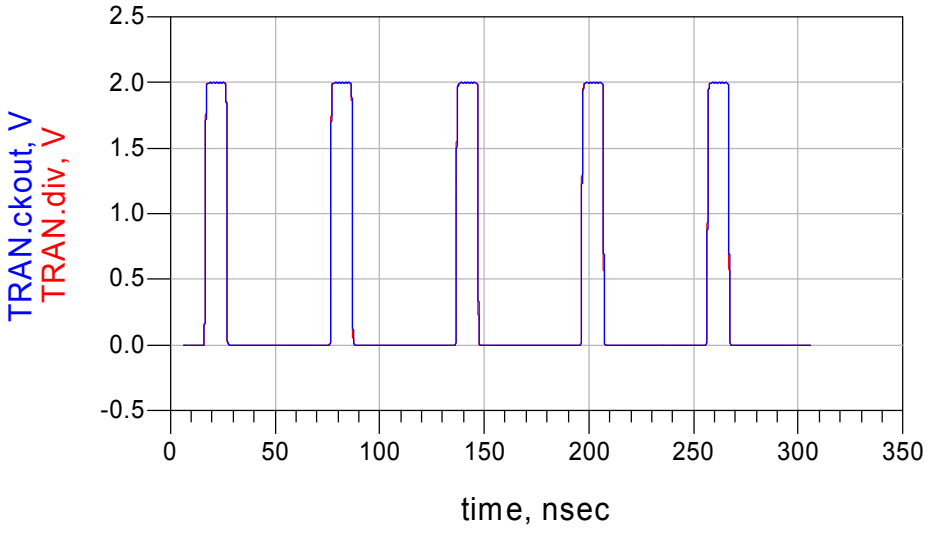


Fig. 5.20: Output Signal of the MMD in Time Domain (/192, FF)

### 5.2.3 Frequency Domain Results

The frequency domain results of division ratio = 192 is presented from Fig. 5.21 to Fig. 5.26. From these results, same conclusions can be drawn as in Section 5.1.

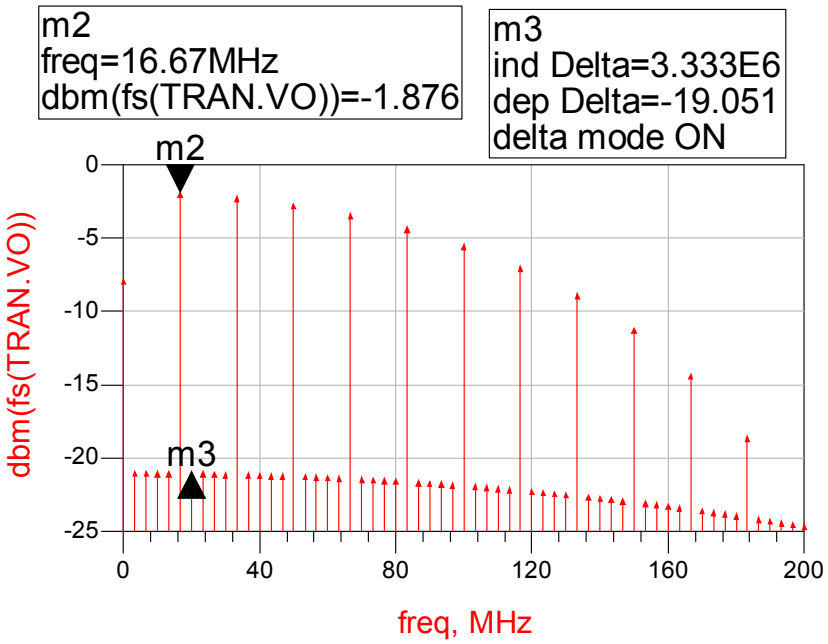


Fig. 5.21: Output Signal of the FD in Frequency Domain (/192, TT)

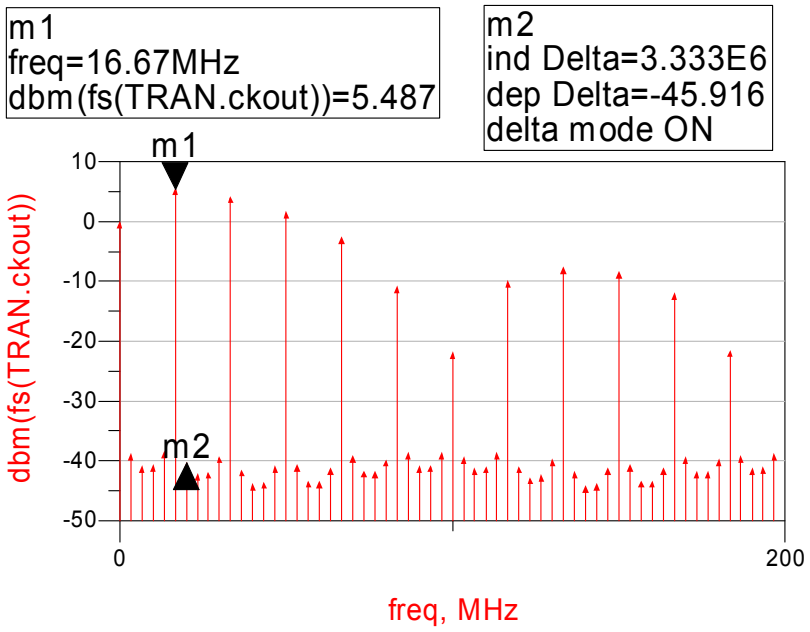


Fig. 5.22: Output Signal of the MMD in Frequency Domain (/192, TT)

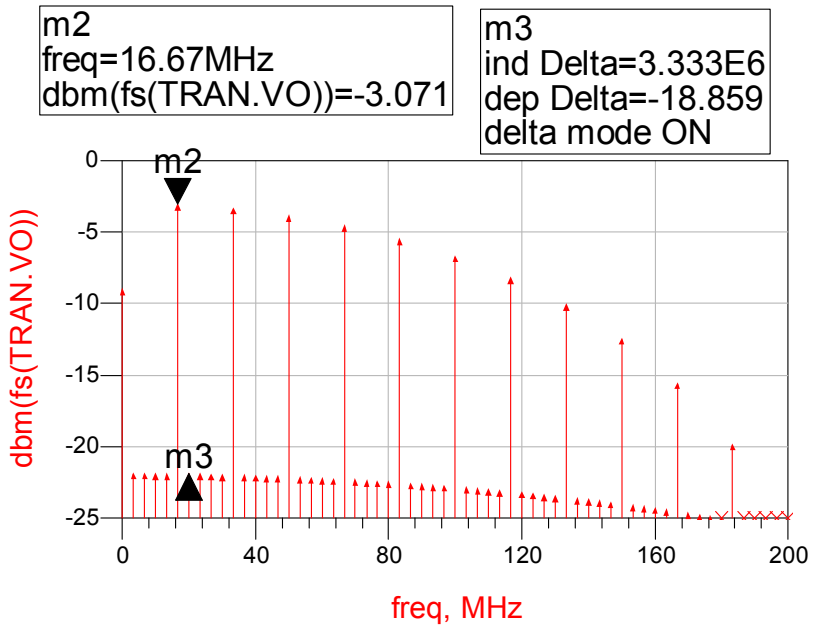


Fig. 5.23: Output Signal of the FD in Frequency Domain (/192, SS)

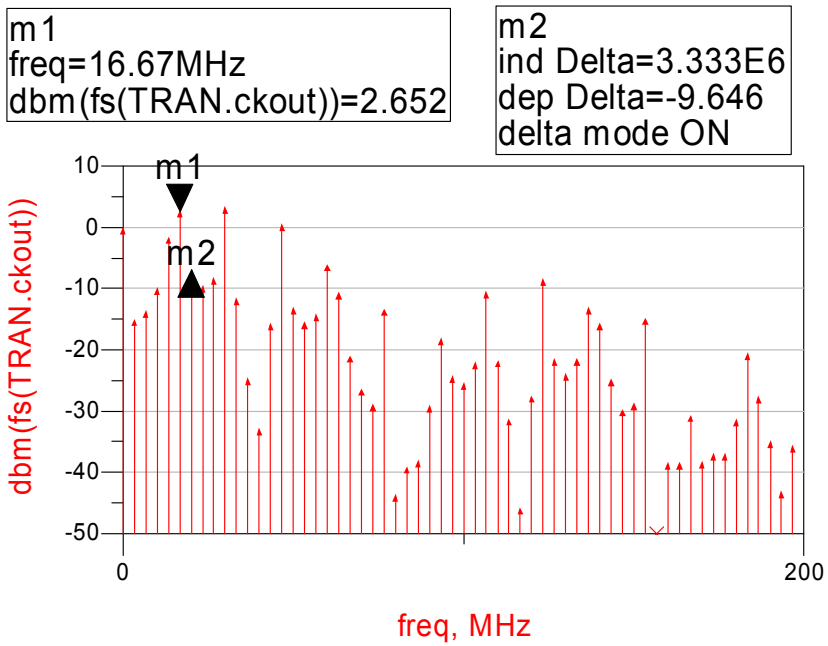


Fig. 5.24: Output Signal of the MMD in Frequency Domain (/192, SS)

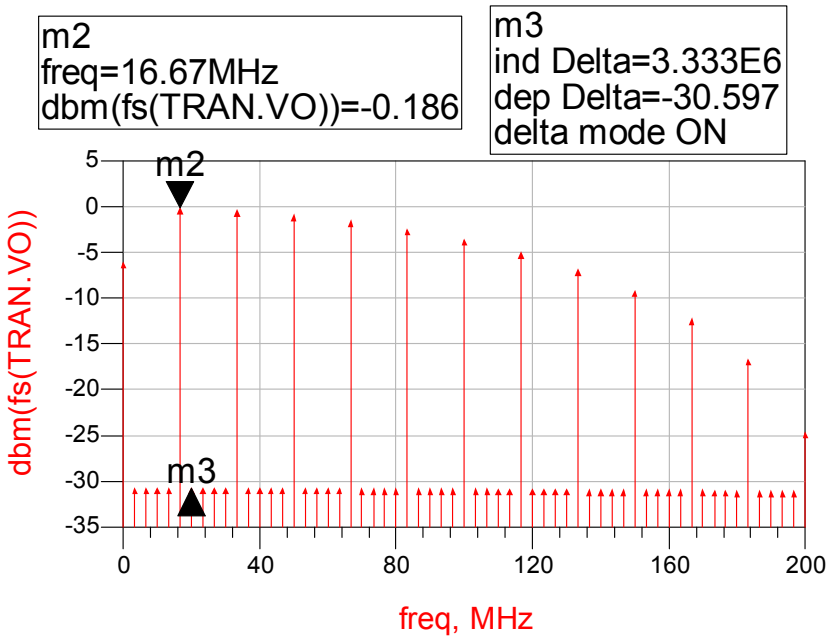


Fig. 5.25: Output Signal of the FD in Frequency Domain (/192, FF)

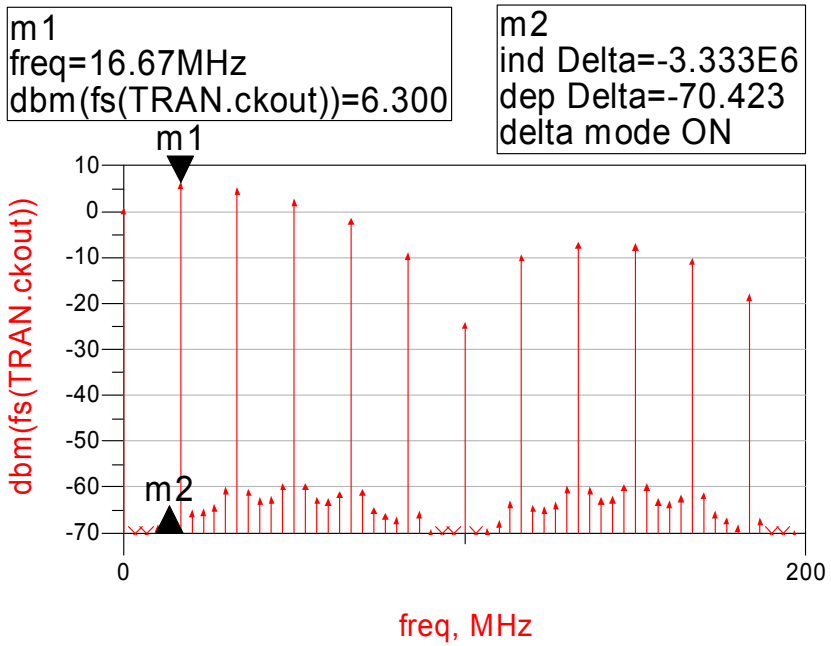


Fig. 5.26: Output Signal of the MMD in Frequency Domain (/192, FF)

## 5.3 Division Ratio = 510

### 5.3.1 Current Consumption

Table 5.3: Current Consumption of the Dividers (/510)

| | SS | TT | FF | Variation |
|---|---|---|---|---|
| FD | 1.48mA | 1.70mA | 2.01mA | -12.9% ~ +18.2% |
| MMD | 3.11mA | 4.05mA | 4.78mA | -23.2% ~ +18.0% |

The current consumption of the FD and MMD in Table 5.3 are almost the same as the results in Table 5.1 & 5.2.

### 5.3.2 Time Domain Results

The time domain results of division ratio = 510 is presented from Fig. 5.21 to Fig. 5.26. From these results, same conclusions can be drawn as in Section 5.1 & 5.2.

Duty cycles:

FD: 2.03%

MMD: 5.5%

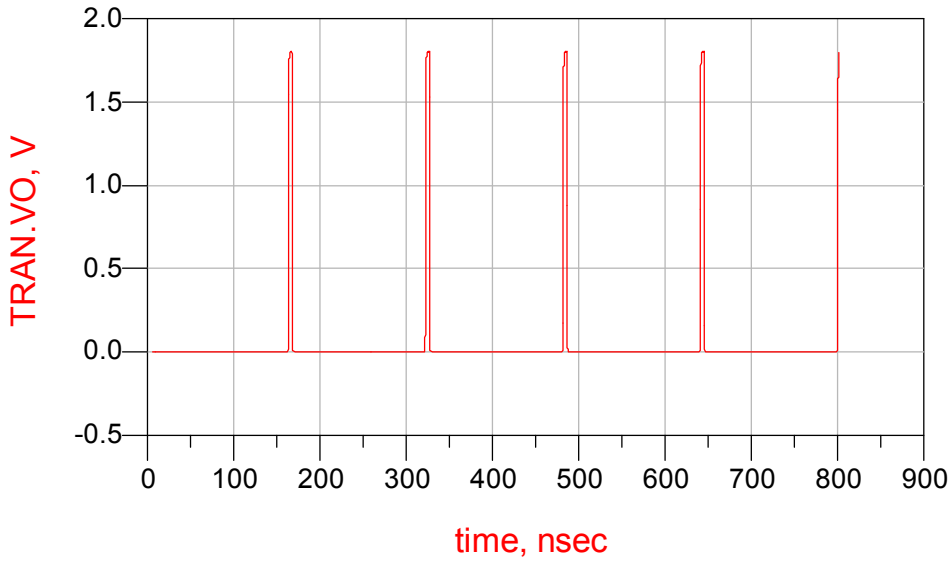


Fig. 5.21: Output Signal of the FD in Time Domain (/510, TT)

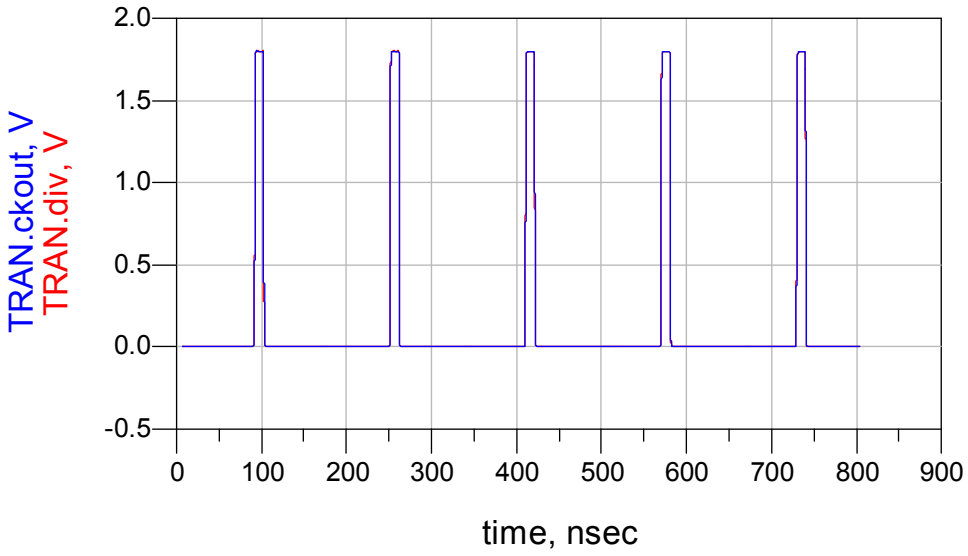


Fig. 5.22: Output Signal of the MMD in Time Domain (/510, TT)

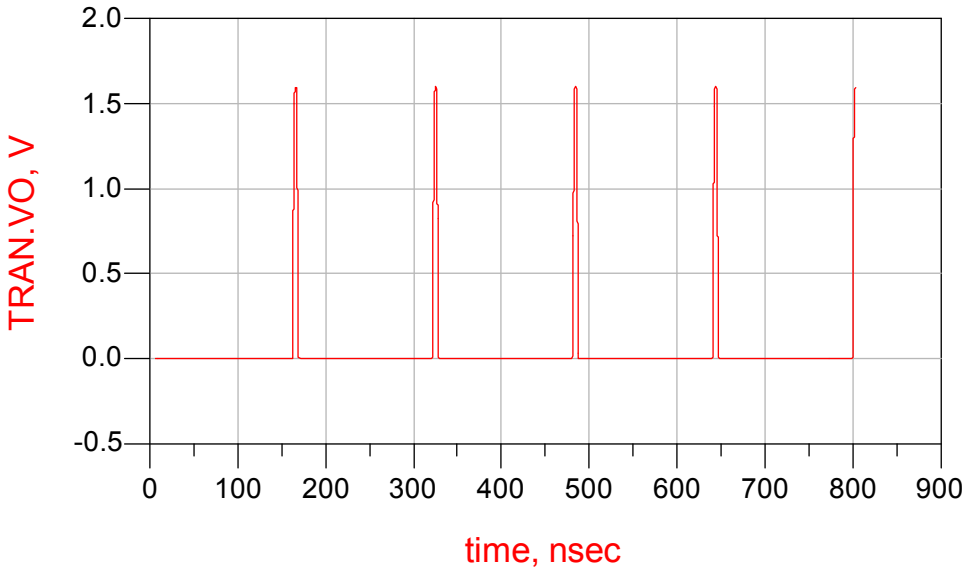


Fig. 5.23: Output Signal of the FD in Time Domain (/510, SS)

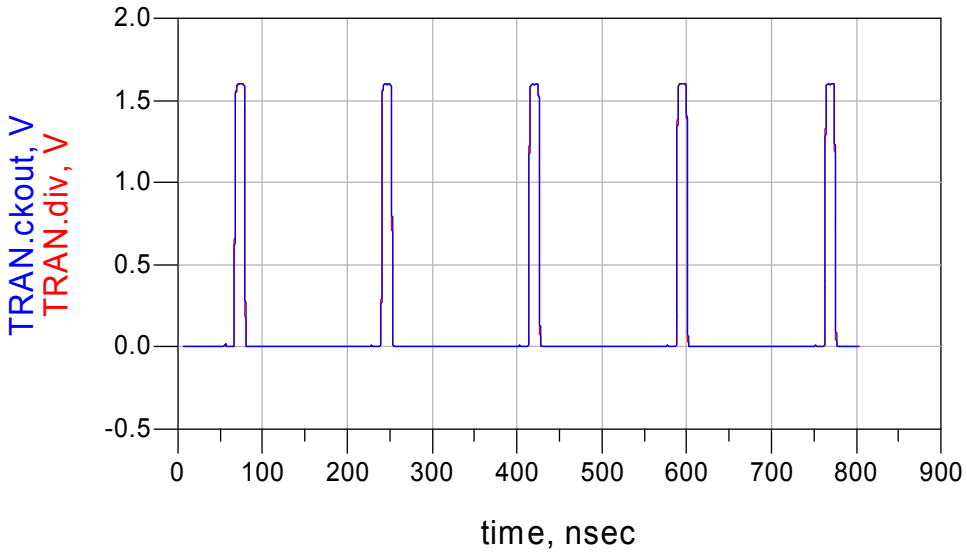


Fig. 5.24: Output Signal of the MMD in Time Domain (/510, SS)

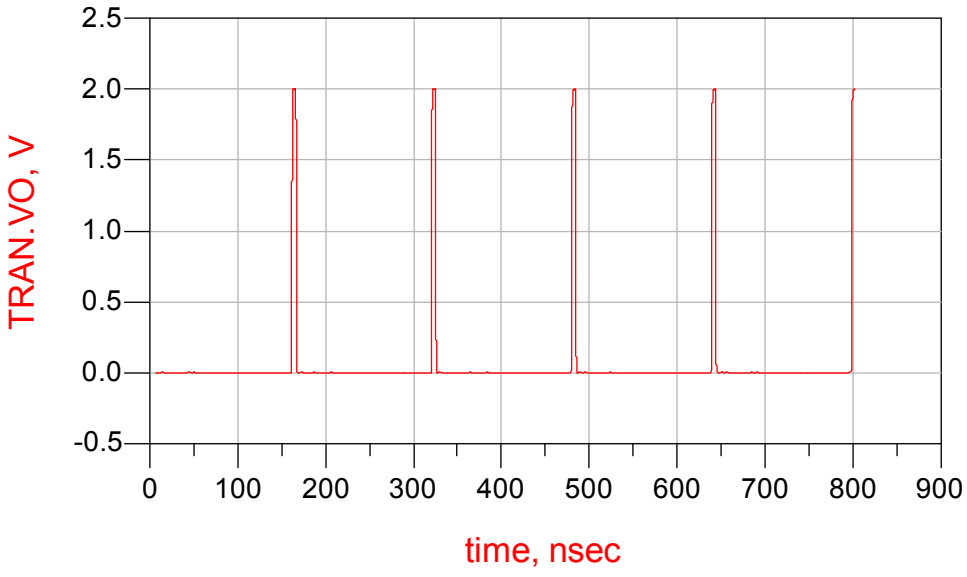


Fig. 5.25: Output Signal of the FD in Time Domain (/510, FF)

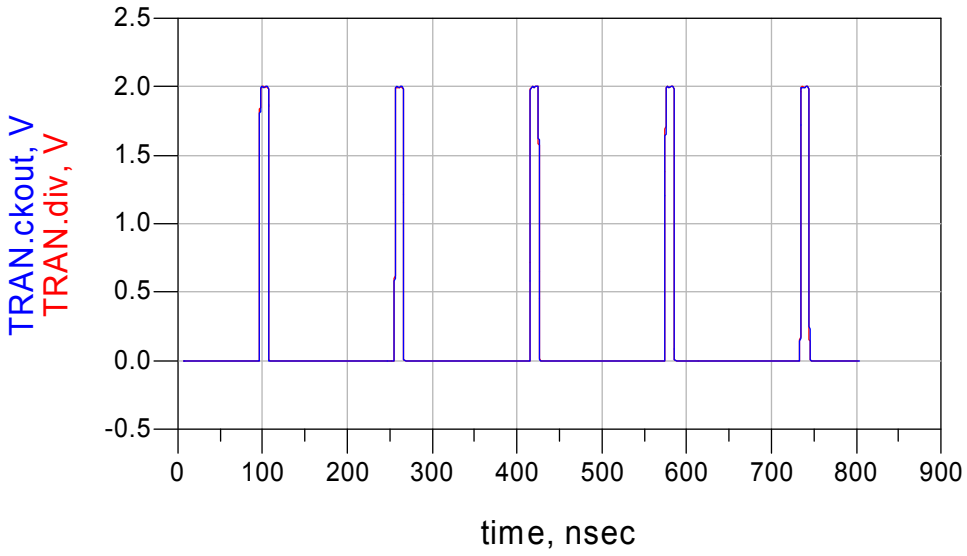


Fig. 5.26: Output Signal of the MMD in Time Domain (/510, FF)

### 5.2.3 Frequency Domain Results

The frequency domain results of division ratio = 510 is presented from Fig. 5.27 to Fig. 5.32. From these results, same conclusions can be drawn as in Section 5.1 & 5.2.

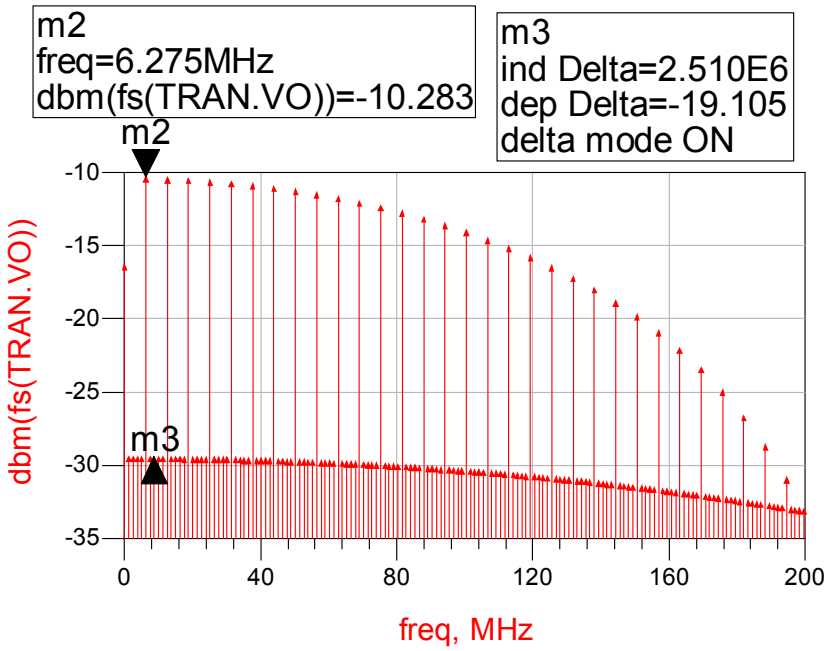


Fig. 5.27: Output Signal of the FD in Frequency Domain (/510, TT)

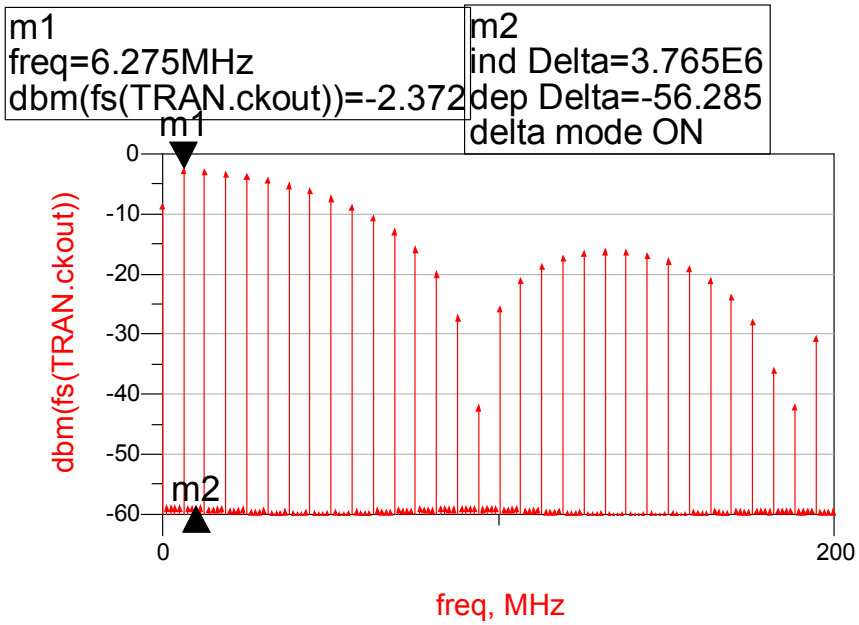


Fig. 5.28: Output Signal of the MMD in Frequency Domain (/510, TT)

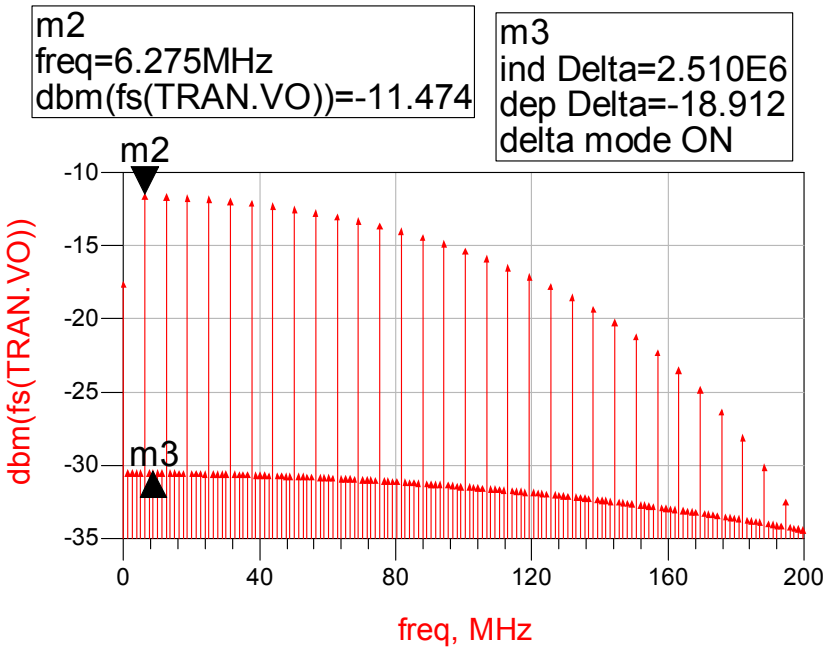


Fig. 5.29: Output Signal of the FD in Frequency Domain (/510, SS)

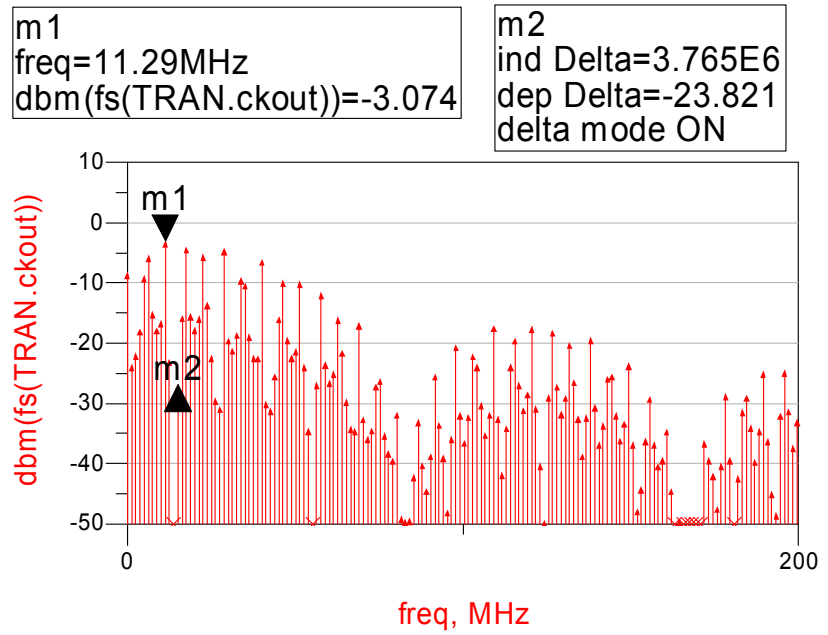


Fig. 5.30: Output Signal of the MMD in Frequency Domain (/510, SS)

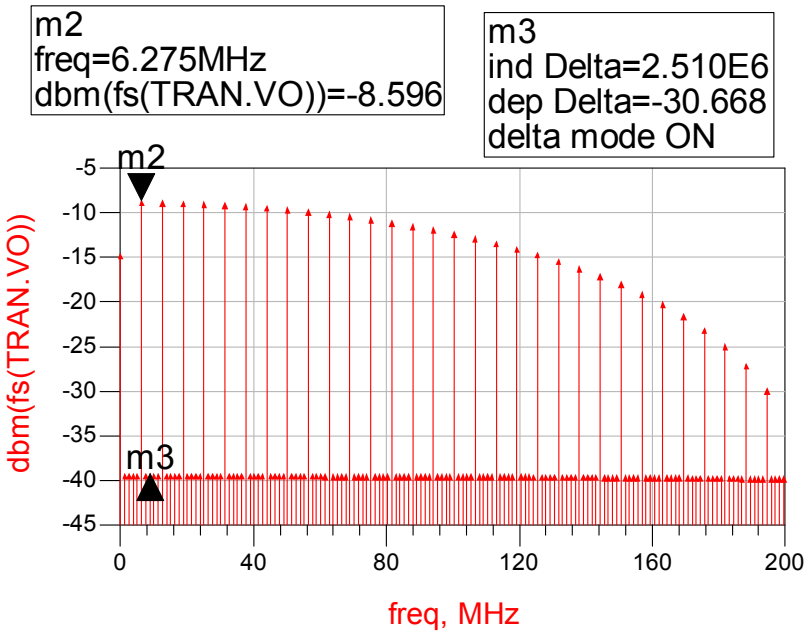


Fig. 5.31: Output Signal of the FD in Frequency Domain (/510, FF)

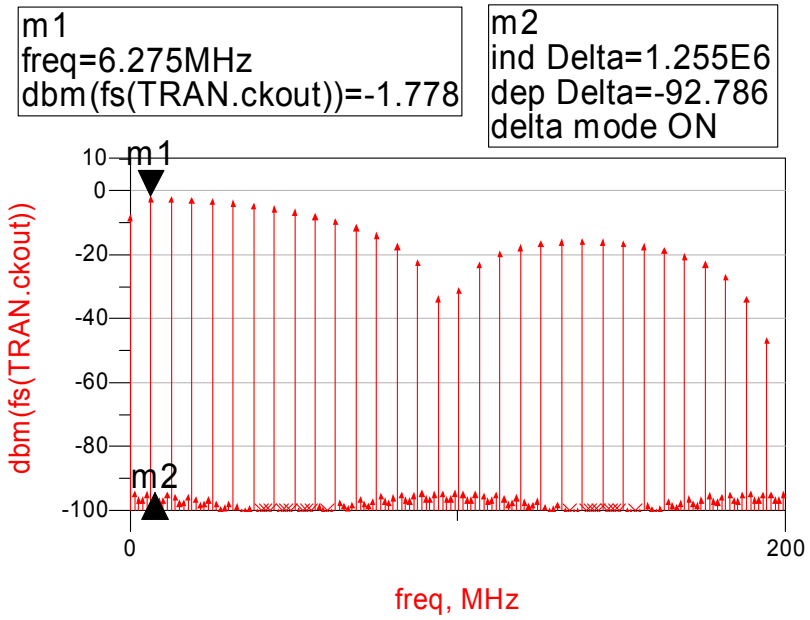


Fig. 5.32: Output Signal of the MMD in Frequency Domain (/510, FF)

# 6. Conclusions

1. The MMD has better spectrum purity than the FD, due to its better duty cycle. But it may not be important in PLL design, as long as the frequency detector of the PLL is edge-triggered.
2. The MMD has lower noise floor than the FD, because MMD are constructed by CML latches, the current of which is strictly constrained by the current source, while the FD consists of CML latches as well as digital counters, which generates lots of glitches in transition.
3. The MMD requires more power than the FD. The FD only employs the power hungry CML latches at higher frequency. Digital counters are used at low frequency in the FD. Furthermore, only one div-by-2/3 prescaler are implemented in the FD. However, the MMD use all CML latches along the divider chain to its outputs, and except the first stage, all prescalers in the MMD are div-by-2/3 circuits.
4. Due to its modularity, the MMD design requires less time and effort.

# 7. Reference


[1] C. Lam and B. Razavi, "A 2.6-GHz/5.2GHz Frequency Synthesizer in 0.4-um CMOS Technology", *IEEE J. Solid-State Circuits*, Vol. 35, No. 5, pp. 788-794, May 2000.

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