A 1.8V-5V DC/DC Booster Design Using XFAB XC06 0.6um Process

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1. Introduction:

This is a 1.8V to 5.0V DC/DC booster design using XFAB XC06 0.6um process. The control method of this booster is constant Ton and the steady-state operating mode is DCM.

The simulation result shows that, the current consumption of the Booster IC is around 1mA while efficiency is 78% at 1.5V battery voltage supply.

In photoflash charger, a NMOS power switch is required for the flyback converter. An IGBT is also needed to trigger the flash light. The drivers require a higher voltage such as 3V or more in order to driver the NMOS and IGBT efficiently. However, battery voltage could be as low as 1.5V and renders the driving of NMOS and IGBT inefficient.

Moreover, the Picasso PFC IC itself needs to operate at about 2.8V. It is also difficult to design the PFC IC to operate at 1.8V using XC06 process without tradeoff with some performance parameters. If necessary, PFC IC could also draw it voltage supply from the booster. The expected current consumption of PFC IC is about 5mA. The booster is designed to be able to provide 10mA of constant current drain.

This booster is designed to provide the supply voltage for PFC IC, NMOS driver and IGBT driver. The design targets include:

1. Able to operate at low battery voltage of 1.8V;
2. Minimize the number of external components;
3. Lower down the peak charging current in order to use small profile chip inductor.

The external components of the booster are:

1. A small inductor, 22uH, Isat ≥ 400mA, Ipeak ≥ 500mA.
2. Output capacitor: 10uF, low ESR.
3. Input decoupling capacitor.

2. Features of the booster:

2.1 Internal Synchronous Rectifier:

The booster uses an internal PMOS as a synchronous rectifier and thus no external diode is required.

2.2 Shutdown Output Load Disconnect:

When the chip is shut down, the output load and the chip is disconnected. This prevents the flow of leakage current from battery to the output.

2.3 Low Voltage Startup:

It is difficult to design circuit to work at 1.8V using XC06 with good performance. To overcome this limitation, a “Low Voltage Startup” method is used. Only the “Low Voltage Startup”circuit needs to function at 1.5V or during the startup phase. After startup, the circuit gets the supply voltage from the output capacitor instead from the battery and the startup circuit is disabled. Hence, only the “Low Voltage Startup” circuit need to operate at low voltage and its performance degradation is acceptable as long as the circuit can startup properly.

Once the boost startup, the battery voltage can drop down to as low as 1.3V without affecting the operation of the circuit. The only limitation in the application is the ability of the battery to supply sufficient energy to the output.

2.4 Under Voltage Lockout:

After the output voltage is boosted to the target voltage (5V for this design), any significant drop of the output voltage is considered to be an abnormal condition. This could be caused by a heavy load plug in or battery voltage drop to below 1.3V. In this situation, the Under Voltage Lockout function will be triggered and the chip will enter into power down mode. To release the chip from this mode, user needs to either cut off the battery power supply for a while or toggle the shutdown pin (SHDN).

2.5 Anti-ringing Control:

During DCM, the voltage at one of the inductor terminal will ring. To minimize EMI during the voltage ringing, anti-ringing control is implemented in the booster design.

2.6 Current Limit:

Peak charging current is limited to be 300mA. During the entire operation, the inductor current will not exceed 300mA. This allows the use of small size chip inductor.

3. Block Diagram:

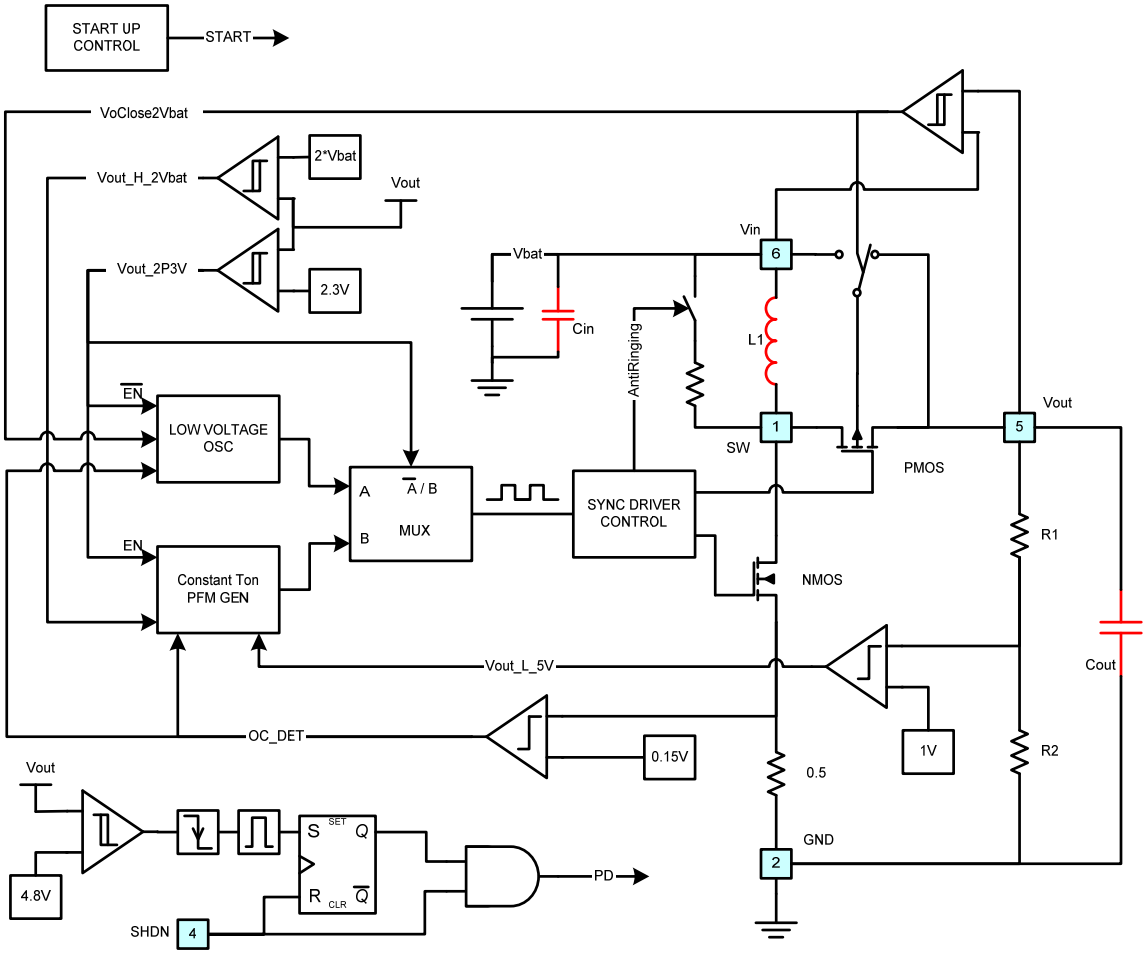

Figure 1 Block diagram of the booster.

4. Startup Flow:

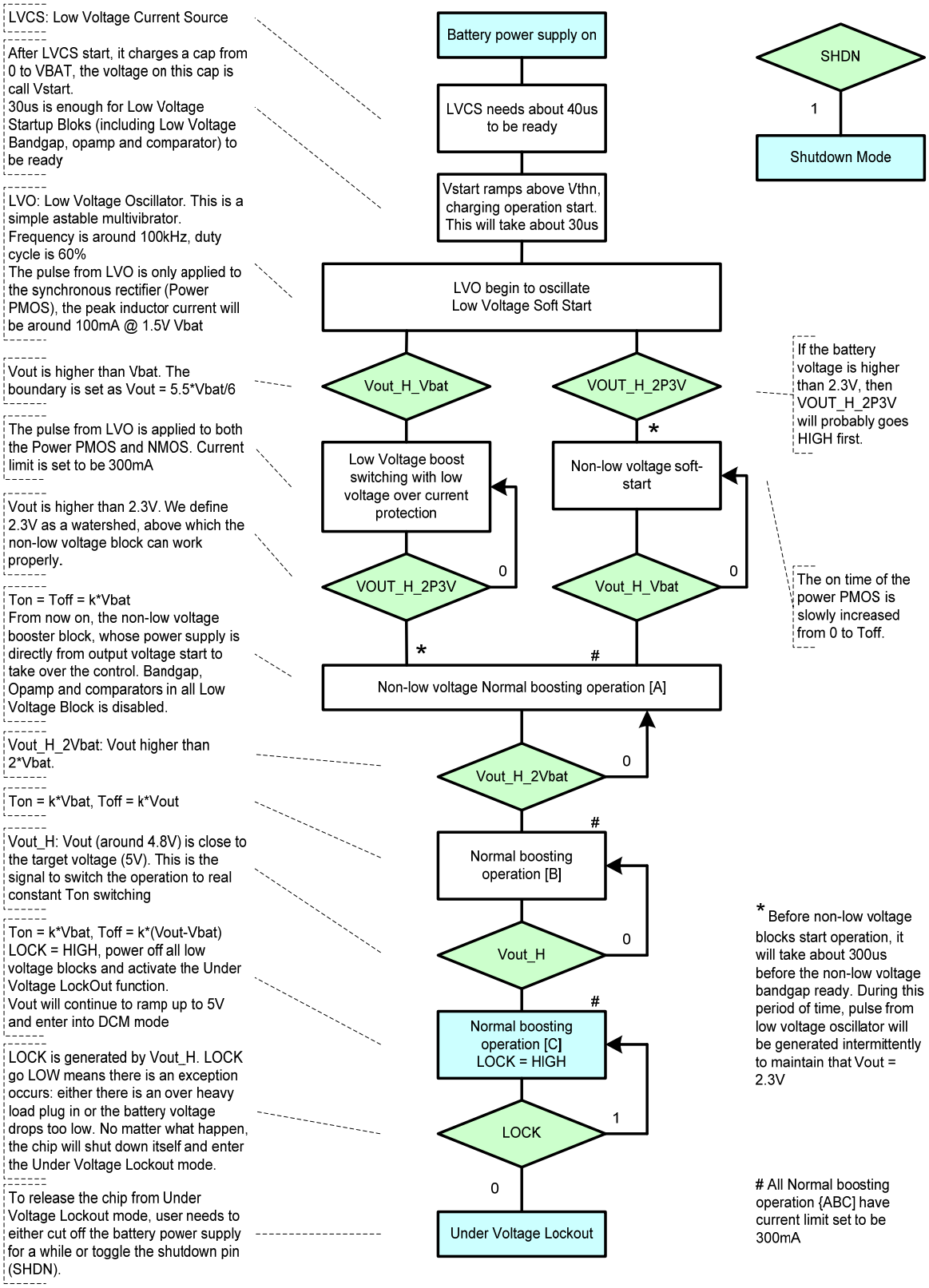

Figure 2 Booster Startup Flow.

Note 1: Depending on the battery voltage, the startup flow will go through one of two paths. If Vbat is less than 2.3V, during charging, Vout will go higher than Vbat before it goes higher than 2.3V, thus the startup flow goes through the left path. On the other hand, if Vbat is higher than 2.3V, then the startup flow will go through the right path.

Note 2: The reason why the low voltage blocks are not used to control the entire boosting operation is that, the low voltage blocks are designed to work under a supply voltage a little bit higher than the threshold voltage of the 0.6um process, these circuits seem a little tricky. They are not as fast, accurate and reliable as the non-low-voltage block. Their task is to work in open loop in order to boost the output voltage to a level that the non-low-voltage blocks can take over the control.

Note 3: About the three normal boosting operation. The real constant Ton will only be applied after Vout_H goes high, or Vout ramp up to a level very close to the target voltage. Before that, the Toff time is not derived from the constant Ton emulation prediction, it is fixed in fact. The reason why Toff is fixed during the startup transient is that the synchronized rectifier, or power PMOS, should be properly opened before the inductor current drops to zero. In practice, we need to provide an offset of the real Toff time, or make Toff early, to ensure the PMOS can be turned off in time. However, during the startup transient, this amount of offset is not easy to define. If the offset time is not large enough, reverse inductor current will appear and the startup will probably fail. On the other hand, if the offset time is set too large, it will greatly reduce the efficiency when the booster is working in DCM mode (Vout reaches 5V). Base on the discussion above, under different Vout level, Toff is set to different value:

1. Vbat < Vout < 2*Vbat: Ton = Toff = k*Vbat; (k is a constant);
2. 2*Vbat < Vout < 5V: Ton = k*Vbat, Toff = k*Vout;
3. Vout = 5V: Ton = k*Vbat, Toff = k*(Vout – Vbat). (DCM mode, real constant Ton operation).

5. Some Important Signals Descriptions:

Important Signal		Descriptions	HIGH	LOW
ON/OFF Control	SHDN	SHDN is the external signal to cut power supply of all blocks.	Power down, turn PD HIGH	Power up if now Under Voltage Lockout
	START	After power up, START will remain LOW for about 50us to allow all block of the chip to startup and be stable, then it go HIGH, the chip begins to operate	Chip starts to operate	The chip is powered up, but not operating
	LOCK	Once the output voltage ramp up close to the target voltage (5V), LOCK goes HIGH: 1. disable the Bandgap, OPAMP and Comparator in the Low Voltage Startup Circuit (LVSC). Ensuring the booster remains in that working condition even without LVSC. 2. Switch t	Disable the Bandgap, OPAMP and Comparator in the Low Voltage Startup Circuit	In UVLO, turns PD HIGH, shutdown the chip
	REF_READY	Once the output voltage ramp up to around 2.3V, the non-low voltage blocks get sufficient supply to operate, but it will take about 300us before the bandgap ready,	Non-low voltage bandgap is ready	Non-low voltage bandgap is not ready
	PD	Power Down signal.	Chip power down	Chip power up
Judgment Signal	Vout_H_Vbat	Vout higher than Vbat. Its actual meaning is Vout close to Vbat. The boundary is Vout = 5.5*Vbat/6	Exit low voltage soft start mode	Low voltage soft start mode
	VOUT_H_2P3V	Vout higher than 2.3V. We define 2.3V as a watershed, above which the Non-low voltage block can work properly.	Normal booster block, whose power supply is directly from output voltage start to take over the control. Bandgap, OPAMP and comparators in all Low Voltage Block is shutdown.	Low voltage blocks control the boost operation
	Vout_H_2Vbat	Vout higher than 2*Vbat.	When Vout_H=LOW, Ton=k*Vbat, Toff=k*Vout	Ton=Toff=k*Vbat
	Vout_H	Vout (around 4.8V) is close to the target voltage (5V). This is the signal to turn the chip to Real Constant Ton switching operation and switch into the under voltage lockout mode	Ton=k*Vbat, Toff=k*(Vout-Vbat), LOCK turn HIGH	In UVLO, turns LOCK LOW and enter UVLO
	Vout_L_5V	Vout Lower than 5V. Output voltage sensing feedback signal	Vout lower than 5V, trigger a single pulse to charge Vout	Vout higher than 5V
	OC_DET	Over Current Detected. This signal monitor the inductor current when the power NMOS is conduct.	Current exceed the limited level (300mA), shut down the power NMOS	

6. Detail Descriptions:

6.1 Low Voltage Biasing Current Source:

At low voltage supply (1.8V), a reference current source is needed to supply the basic block such as OPAMP and comparator. This bias current does not need to be very accurate and fast, but it should be:

1. Able to start operation at very low voltage (lower than 1.8V).
2. The current bias should not vary too much in a very wide range of supply voltage (from 1V to 5V).
3. The circuit should be simple and consume little power.

The low voltage biasing current source used [1] is shown in Figure 3.

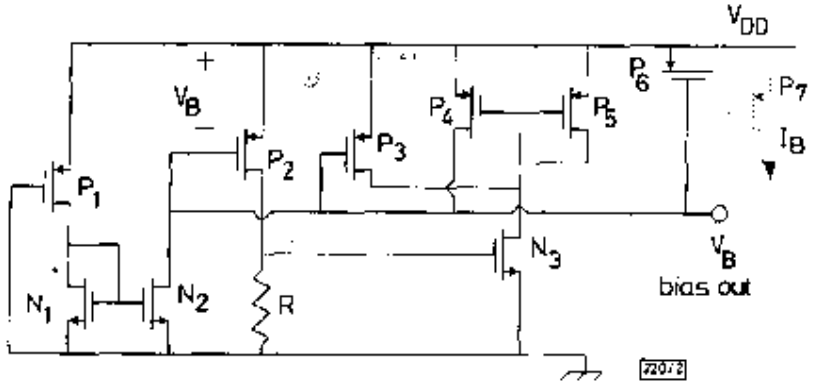

Figure 3 Low-voltage CMOS bias circuit. [1]

6.2 Low Voltage Bandgap:

The non-low-voltage blocks will take over the boosting operation when the output voltage rises to around 2.3V. Prior to that, only the low voltage blocks are working. A low voltage comparator is needed to compare the output voltage with reference voltage (scale version of 2.3V). This reference voltage level is generated by a low voltage Bandgap. The Bandgap Voltage Reference [2] is shown in Figure 4. The bias current generated by the Low Voltage Bandgap could be used to bias all the low voltage OPAMP and comparators. However, this is not done. The reason is that it was found during simulation that it is not easy to tune the Low Voltage Bandgap when its own current source is being used to bias its own OPAMP. Since the biasing current is not necessarily to be accurate with respect to supply voltage and temperature, the Low Voltage Biasing Current Source as mentioned above is used.

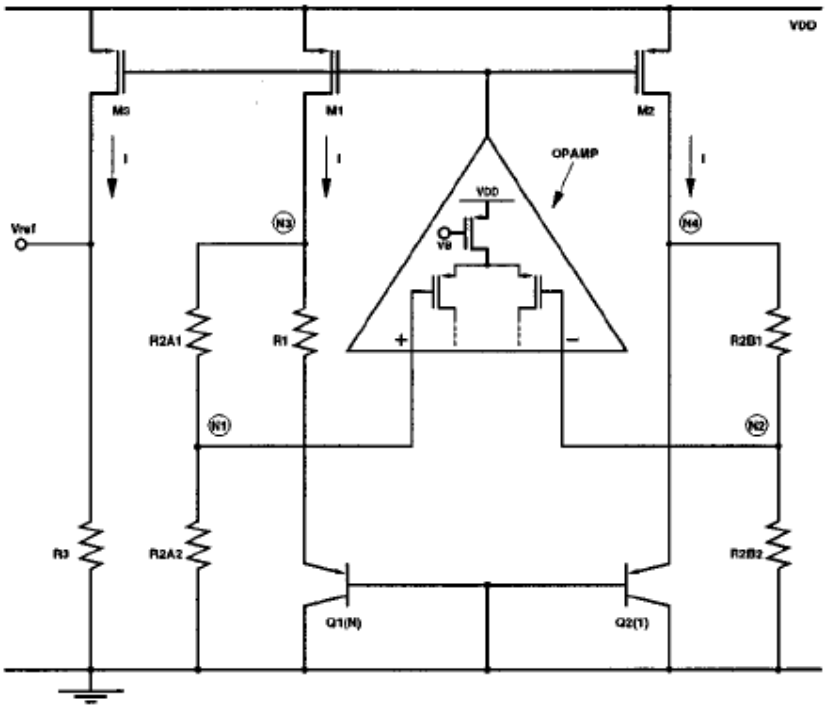

Figure 4 Low Voltage Bandgap. [2]

6.3 Power Supply Switch:

To shut down the synchronous rectifier, or power PMOS, is not straightforward. Gate and substrate of the power PMOS should be tied to the highest voltage level to off the PMOS. Since the output voltage can be anywhere from 0V (when there is no battery or in shutdown mode) to 5V, the "highest level" will be either the battery voltage or output voltage. A low voltage control switch that can switch power supply between these two sources is needed. It must also prevent leakage current from flowing.

As shown in Figure 5, SW2 is turned on when Vout is less than Vbat. Thus Vdd_driver = Vbat. At the same time, SW1 is turn off preventing current flow from Vdd_driver to Vout. The situation is reversed when Vout is higher than Vbat. SW1 and SW2 are One Way Current Switch. Its circuitry is shown in Figure 6.

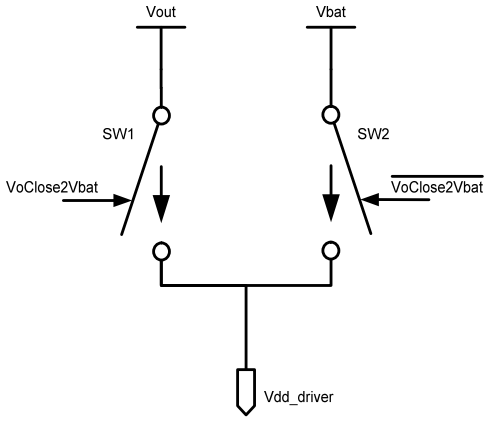

Figure 5 Power Supply Switch.

The function of the One Way Current Switch is:

1. When Vin > Vout: SW = HIGH, SWITCH conducts and provides a current path from Vin to Vout.
2. When Vin < Vout: SW = LOW, SWITCH not conducts and prevents current flowing from Vout to Vin.

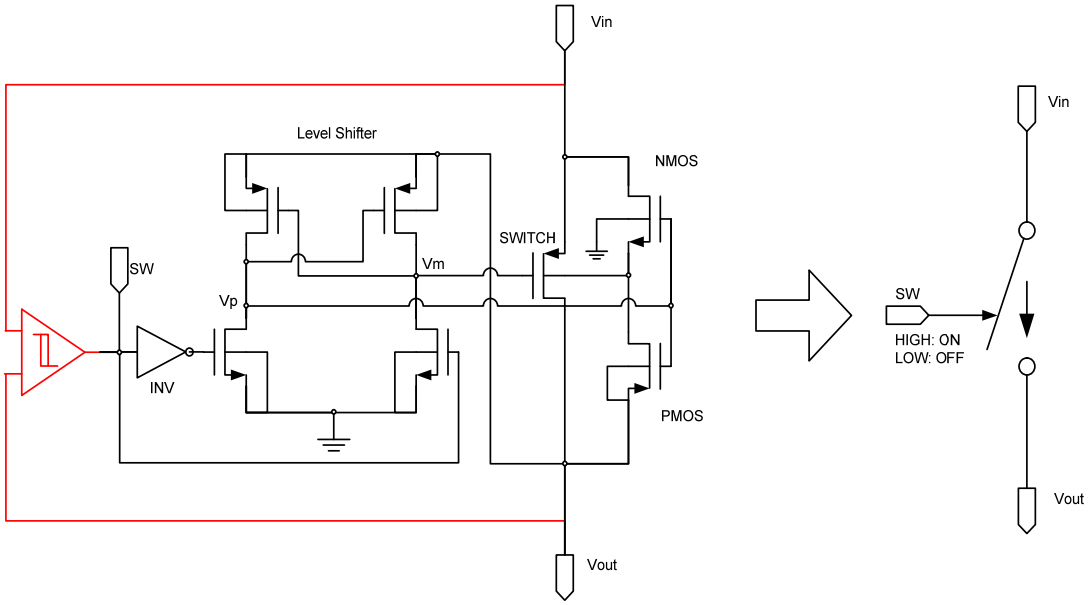

Figure 6 One Way Current Switch.

7. Future Work:

There are still something unsolved in this design:

1. If the chip is shutdown after Vout already ramp up to 5V, there will be a peak current flowing back from the output capacitor to the battery through the power PMOS and inductor, the shutdown output disconnect will not work in this case. This is because, as mentioned before, to completely turn off the power PMOS, its gate and substrate should be tied to the highest voltage level. However, in shutdown mode, no comparator is operating and thus the chip is not able to know which voltage level, Vbat or Vout, is higher. By default, the gate and substrate of the PMOS is tie to Vbat under shutdown mode preventing leakage current from Vbat to Vout. This problem can be solved by not turning off the comparator, which controls the Power Supply Switch in shutdown mode. But that will increase the quiescent current consumption when the booster is shutdown. Another solution is to delay the shutdown time of that particular comparator until Vout drop below Vbat, and then shut down that comparator. But this method still cannot guarantee the current from flowing from Vout to Vbat after the chip is totally shutdown, and Vout is higher than Vbat.

2. The feedback topology will result in a large ripple voltage in the output voltage. Since the output voltage is divided down by 5 to be compared with the reference voltage, together with the sensitivity limit of the comparator (around 5-10mV) and the delay of the feedback loop, the output ripple will be large.

3. Power consumption during normal operation and shutdown mode is still high comparing with products from our competitors.

8. Simulation Result:

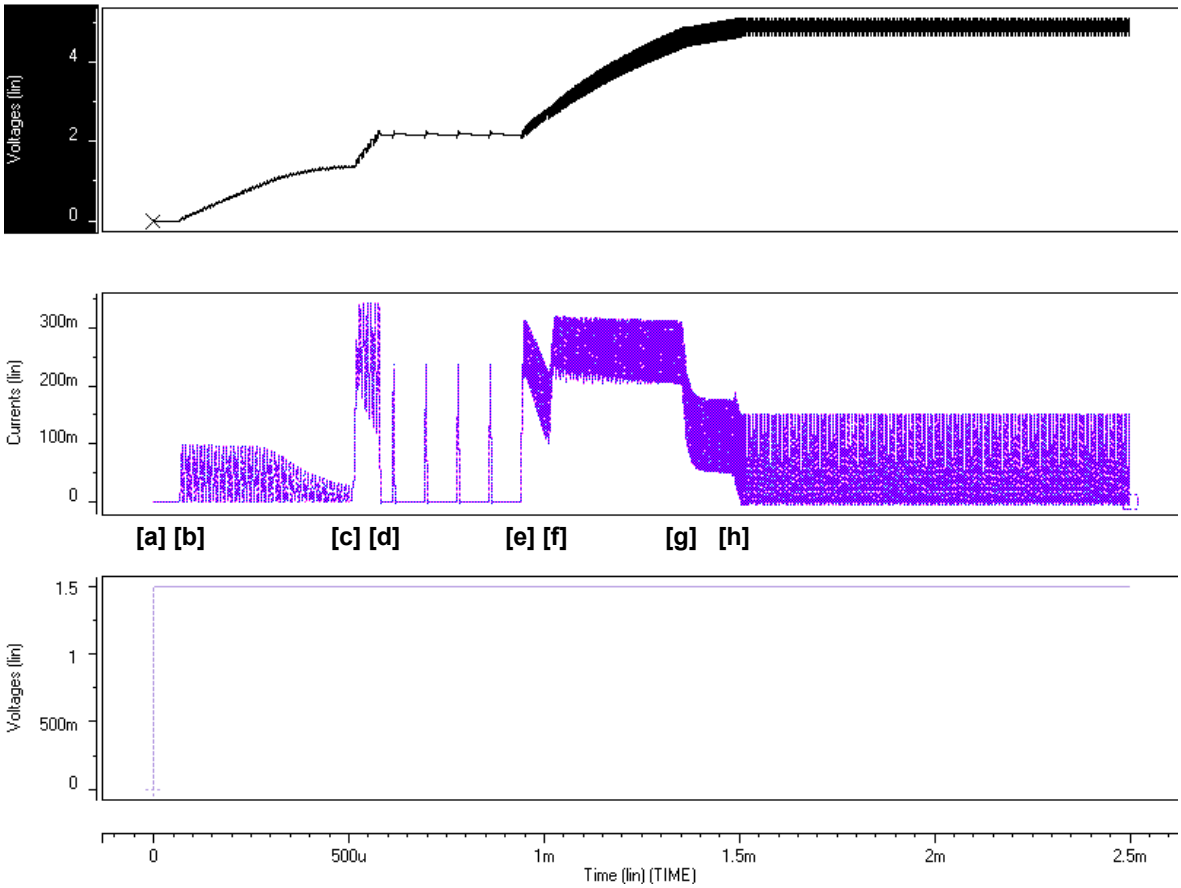

Figure 7 Simulation Result 1, L=22uH, Cout=10uF, Rload=500Ω. Curve 1: Charging profile of Vout; Curve 2: inductor current; Curve 3: Vbat. From curve 2 of inductor current, we can see the startup flow as follow: [a] to [b]: startup and wait for the low voltage block to be ready; [b] to [c]: Vout < Vbat; [c] to [d] Vbat < Vout < 2.3V; [d] to [e] Vout remains on 2.3V, waiting for the non-low voltage block to be ready; [e] to [f]: 2.3V < Vout < 2Vbat; [f] to [g]: 2Vbat < Vout < 4.8V (Vout_H goes high); [g] to [h]: 4.8V < Vout < 5V, real constant Ton emulation begins; After[h]: Vout = 5V, boosting in DCM, real constant Ton emulation.

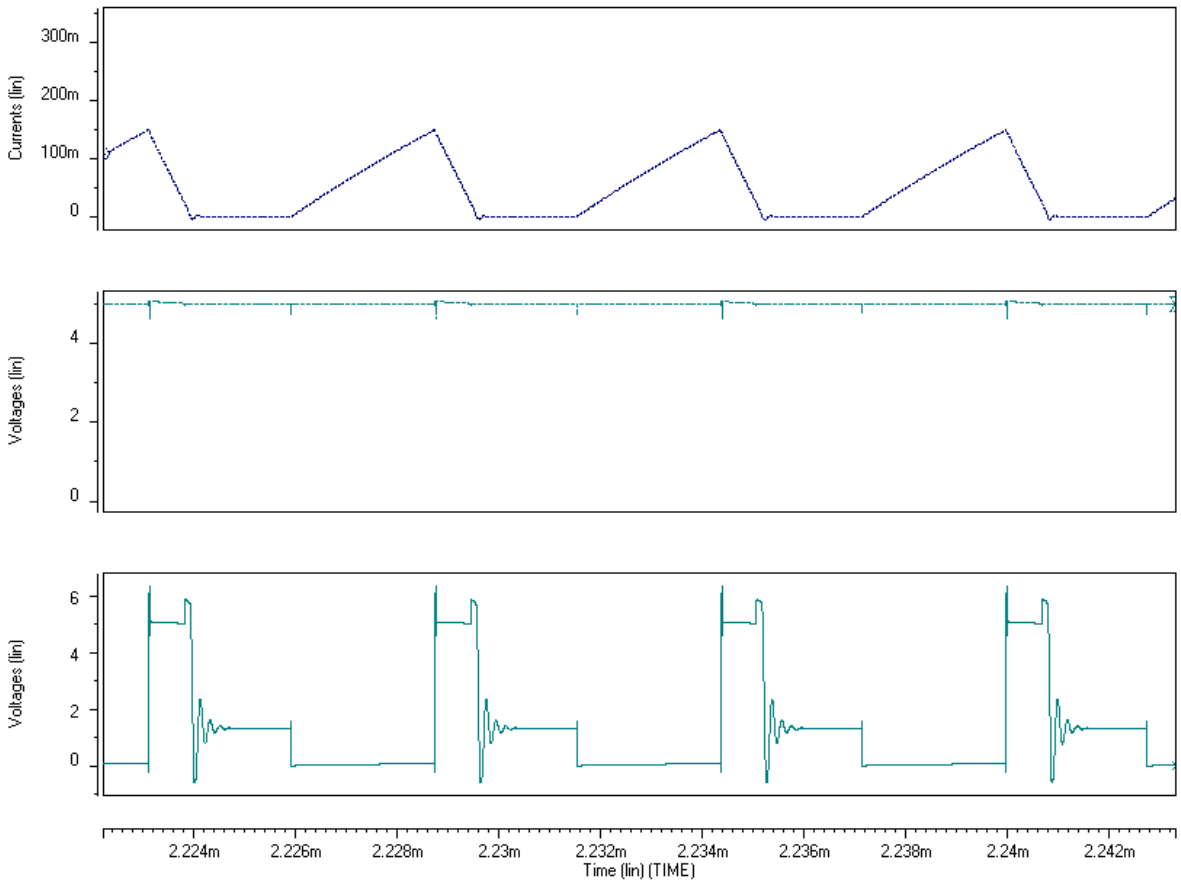

Figure 8 Simulation Result 2, Vbat=1.32V, L=22uH, Cout=10uF, Rload=500Ω. Curve 1: inductor current; Curve 2: Vout (=5V); Curve 3: SW (Anti-Ringing).

9. Reference:

[1] E. Seevinck, "Low-voltage CMOS bias circuit", Electronics Letters, 26th Sep 1996, Vol. 32, No. 20.

[2] Ka Nang Leung, "A Sub-1-V 15-ppm/C CMOS Bandgap Voltage Reference Without Requiring Low Threshold Voltage Device", IEEE Journal of Solid-State Circuits, Vol. 37, No. 4, April 2002.