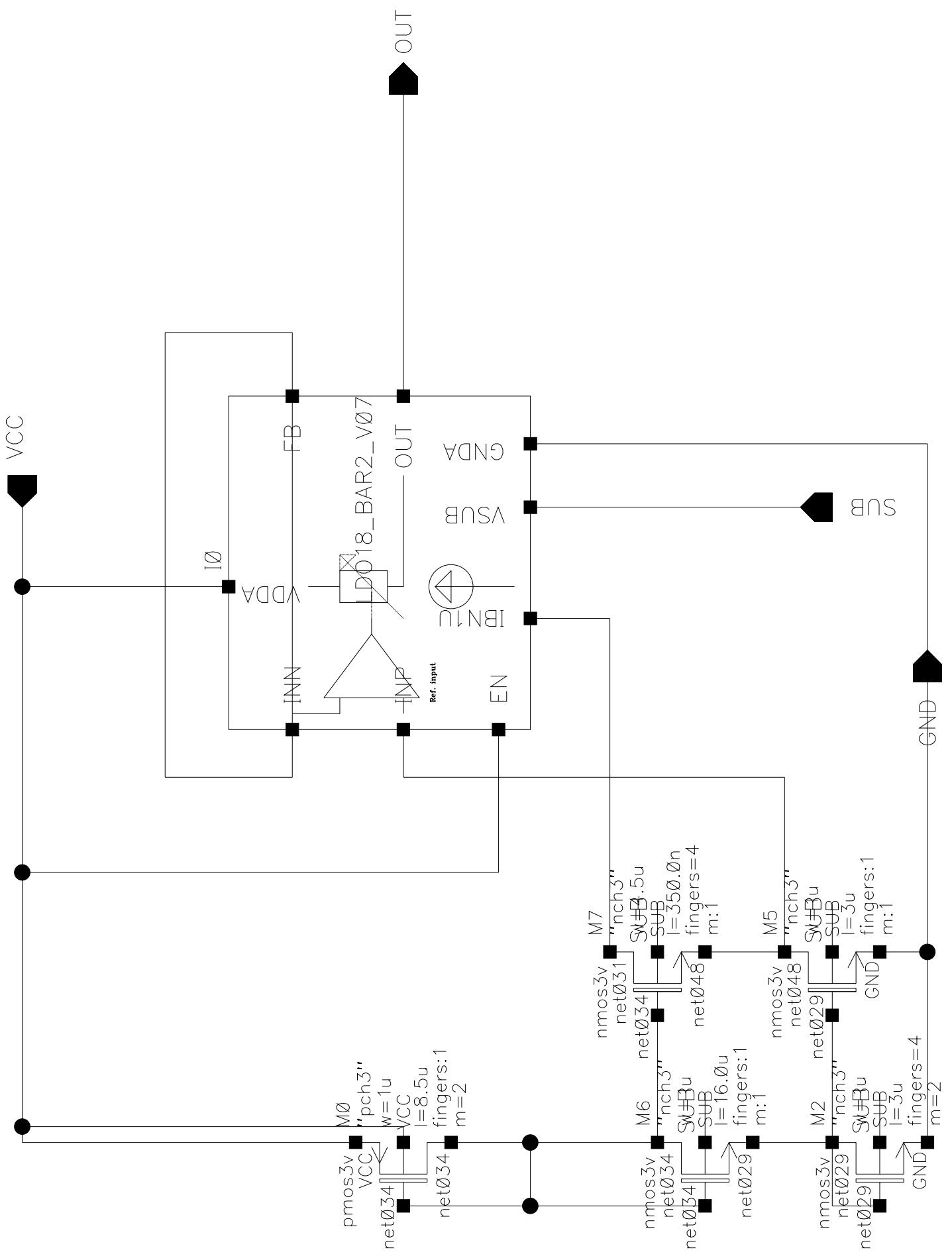


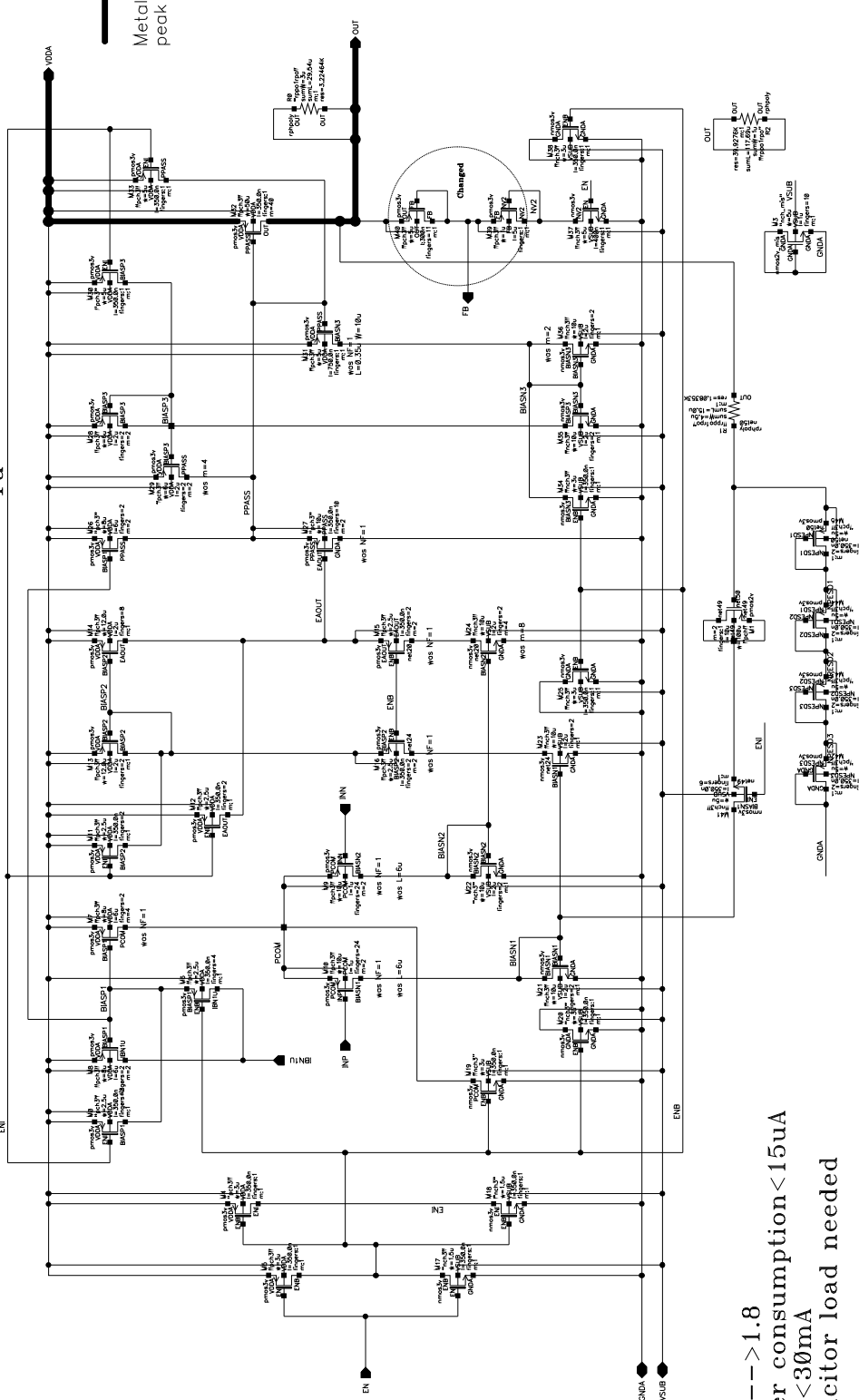
USER: audio_08
DATE: Fri Jul 20 10:04:20 2012
PLOT SIZE: 8.04 x 10.30 Inches
Library: H4_LDO
Cell: DIG_LDO18
View: schematic
Plot Area: (-3.9875 -1.4875) (1.1625 2.5375)



USER: audio_08
DATE: Fri Jul 20 10:04:20 2012
PLOT SIZE: 8.05 x 10.34 Inches
Library: H4_LDO
Cell: LDO18_BAR2_V07
View: schematic
Plot Area: ((0.6875 -11.625) (22.6875 5.5))

REVISIONS		DATE	APPROVED
ZONE	REV	DESCRIPTION	

1u 1u 1u 1u 4u 1u 2u 1u



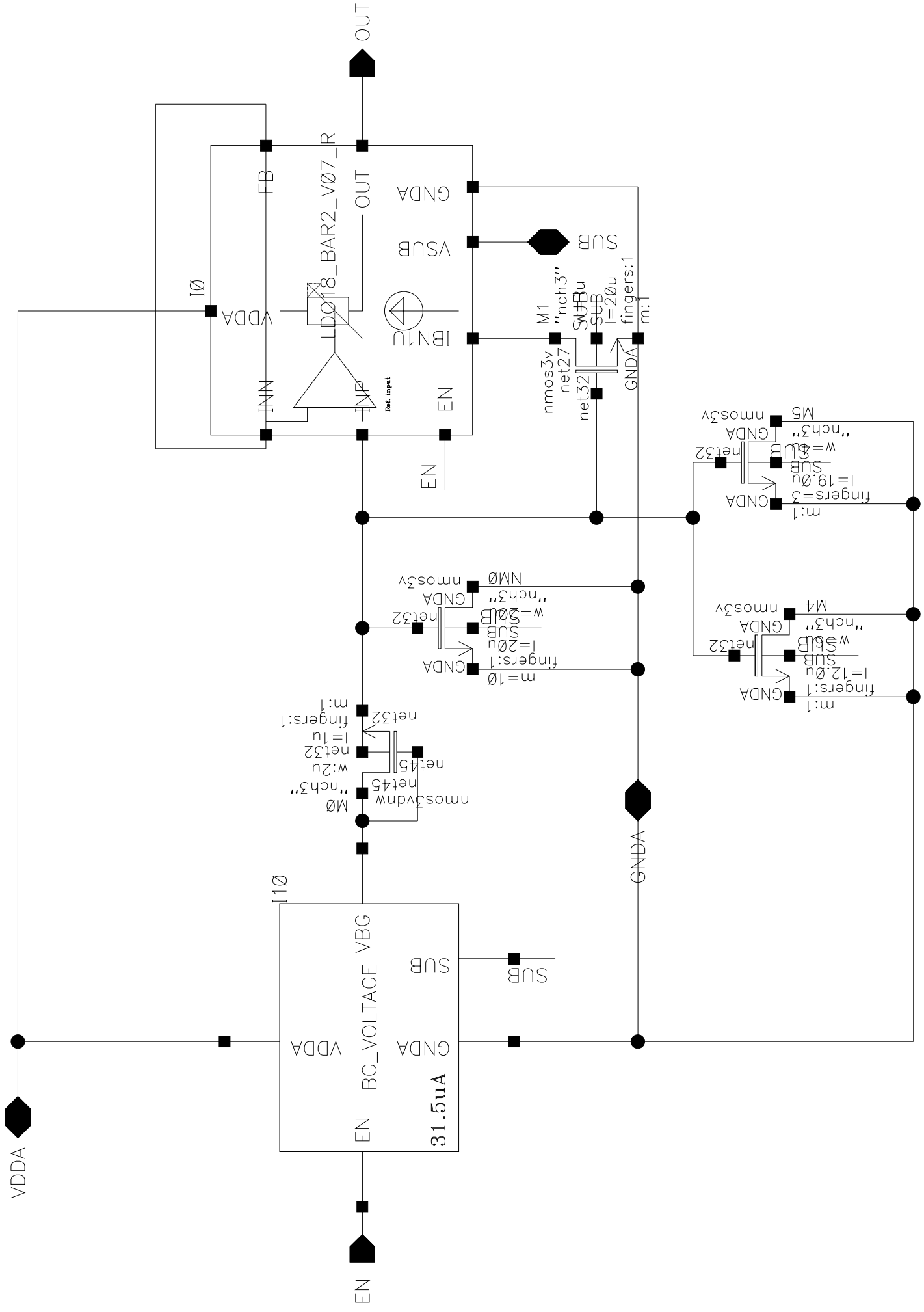
3.3--->1.8
 power consumption<15uA
 Load<30mA
 Capacitor load needed

Modified the transistor size and power consumption
 by Dennis on Sep. 3, 2008

- Layout Notes:
1. Common centroid: MP1A&MP1B,
 2. Match transistor pairs:
 a) MN1B&MN2B;MN1A&MN2A;MN3A&MN3B,
 b) MP2A&MP2B;MP3A&MP3B;MPB0&MPB1&MPB2;MPA0a&MPA0b,
 3. Capacitor MNCAP1 is not necessary to be rectangle, its shapes can be adjusted by the layout space,
 4. Resistor:
 a) XRFB1&XRFB2 need match very well, use W=1.5u L=30u unit resistor and interleave layout,
 b) XRFBDUM is the dummy resistor for metal option of XRFB1 or XRFB2, use L=30u W=1.5u unit resistor,
 c) Dummy resistor need be around the matching resistor array,
 5. Avid metal2 over matched analog devices.

UPDATED	Oct 1 16:29:30 2008	LDO18_BAR2_V07
DRAWN	Harbin Yang	
CHECKED		
ISSUED		
SIZE	C	SCALE
PAGE NO.		SHEET
DWG NO.		OF

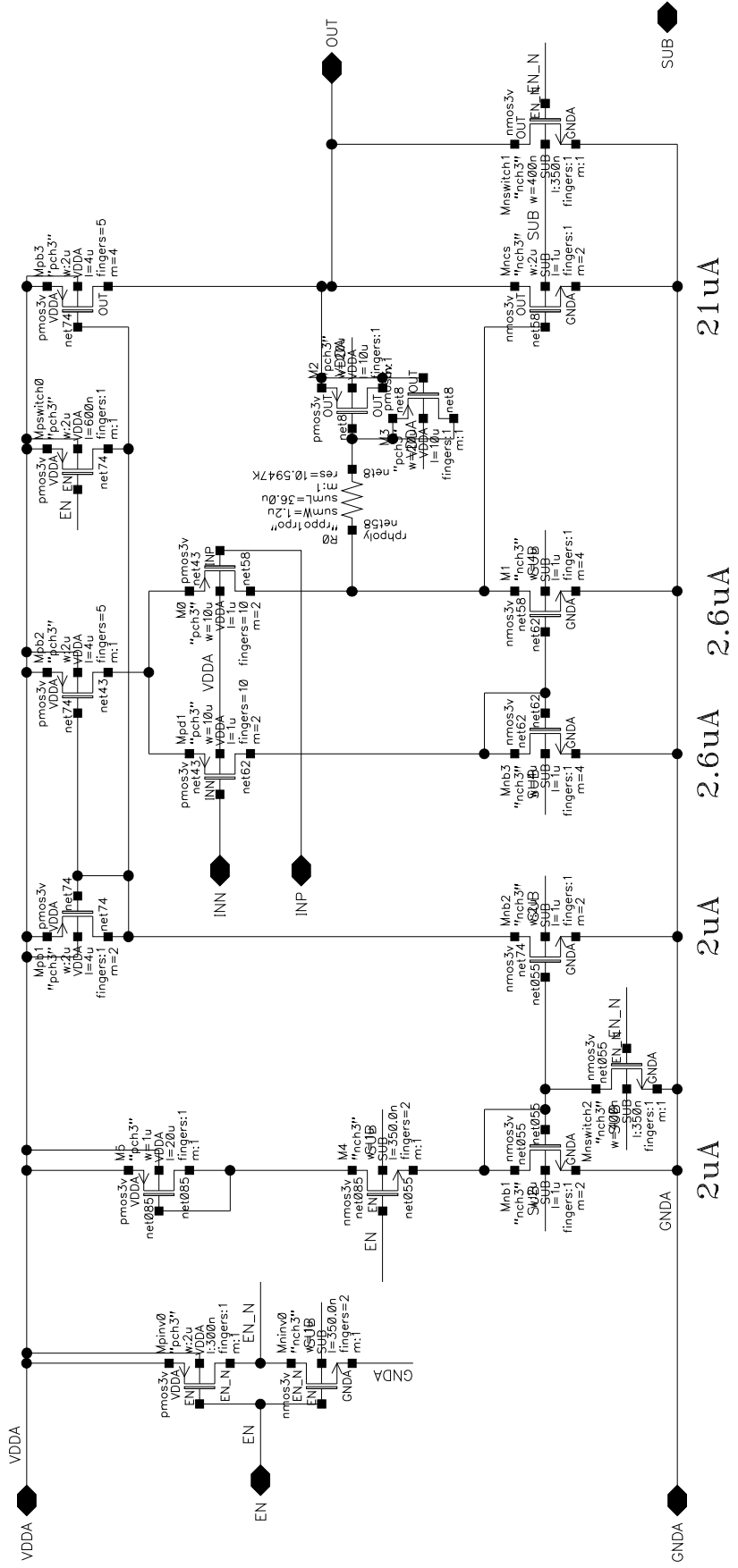
USER: audio_08
DATE: Fri Jul 20 10:03:22 2012
PLOT SIZE: 7.35 x 10.51 inches
Library: H4_LDO
Cell: ANA_LDO18
View: schematic
Plot Area: (-4.225 -2.28125) (1.725 1.875))



USER: audio_08
DATE: Fri Jul 20 10:03:22 2012
PLOT SIZE: 8.05 x 10.42 Inches
Library: H4_LDO
Cell: BG_OPAMP
View: schematic
Plot Area: ((0.00,0)(11.08,5))

REVISIONS

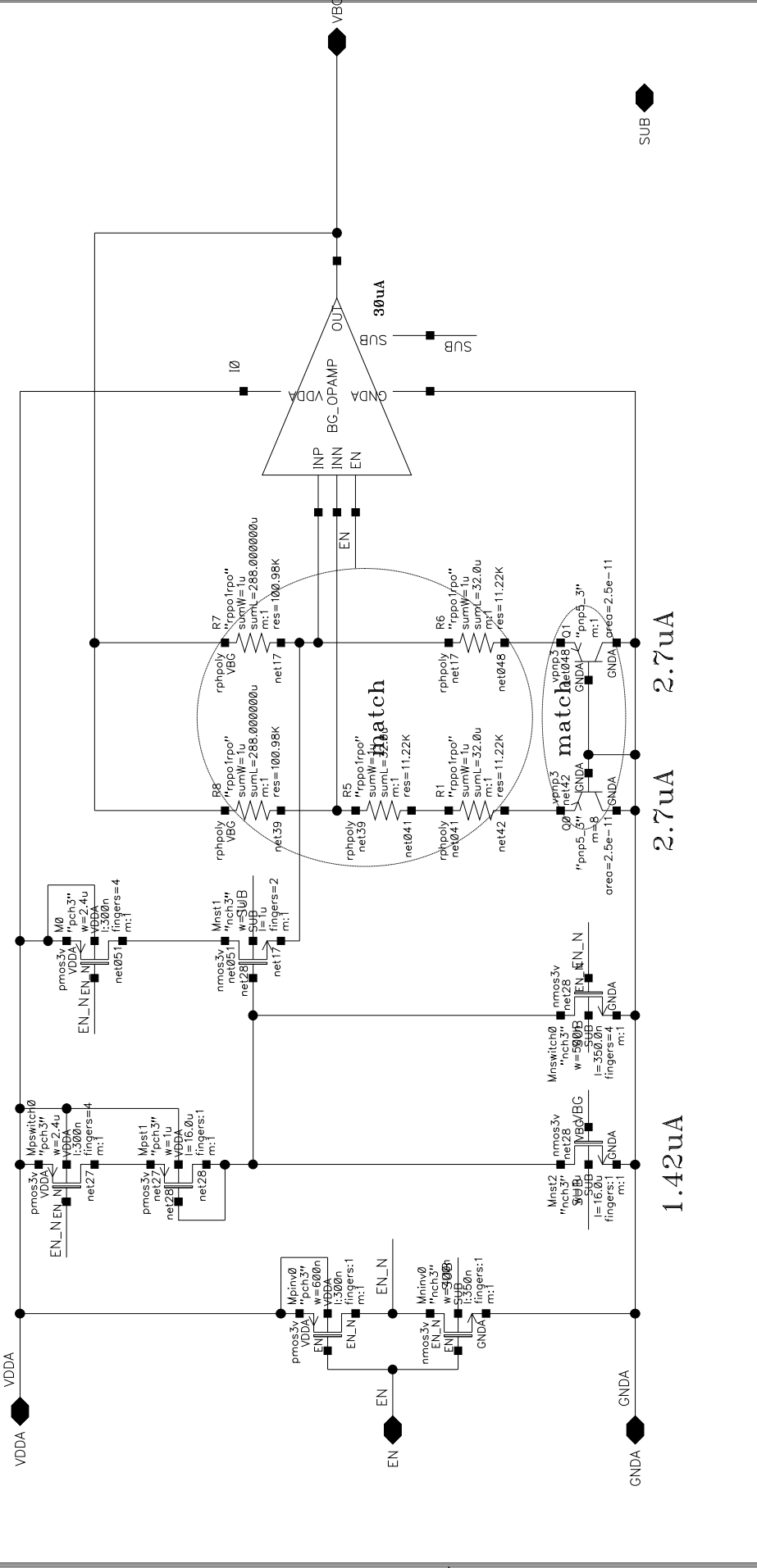
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	Oct 4 12:00:11 2008				
DRAWN					
CHECKED					
CHECKED					
ISSUED					

USER: audio_08
DATE: Fri Jul 20 10:03:22 2012
PLOT SIZE: 8.05 x 10.42 Inches
Library: H4_LDO
Cell: BG_VOLTAGE
View: schematic
Plot Area: ((0.00,0.0)(11.08,5))

CAGE NO.	DWG NO.	SH	REV
		1	
REVISIONS		DATE	APPROVED
ZONE	REV		



UPDATED	Oct 4 12:00:11 2008	02Micro	
DRAWN			
CHECKED			
CHECKED		SIZE	CAGE NO.
ISSUED		A	
		DWG NO.	REV
		SCALE	1 OF 1
		SHEET	1 OF 1

USER: audio_08

DATE: Fri Jul 20 10:03:22 2012

PLOT SIZE: 8.05 x 10.34 Inches

Library: H4_LDO

Cell: LDO18_BAR2_V07_R

View: schematic

Plot Area: (0.6875 -11.625) (22.6875 5.5)

4

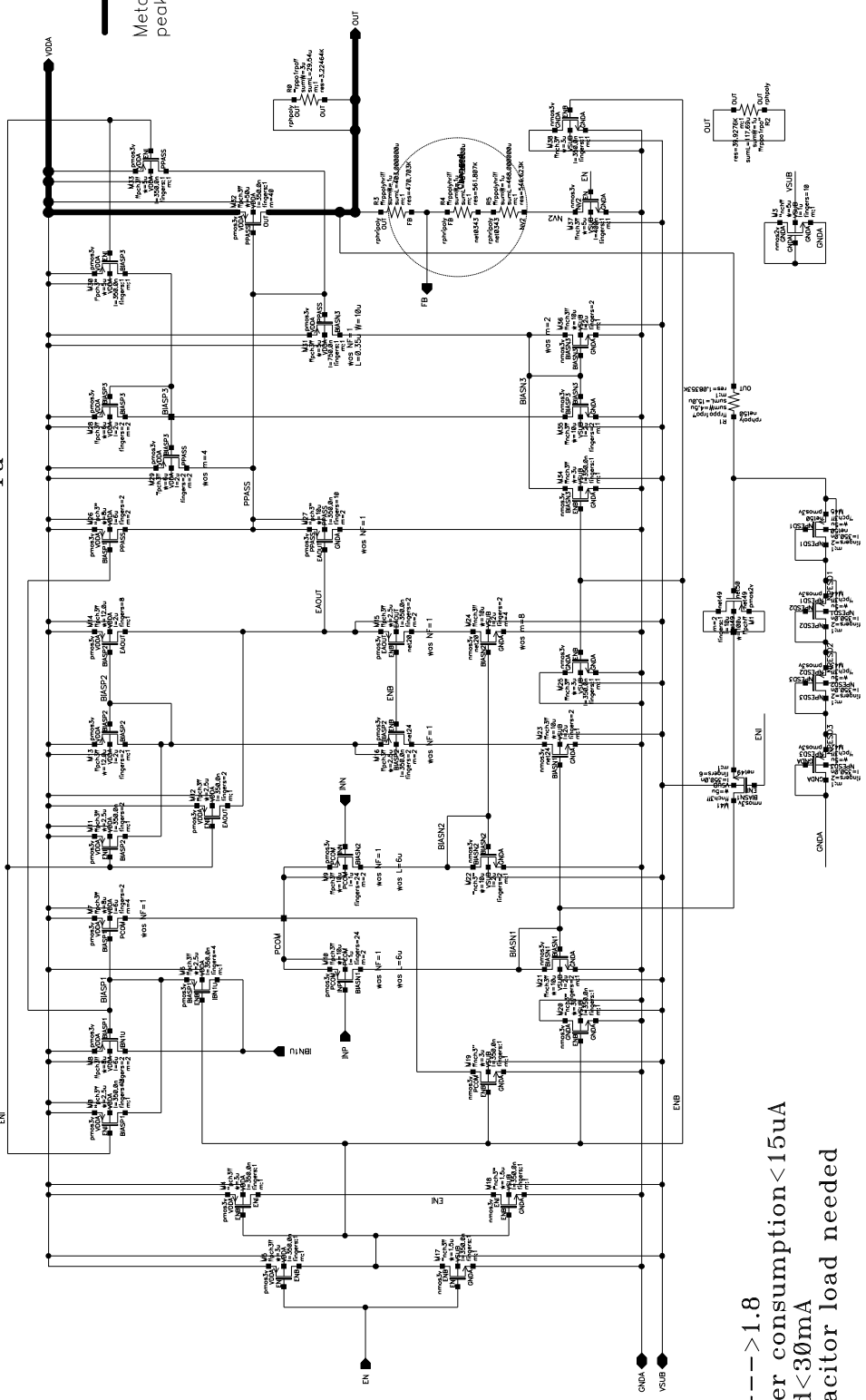
3

2

1

REVISIONS		DATE	APPROVED
ZONE	REV	DESCRIPTION	

1u 2u 1u 4u 1u 1u 1u 1u



3.3--->1.8
 power consumption<15uA
 Load<30mA
 Capacitor load needed

Modified the transistor size and power consumption
 by Dennis on Sep. 3, 2008

- Layout Notes:
1. Common centroid: MP1A&MP1B,
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 a) MN1B&MN2B;MN1A&MN2A;MN3A&MN3B,
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 c) Dummy resistor need be around the matching resistor array,
 5. Aviod metal2 over matched analog devices.

UPDATED	Oct 4 12:00:11 2008	LDO18_BAR2_V07
DRAWN	Haibin Yang	
CHECKED		
ISSUED		
SIZE	C	SCALE
PAGE NO.		SHEET
DWG NO.		OF

4

3

2

1