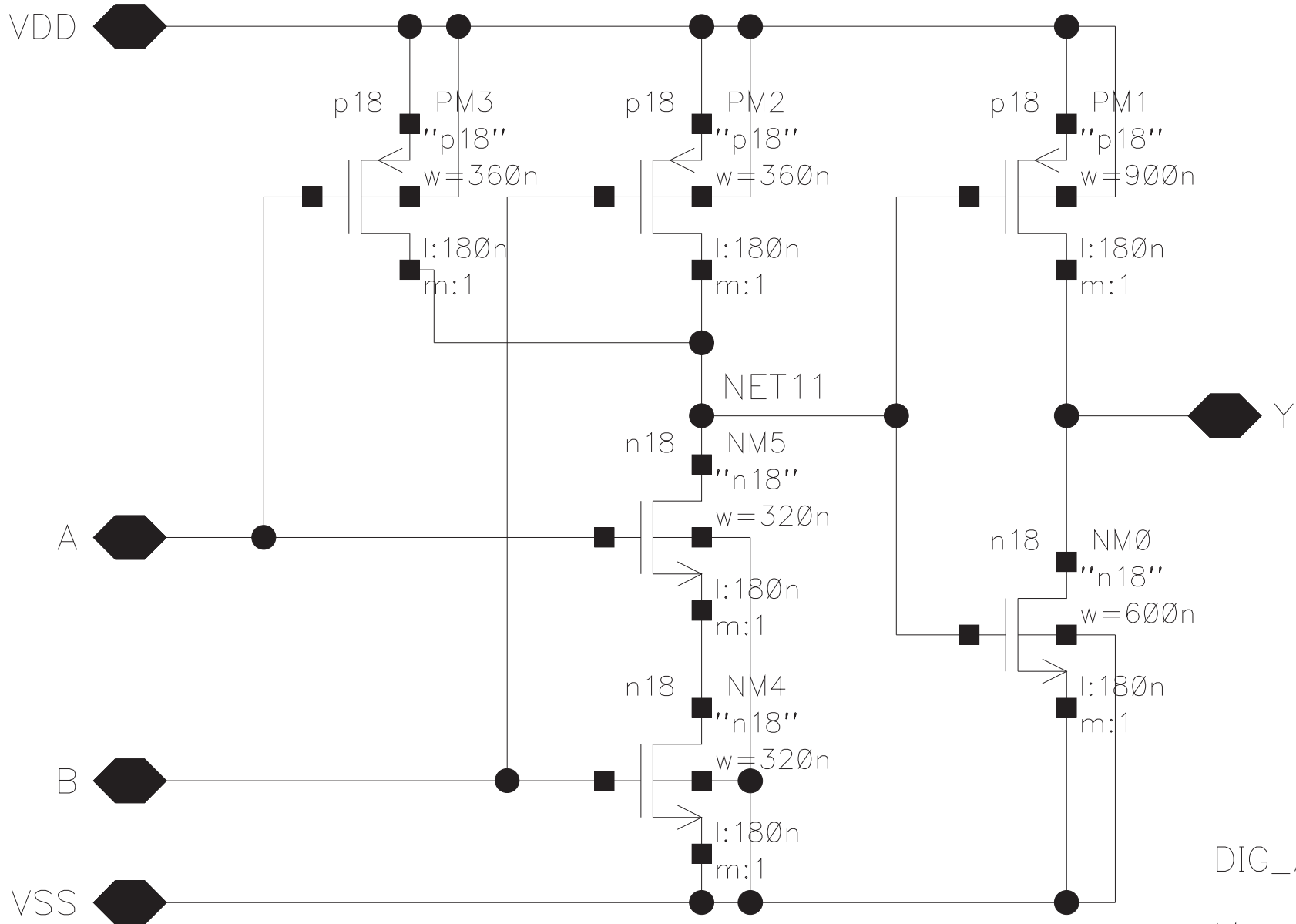


DIG\_ADDHX1

May 17 2007

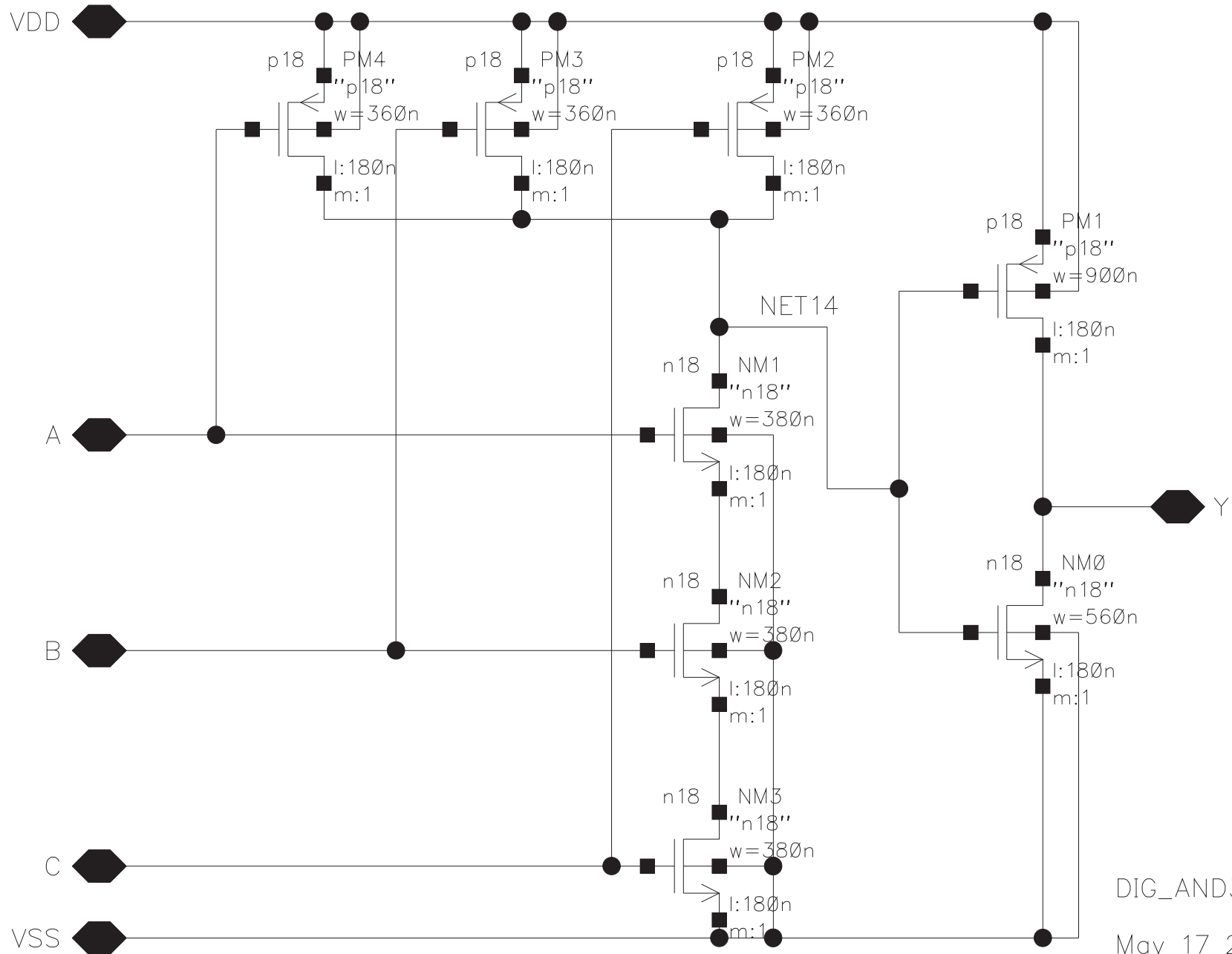
Haibin Yang



DIG\_AND2X1

May 17 2007

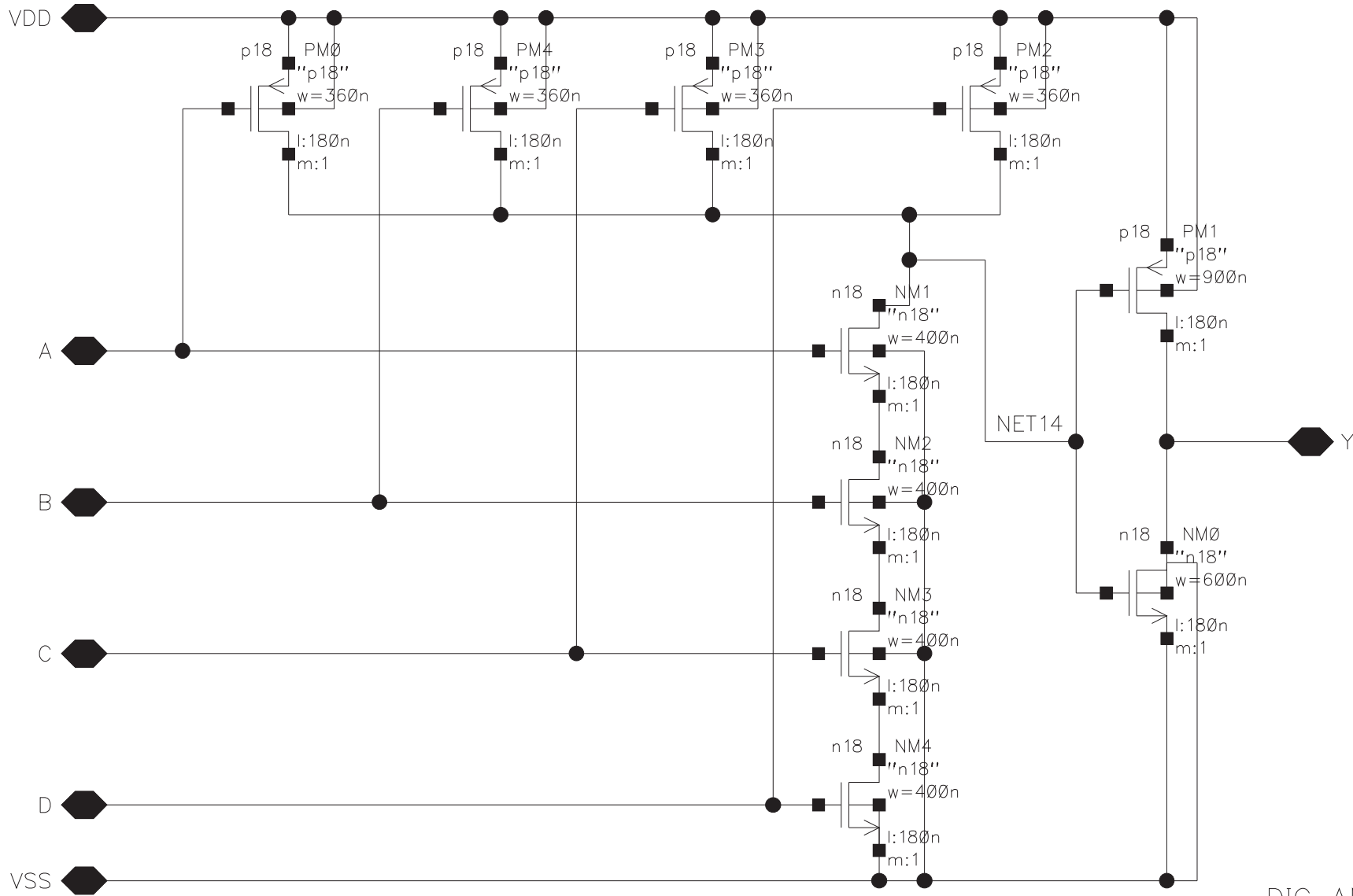
Haibin Yang



DIG\_AND3X1

May 17 2007

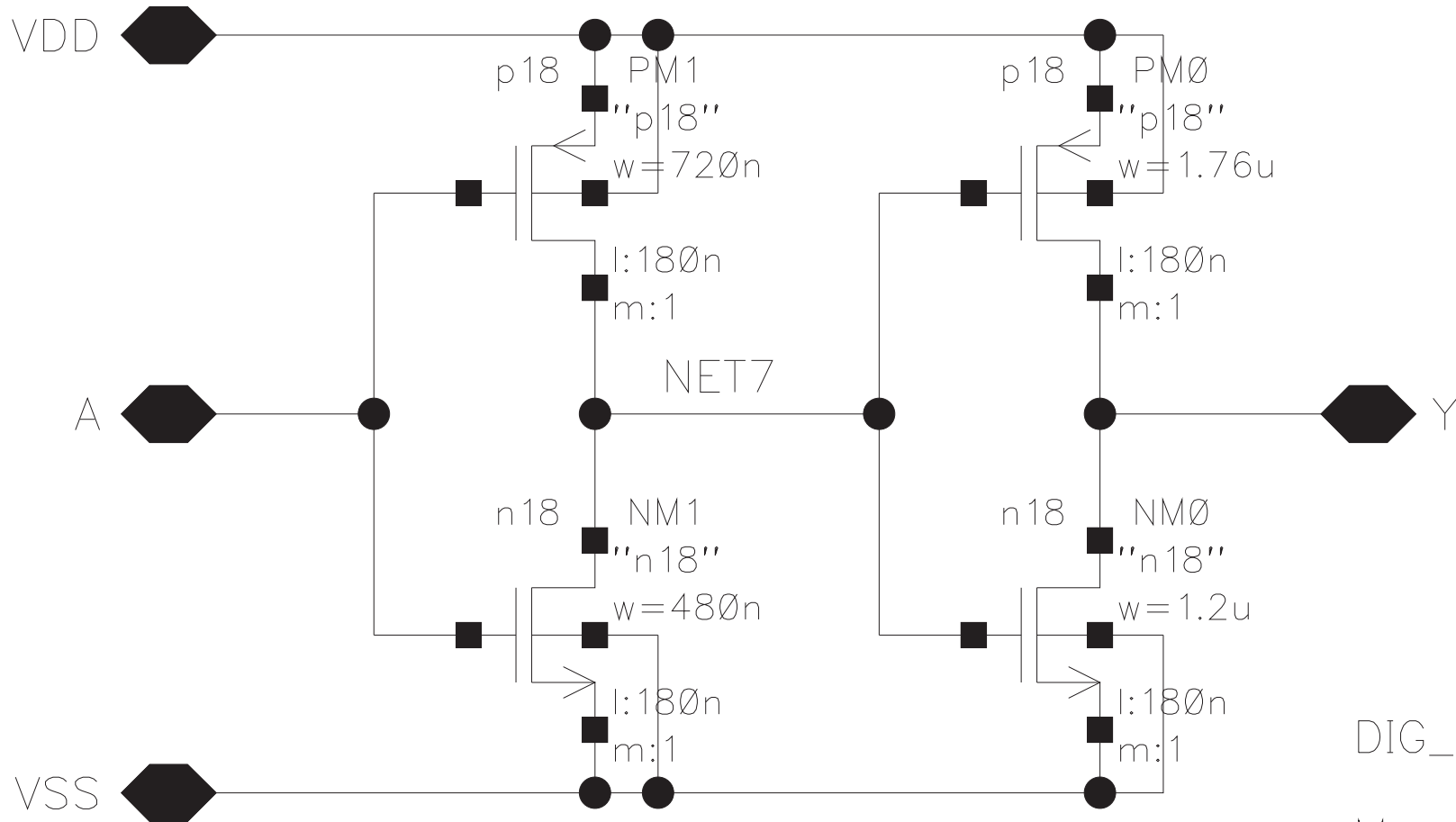
Haibin Yang



DIG\_AND4X1

May 17 2007

Haibin Yang

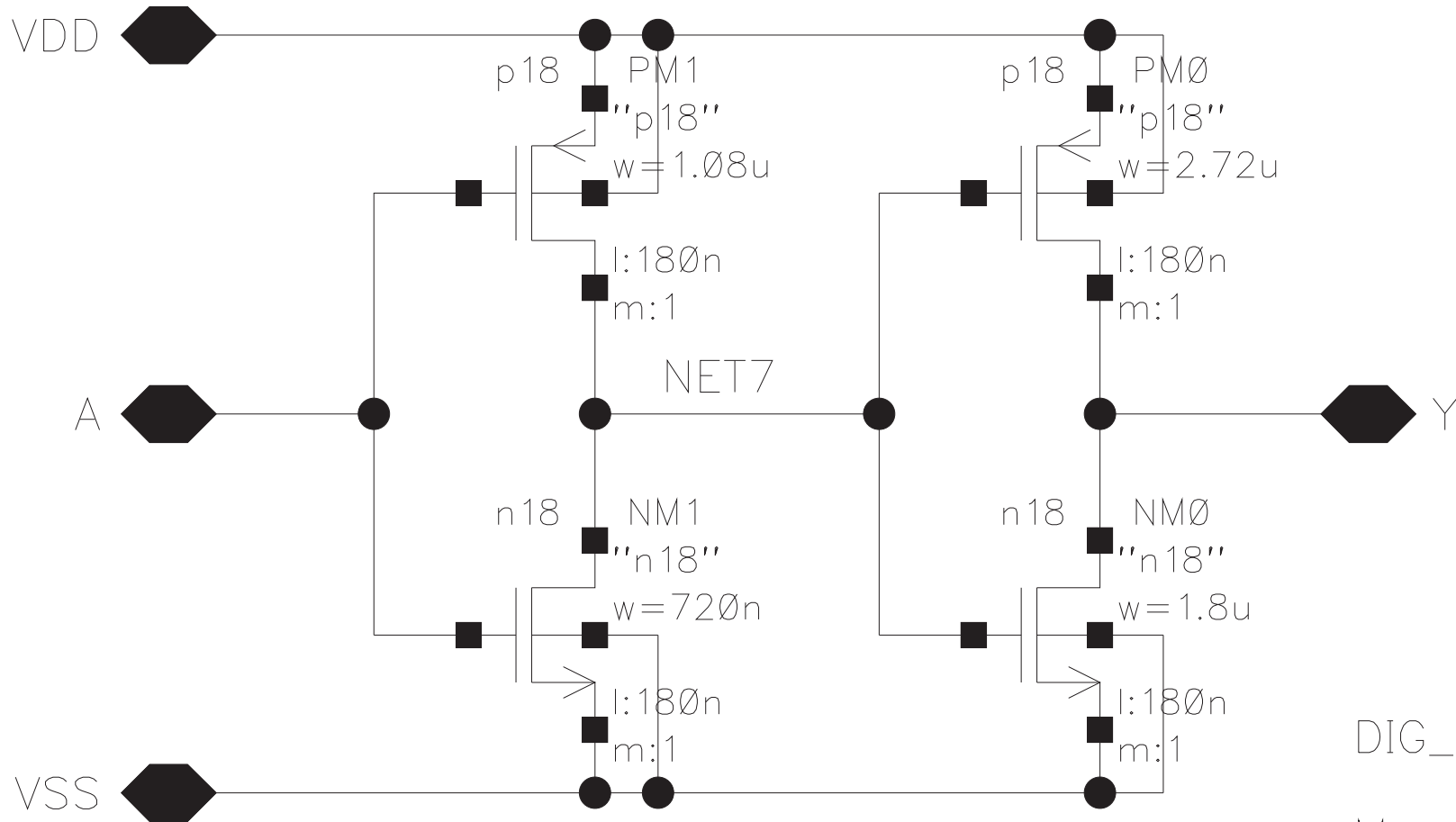


DIG\_BUF2

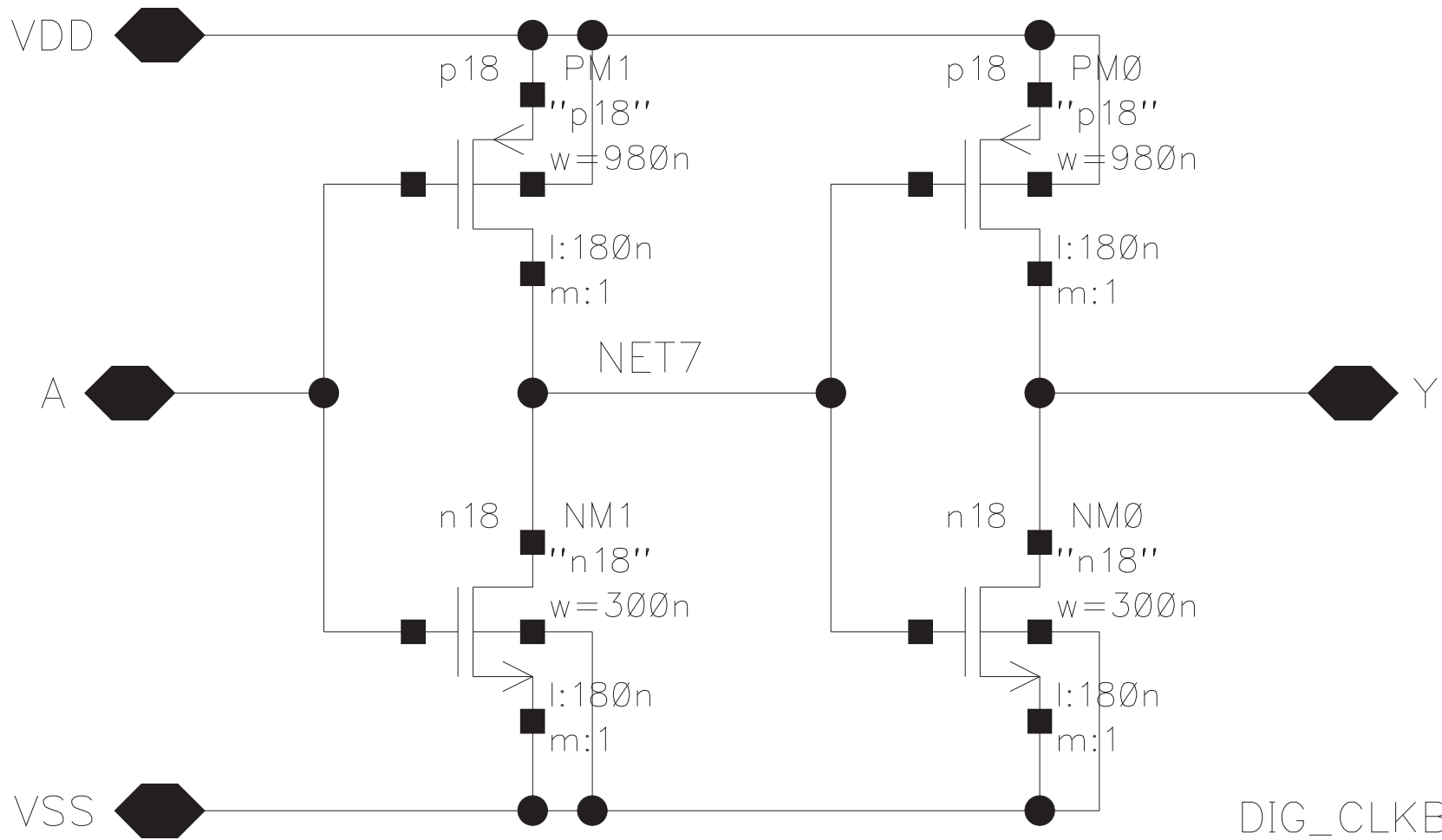
May 17 2007

Haibin Yang





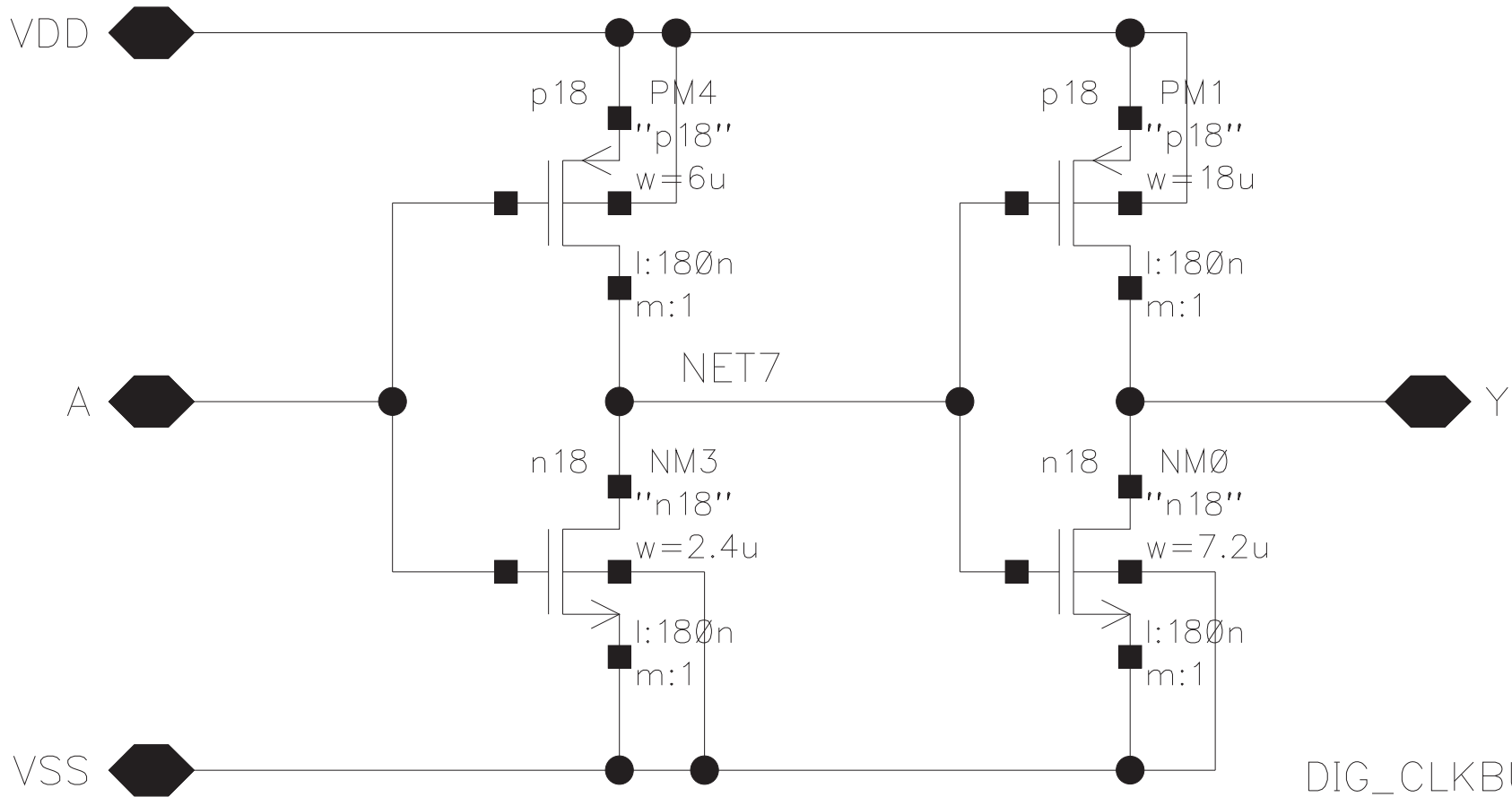
DIG\_BUF3  
May 17 2007  
Haibin Yang



DIG\_CLKBUF\_X1

May 17 2007

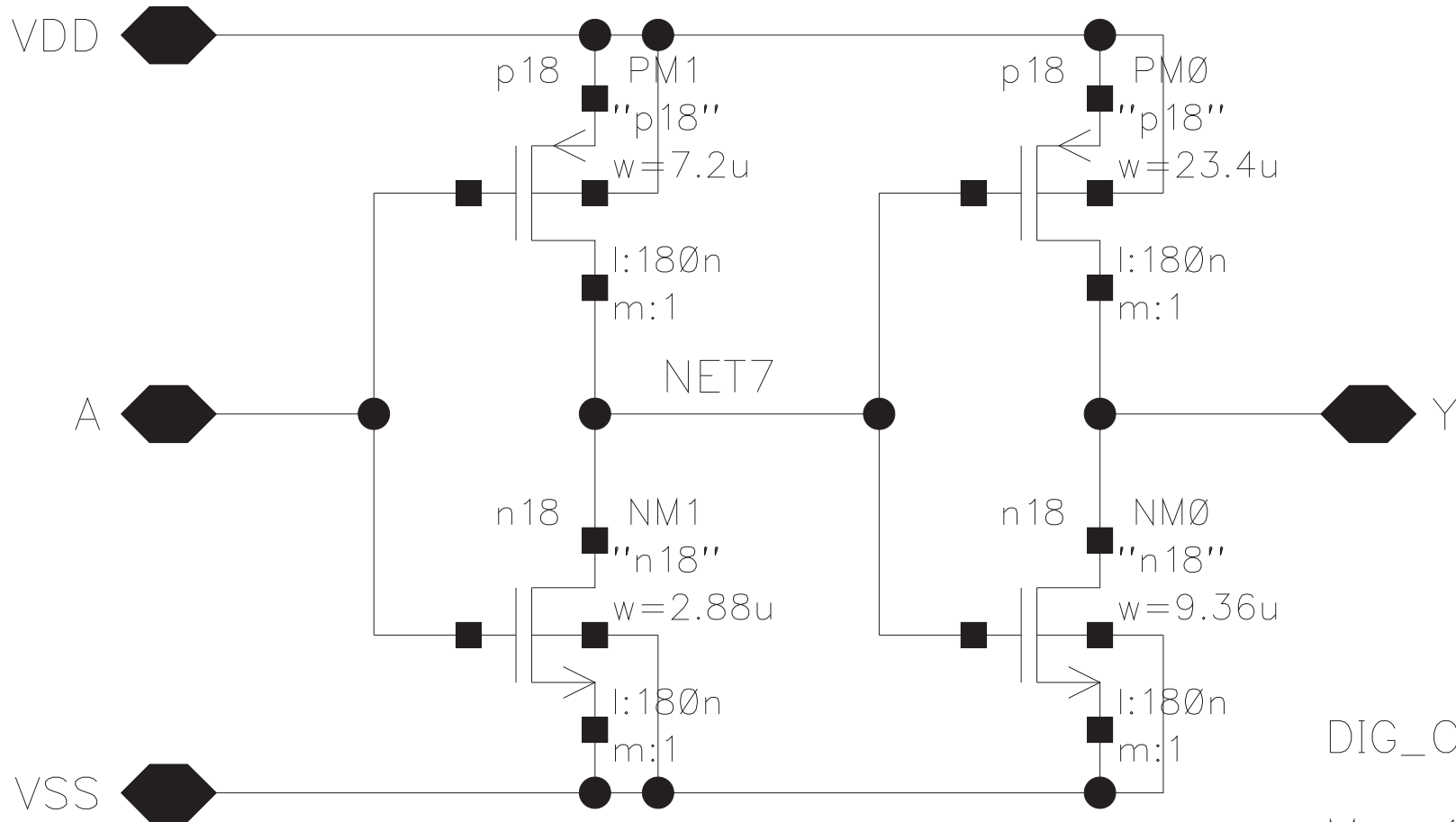
Haibin Yang



DIG\_CLKBUF12

May 17 2007

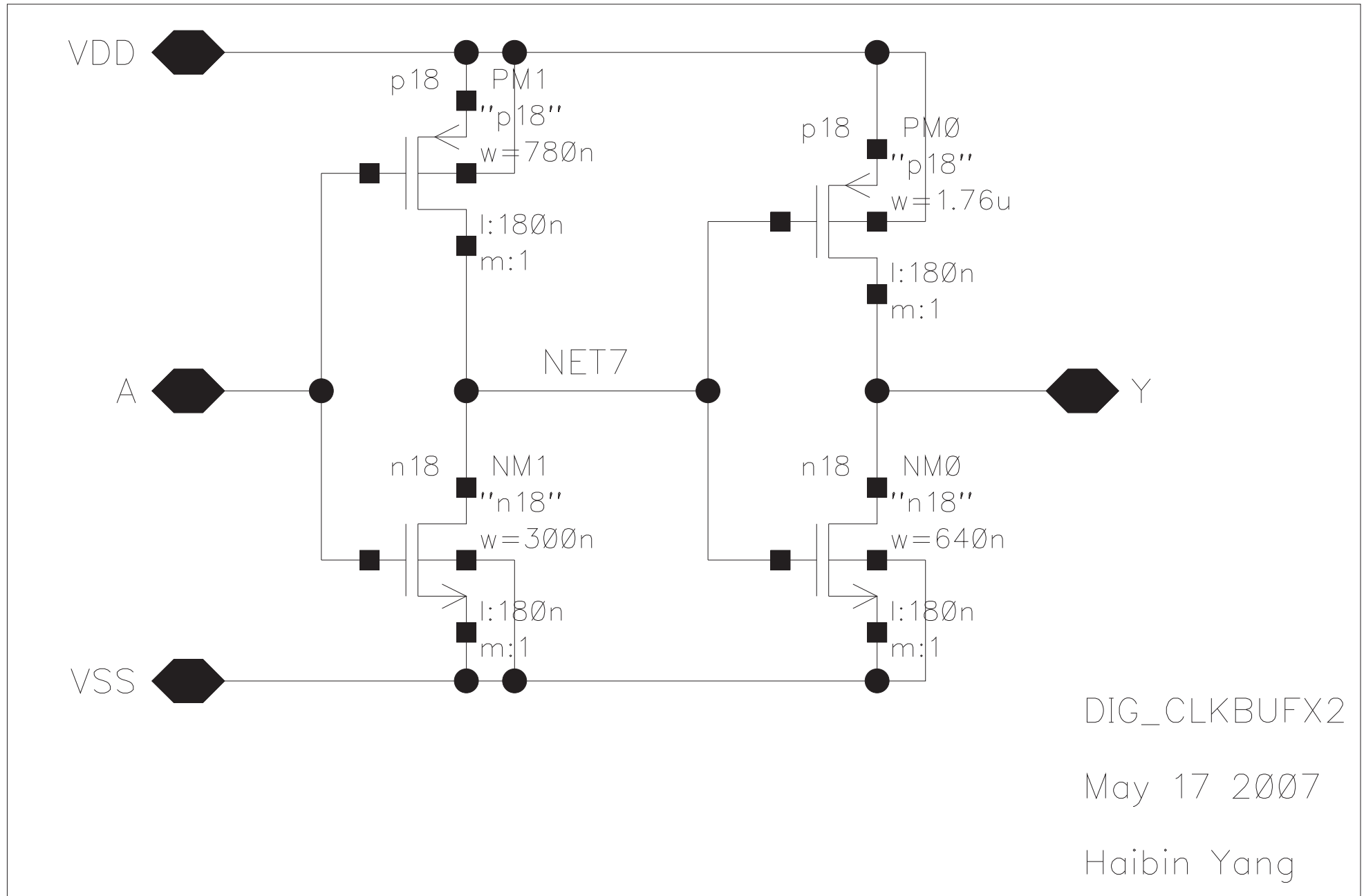
Haibin Yang



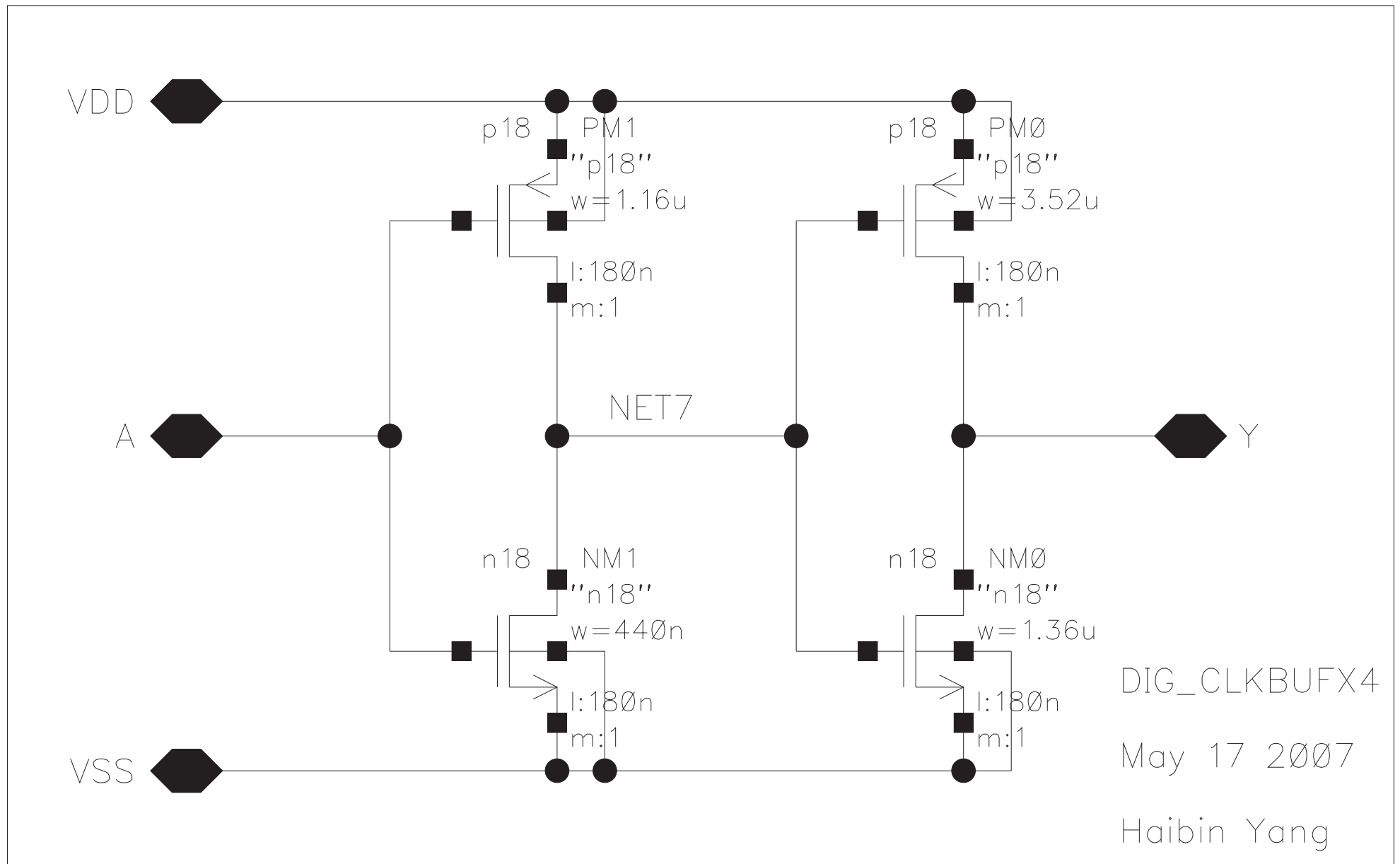
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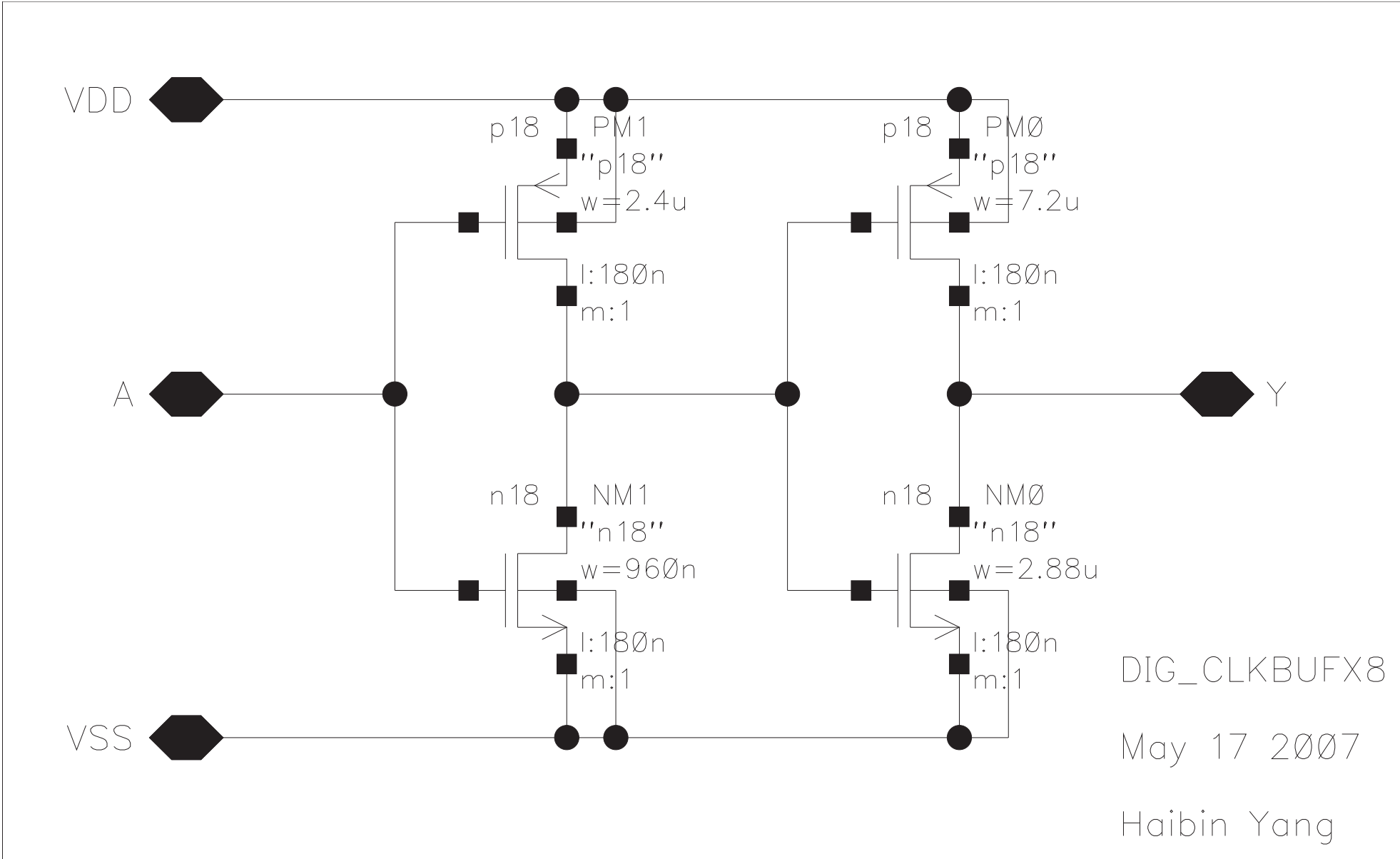
May 17 2007

Haibin Yang







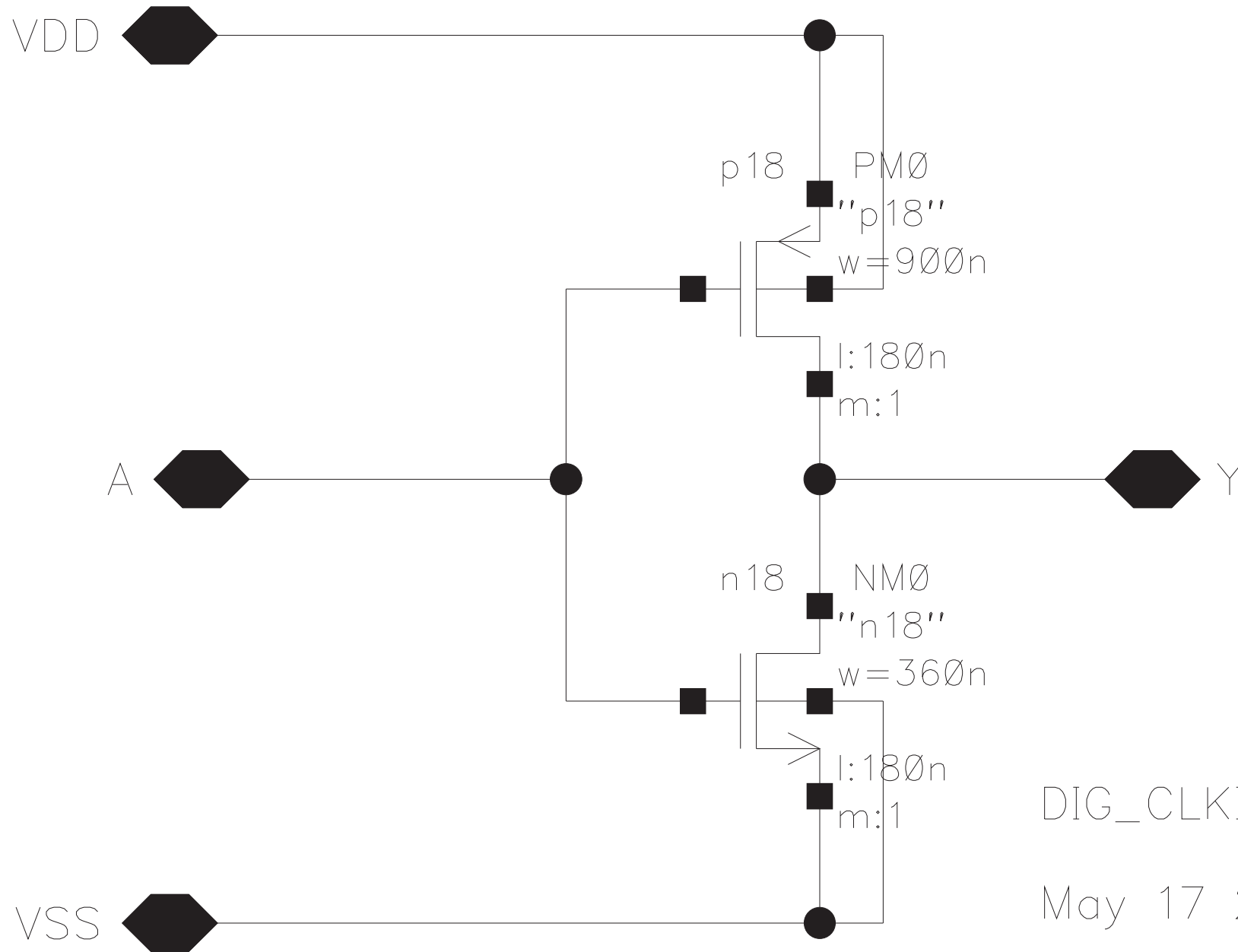


DIG\_CLKBUF8

May 17 2007

Haibin Yang

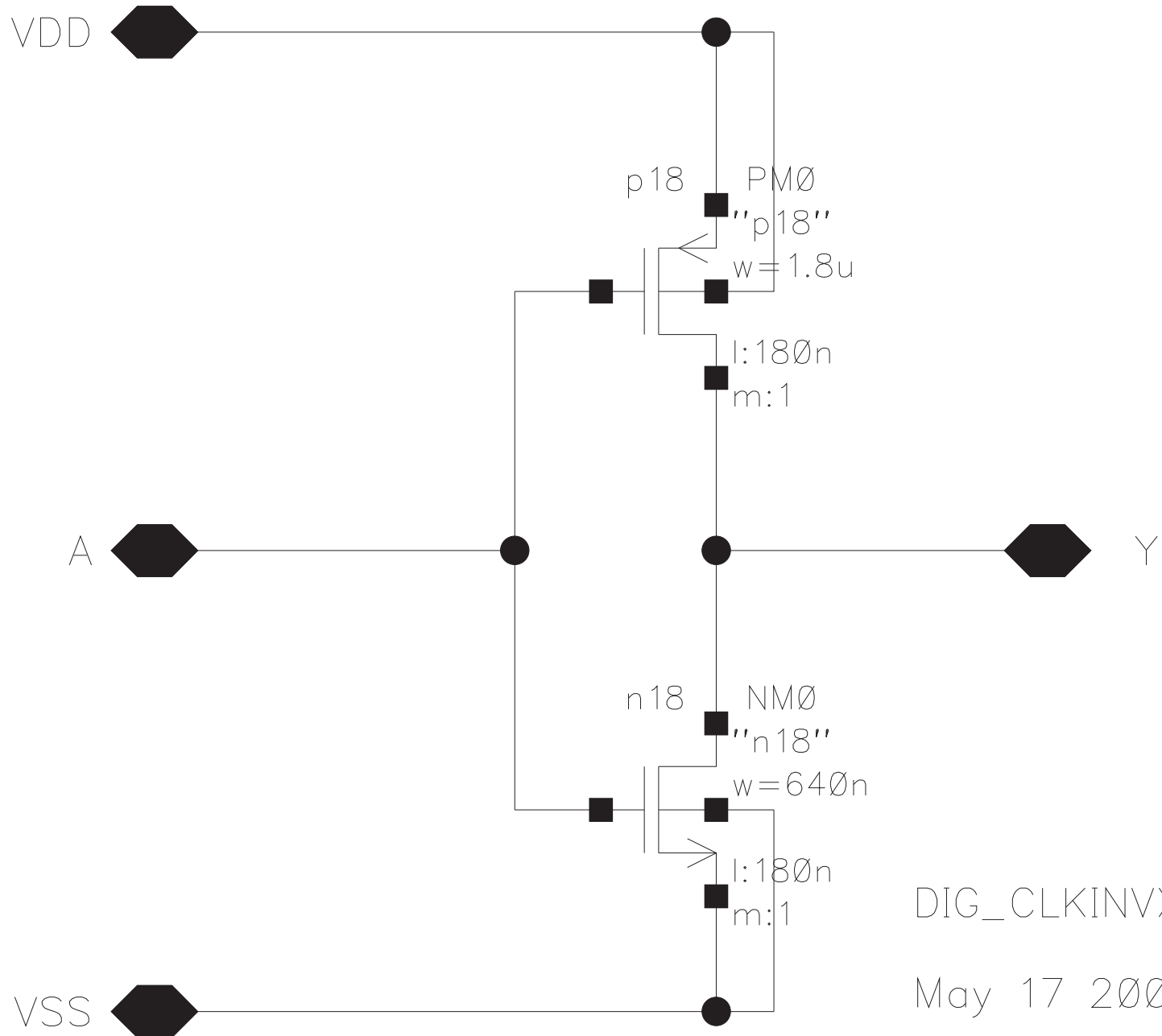




DIG\_CLKINVX1

May 17 2007

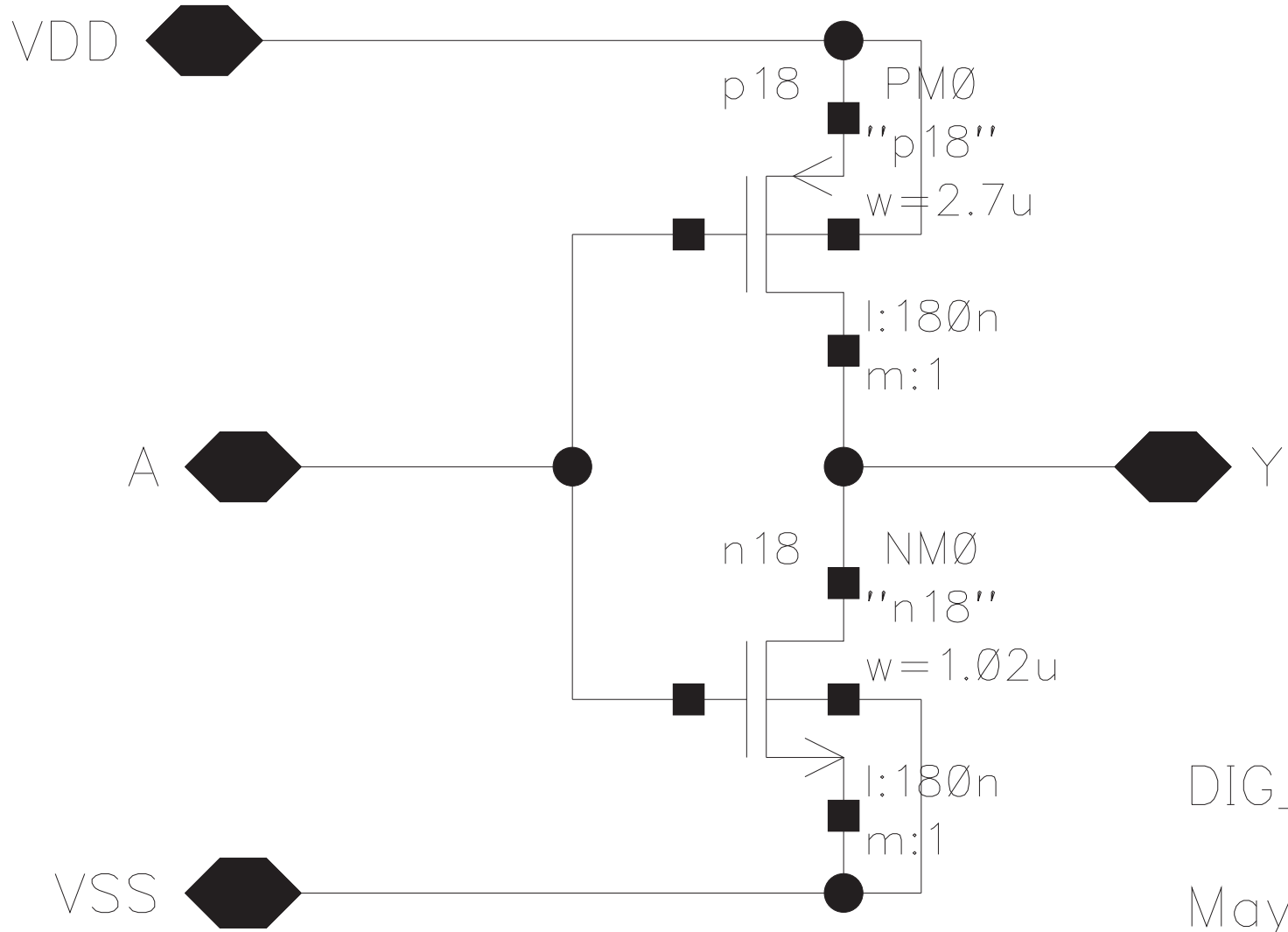
Haibin Yang



DIG\_CLKINVX2

May 17 2007

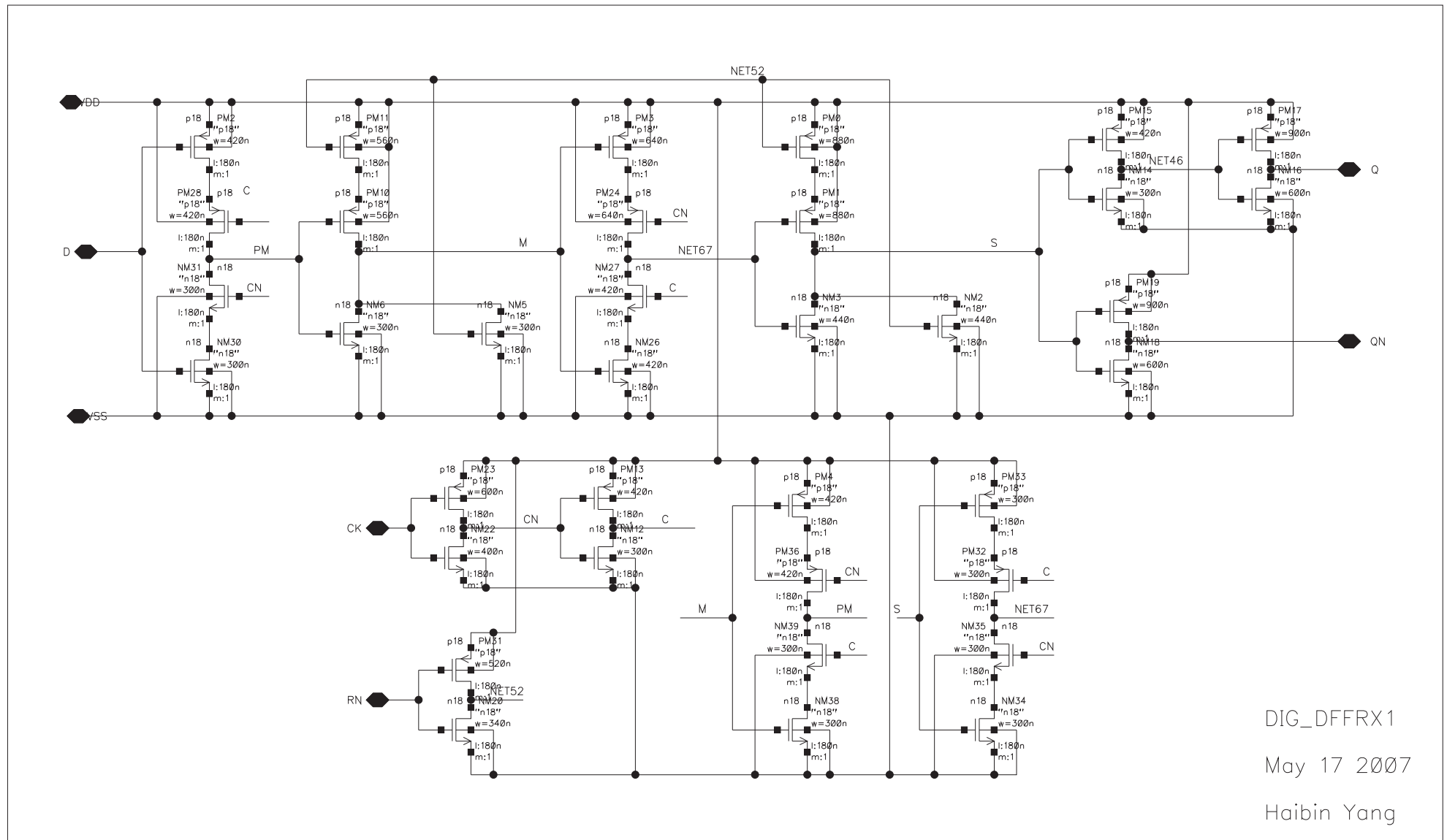
Haibin Yang



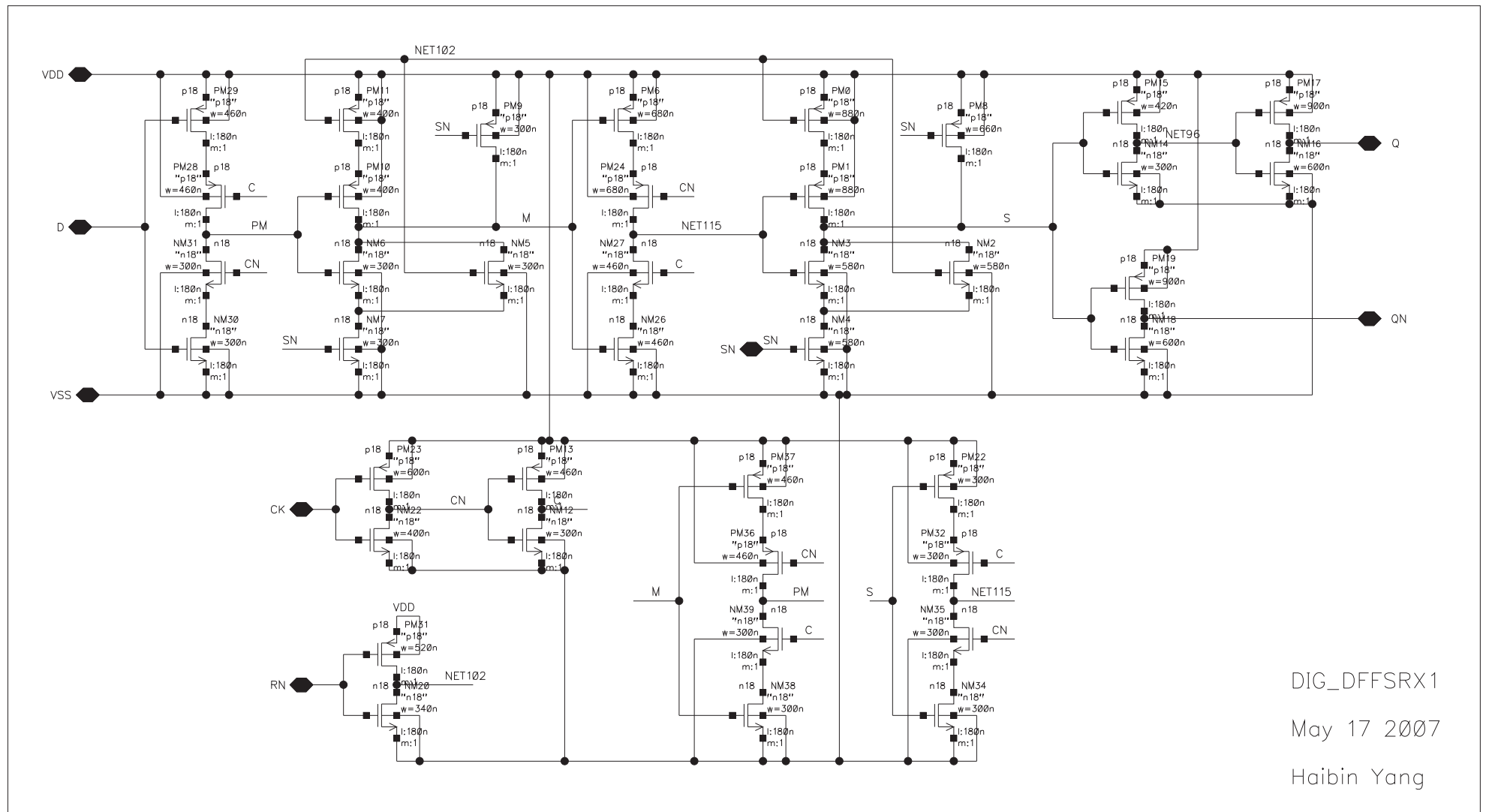
DIG\_CLKINVX3

May 17 2007

Haibin Yang



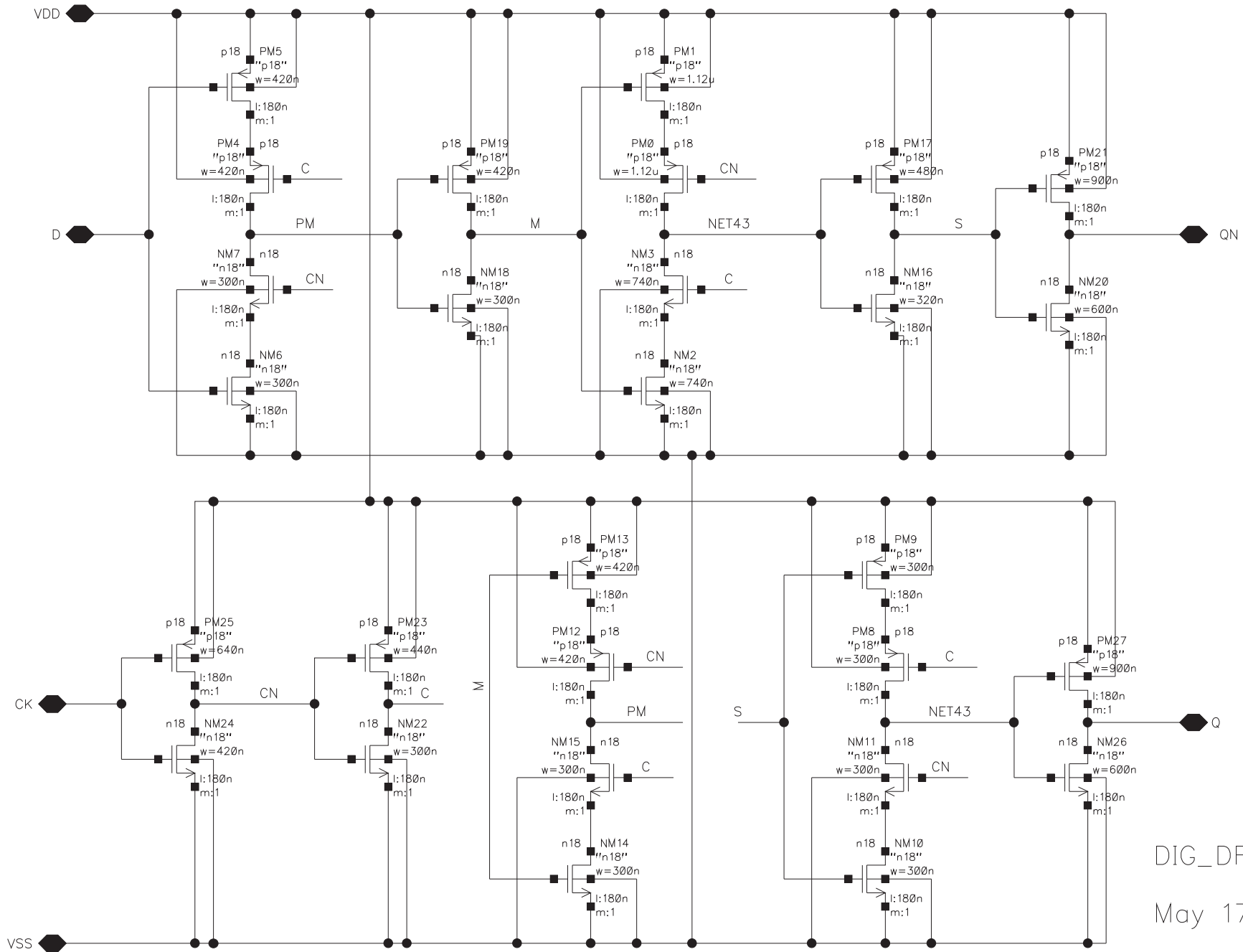
DIG\_DFFRX1  
 May 17 2007  
 Haibin Yang



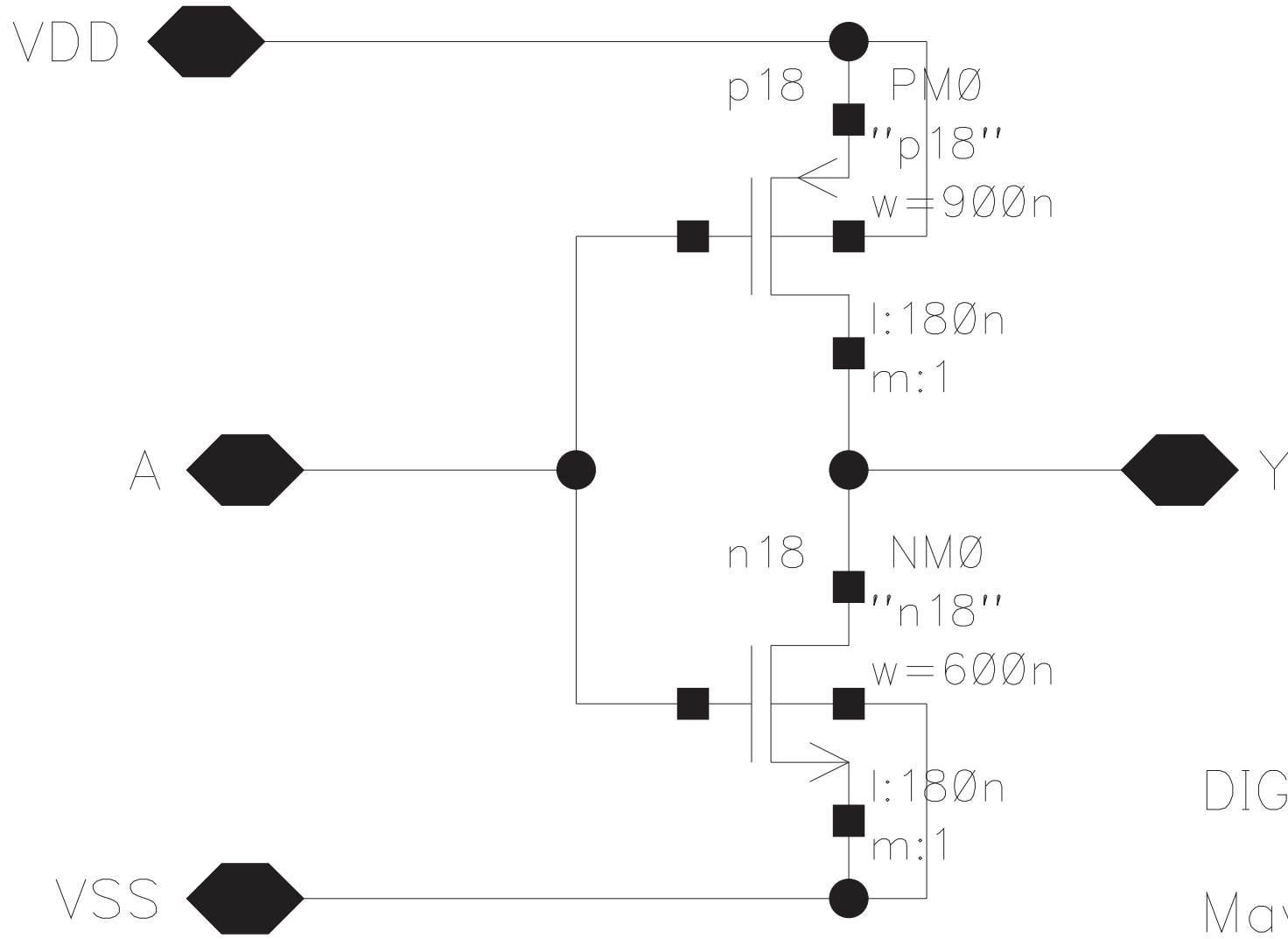
DIG\_DFFSRX1

May 17 2007

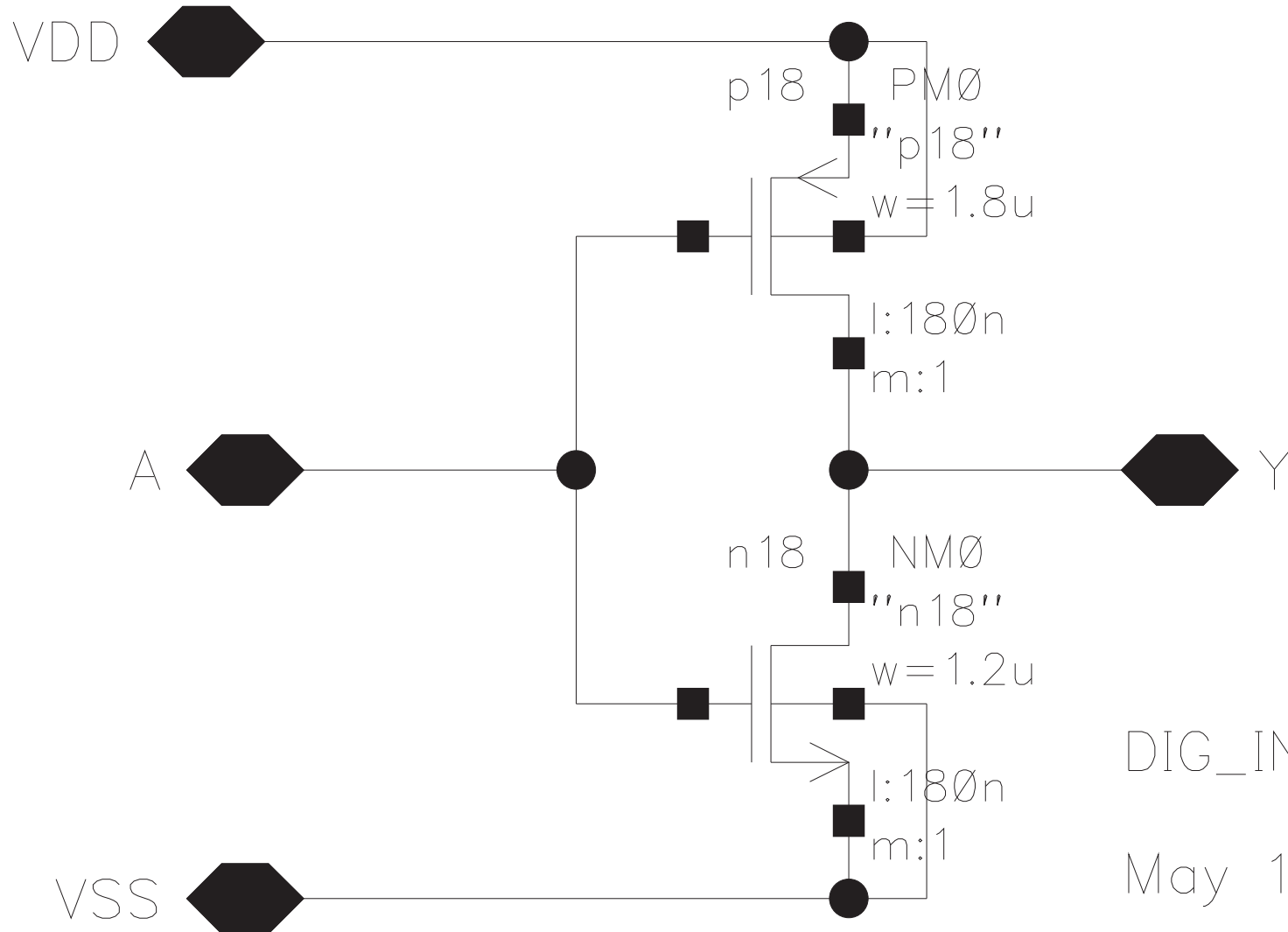
Haibin Yang



DIG\_DFFX1  
 May 17 2007  
 Haibin Yang



DIG\_INVX1  
May 17 2007  
Haibin Yang

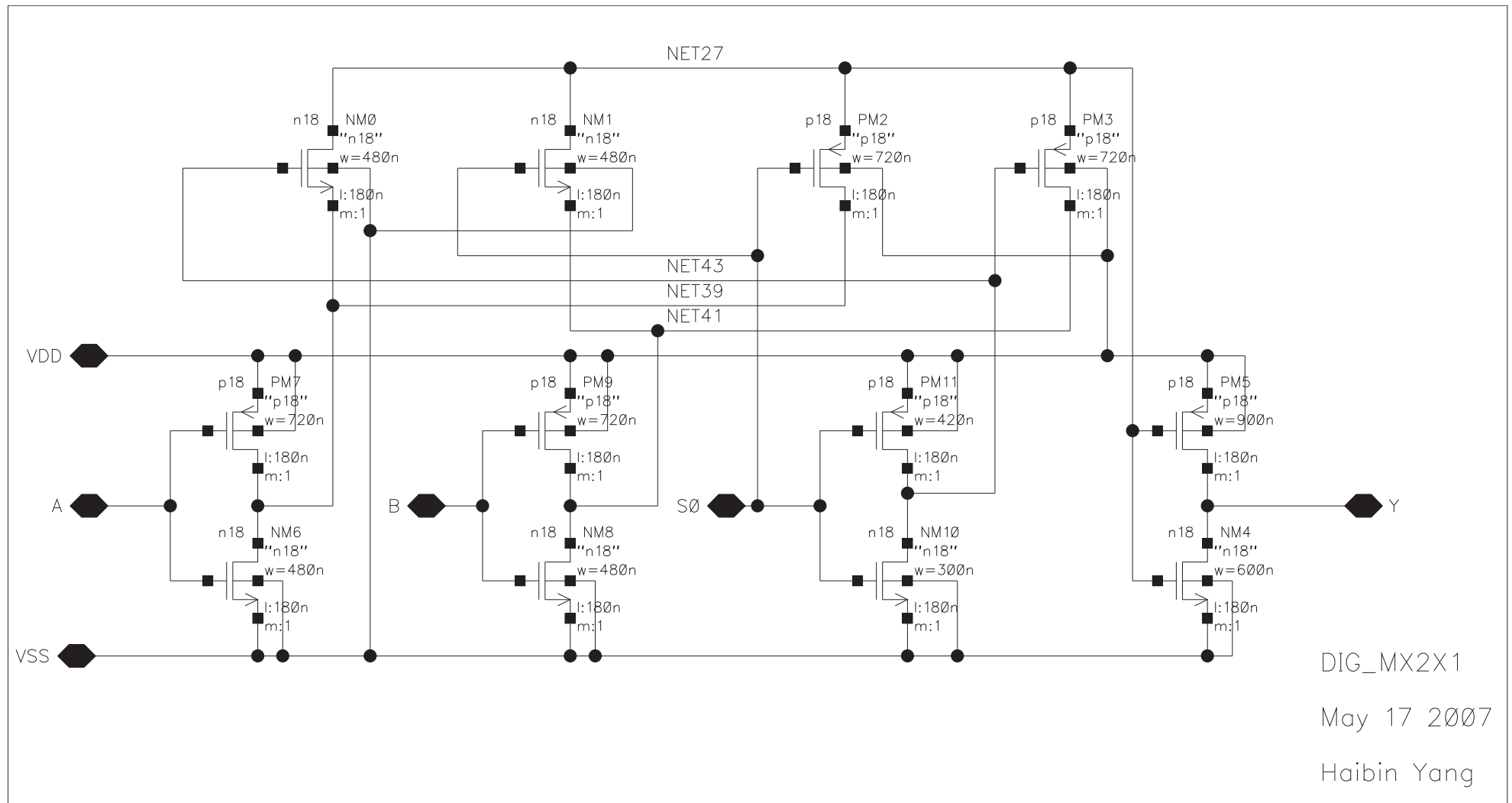


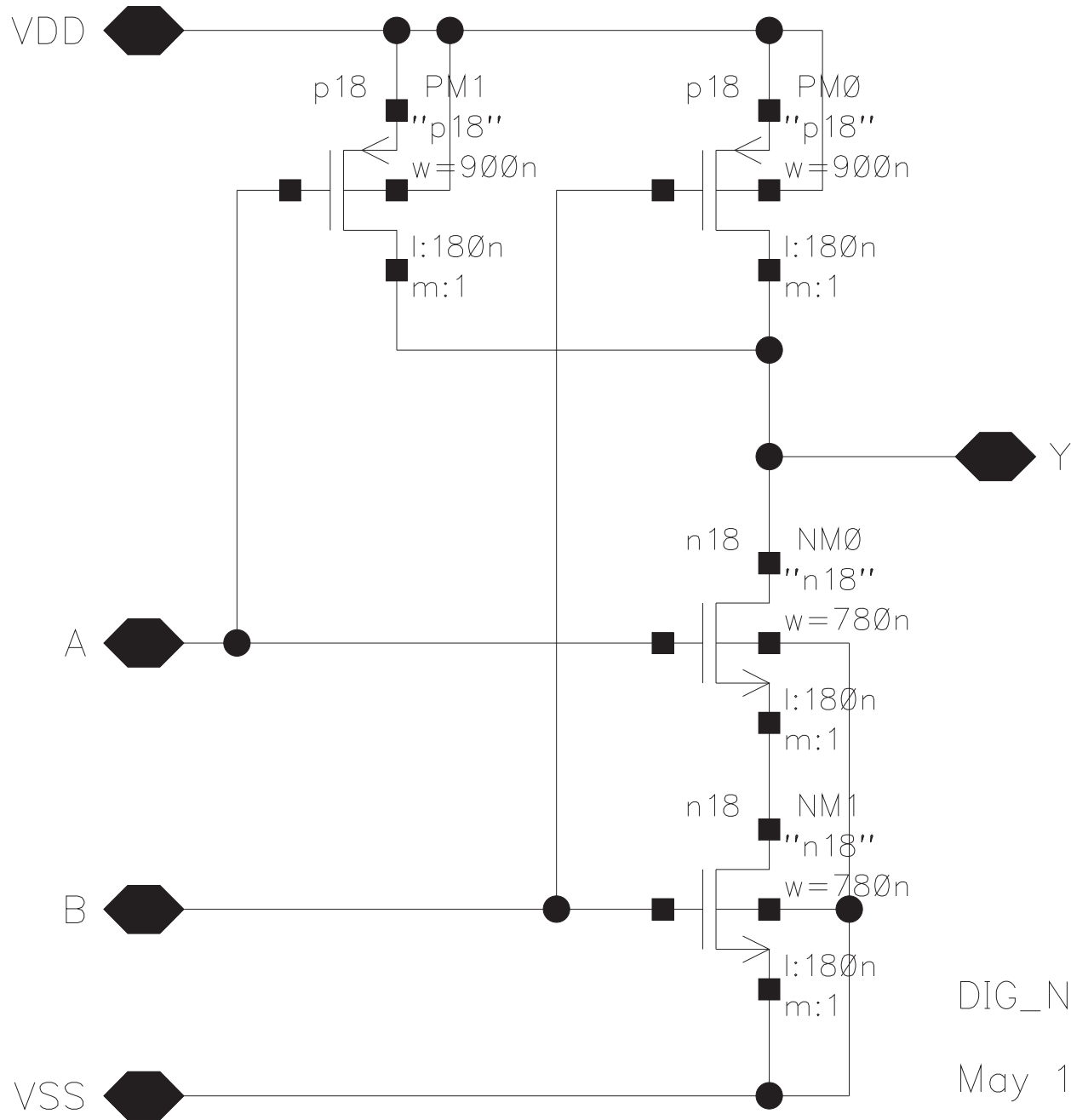
DIG\_INVX2

May 17 2007

Haibin Yang



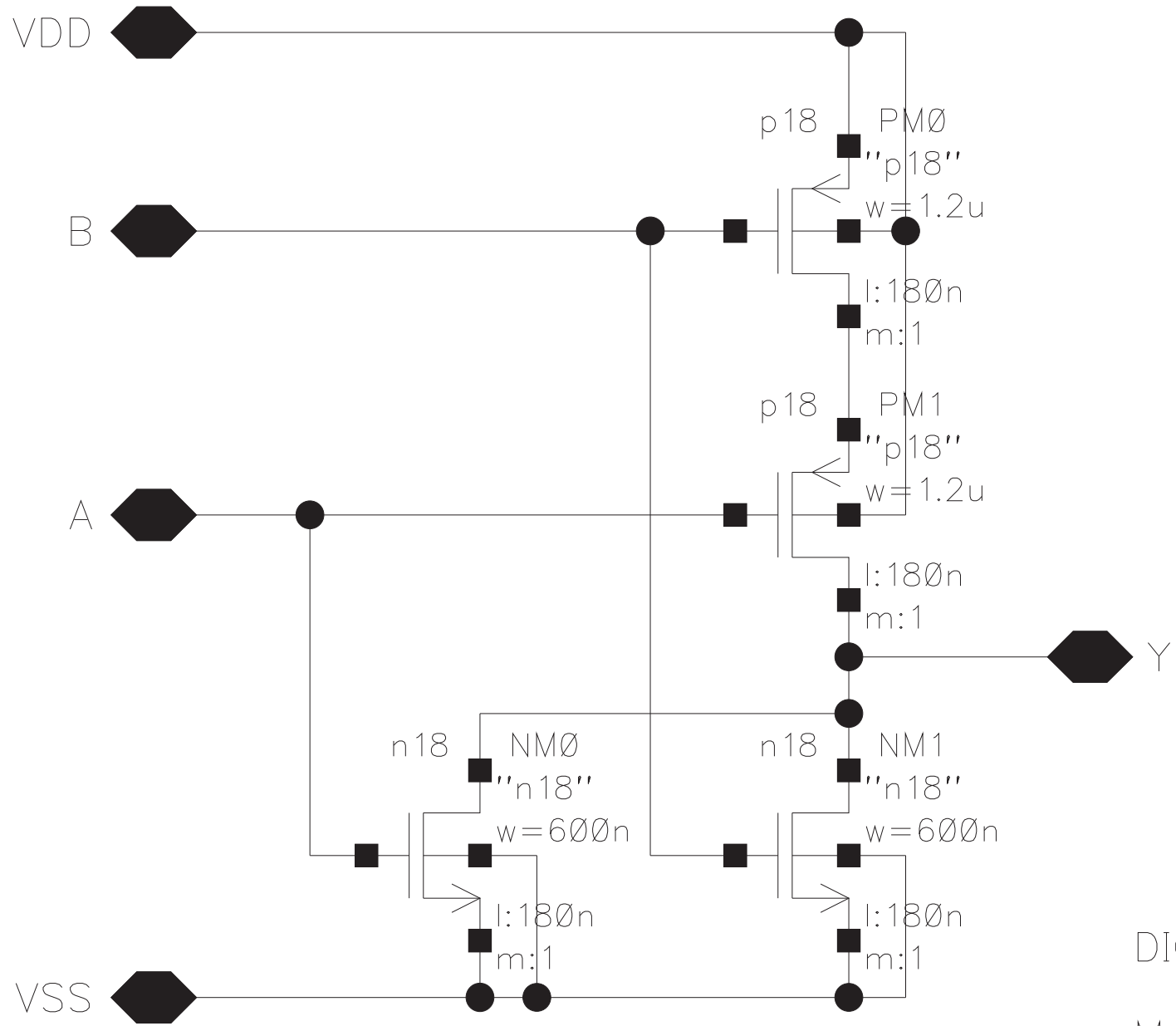




DIG\_NAND2X1

May 17 2007

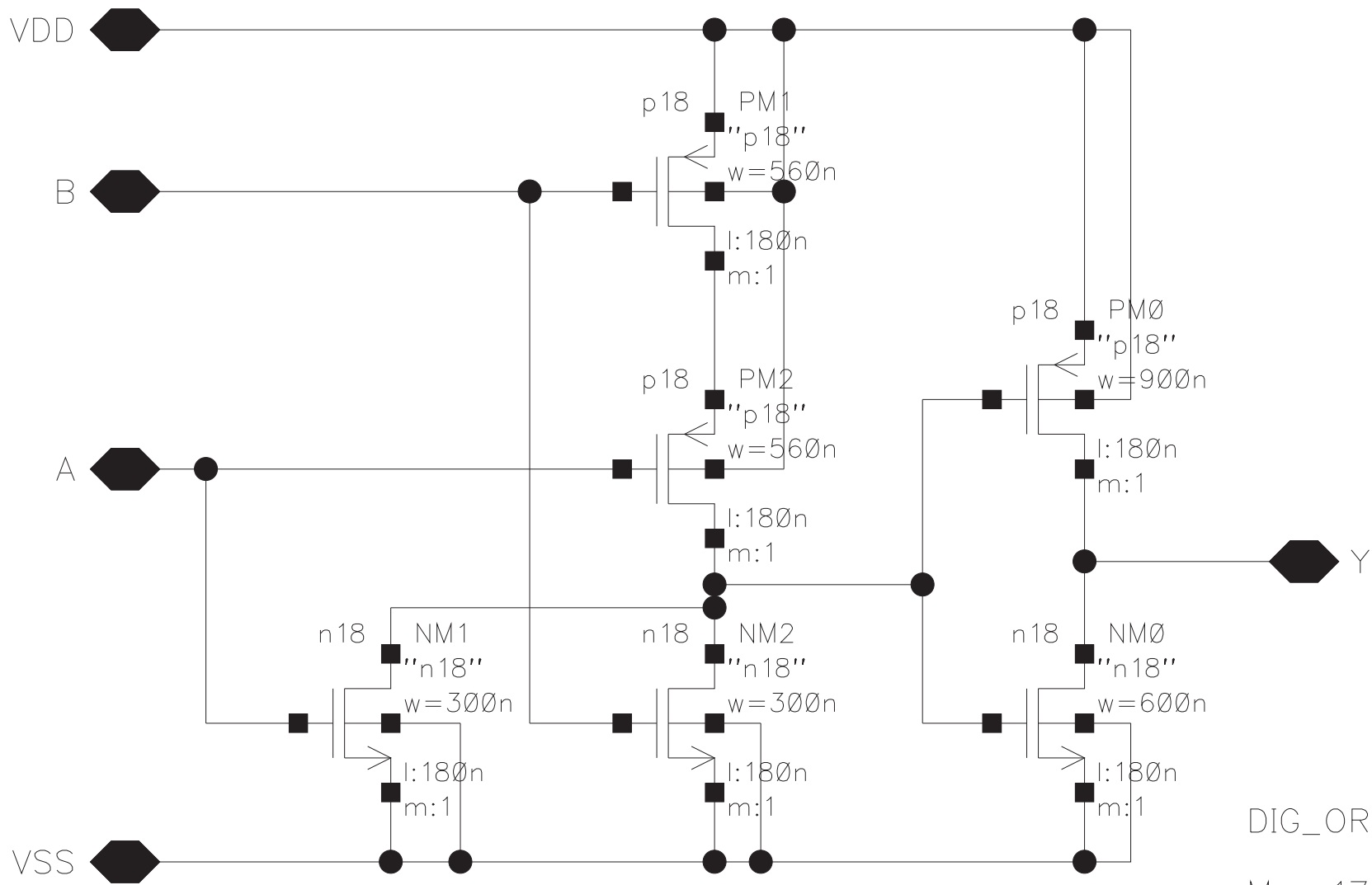
Haibin Yang



DIG\_NOR2X1

May 17 2007

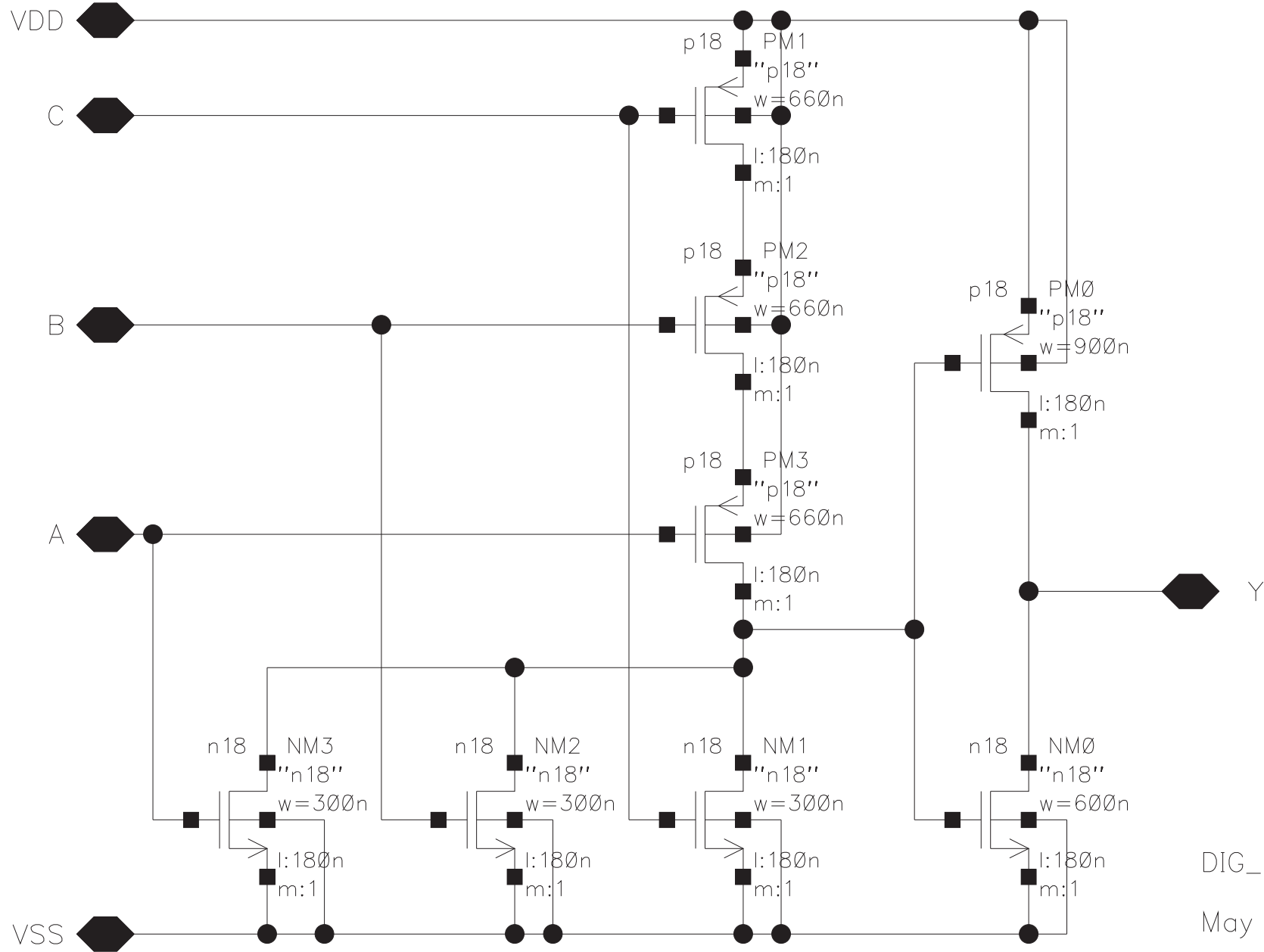
Haibin Yang



DIG\_OR2X1

May 17 2007

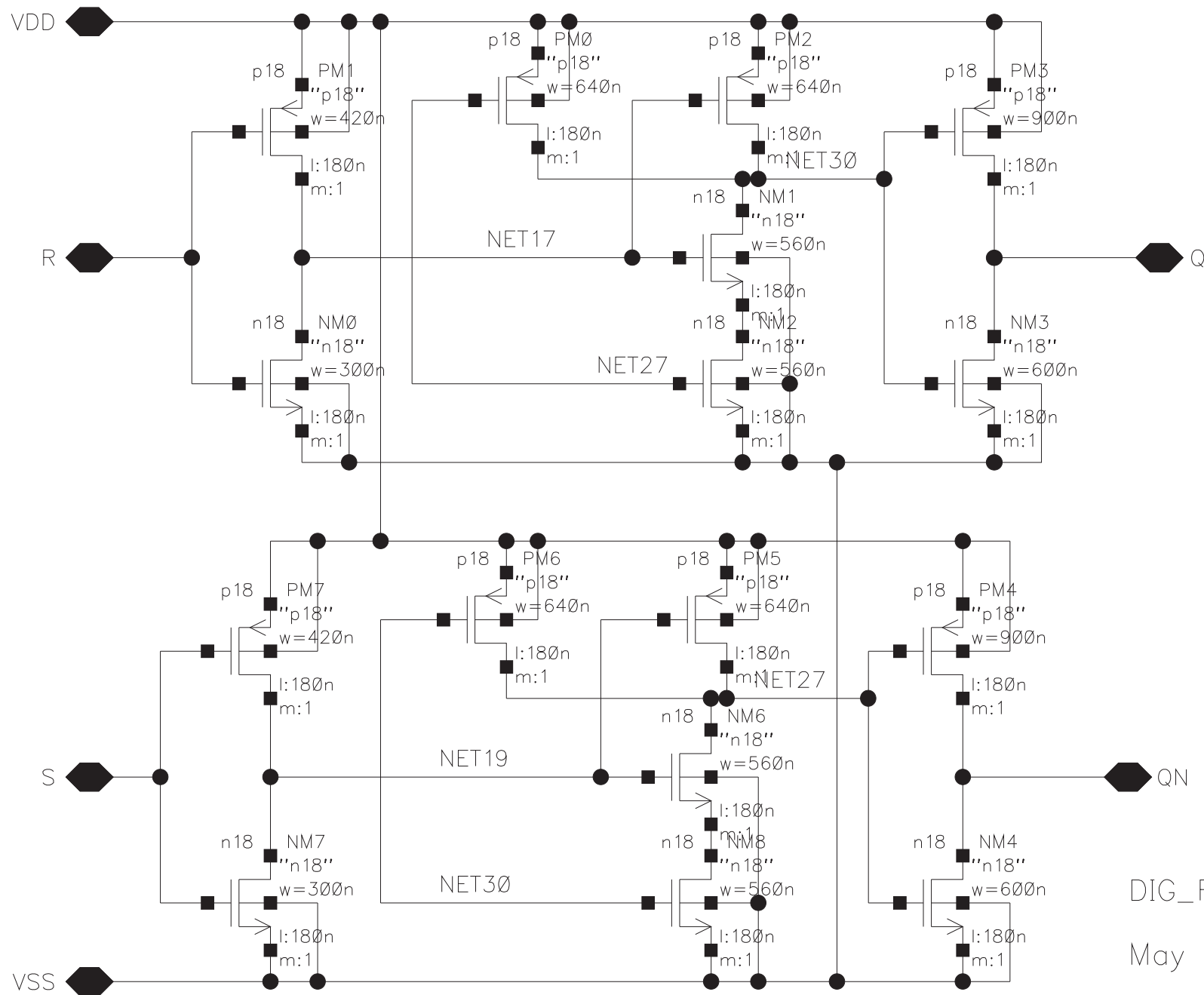
Haibin Yang



DIG\_OR3X1

May 17 2007

Haibin Yang



DIG\_RSLATX1

May 17 2007

Haibin Yang



VDD18

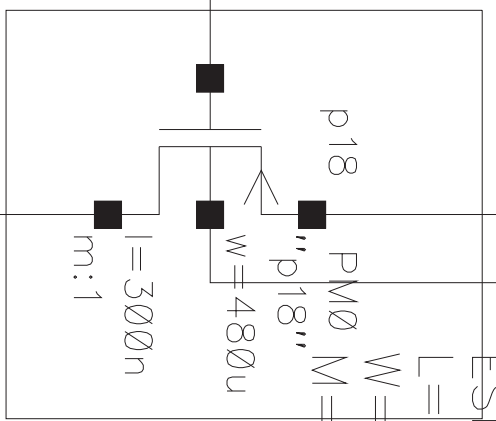


ESD device 1.8 pmos

L=0.3u

W=300u

M=16



p18

PM0  
"p18"

w=480u

l=300n

m:1

PAD

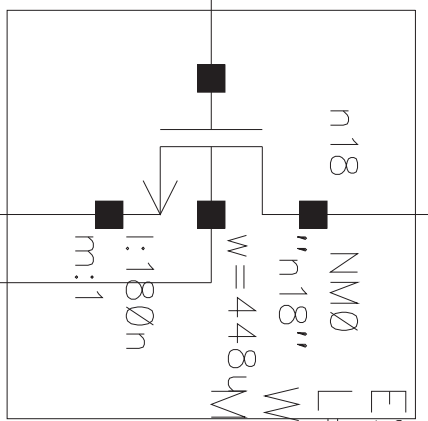


ESD device 1.8 nmos

L=0.18u

W=28u

M=16



n18

NM0  
"n18"

w=448u

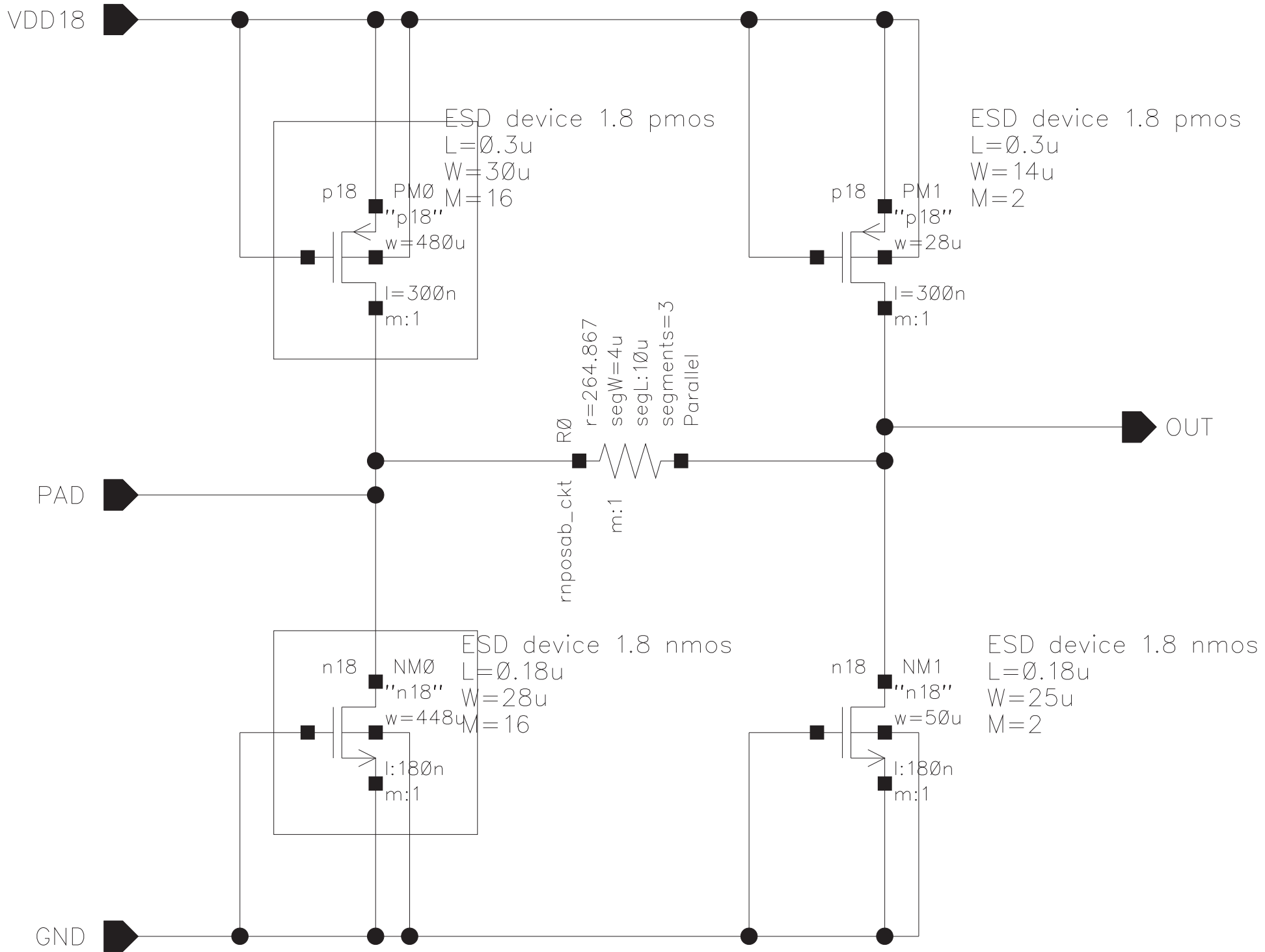
l:180n

m:1

GND







VDD33



ESD device 3.3 pmos

L=0.4u

W=500u

M=8

PM0 from Horizon

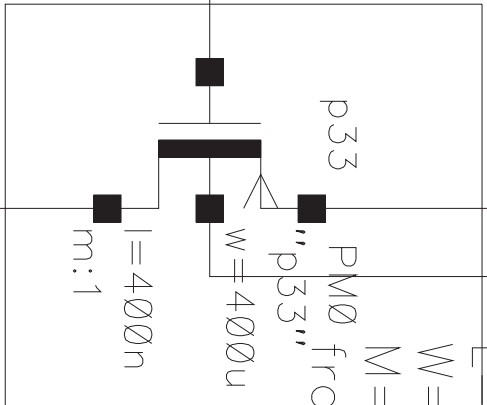
p33

"p33"

w=400u

l=400n

m:1



PAD



ESD device 3.3 nmos

L=0.4u

W=500u

M=8

n33 from Horizon

n33

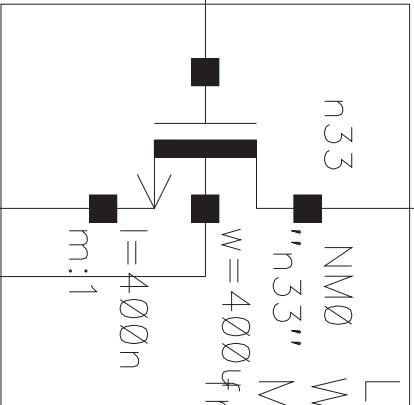
NM0

"n33"

w=400u

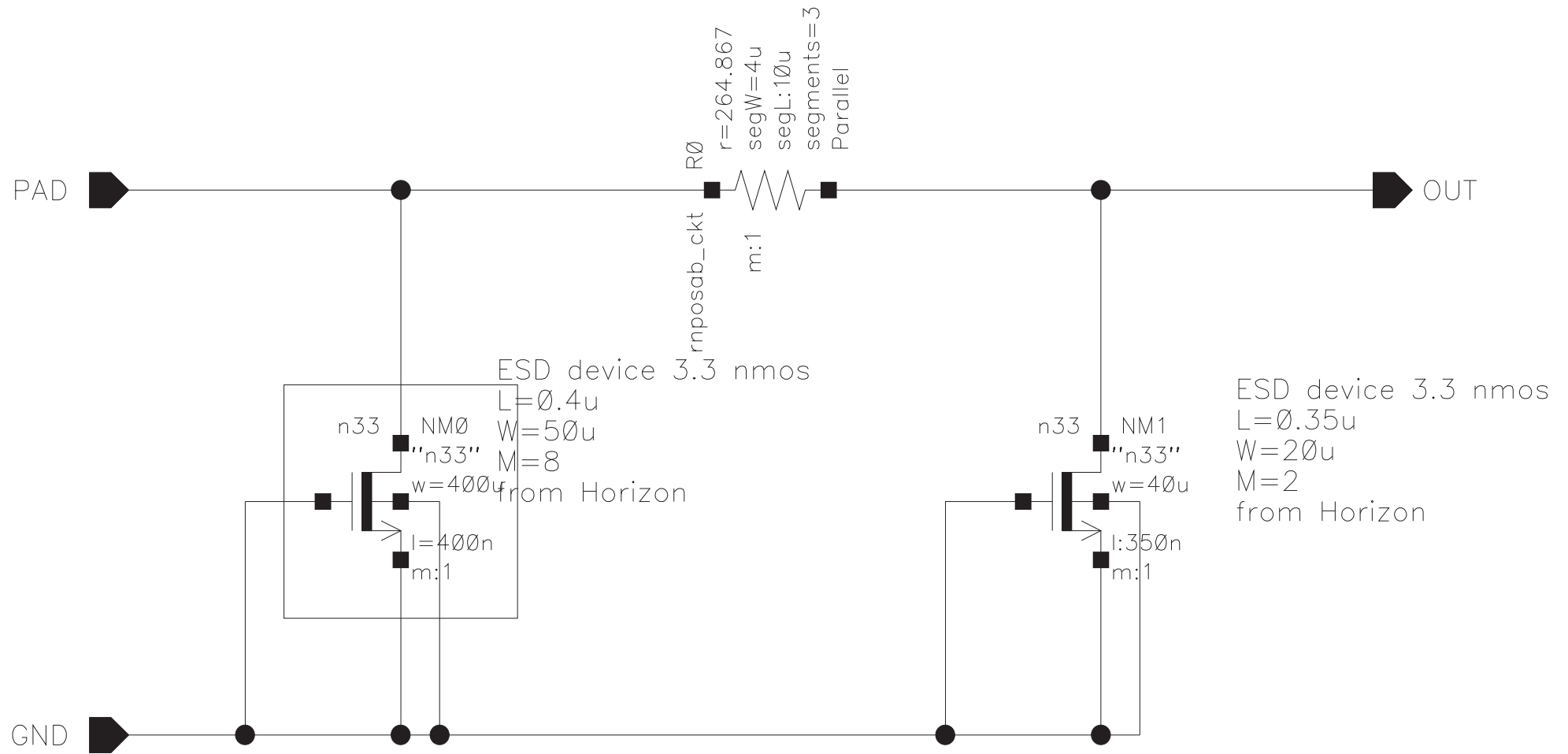
l=400n

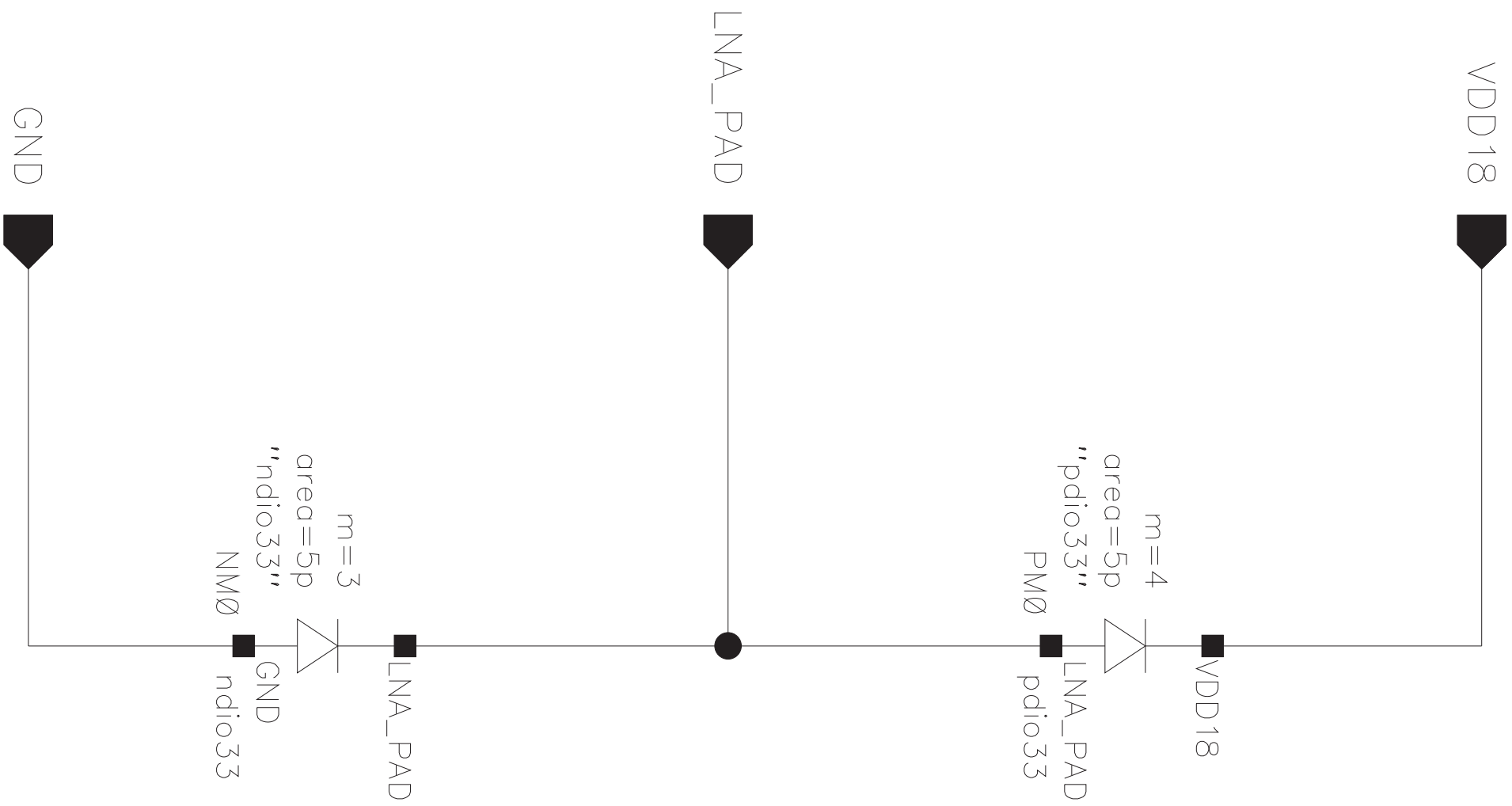
m:1



GND

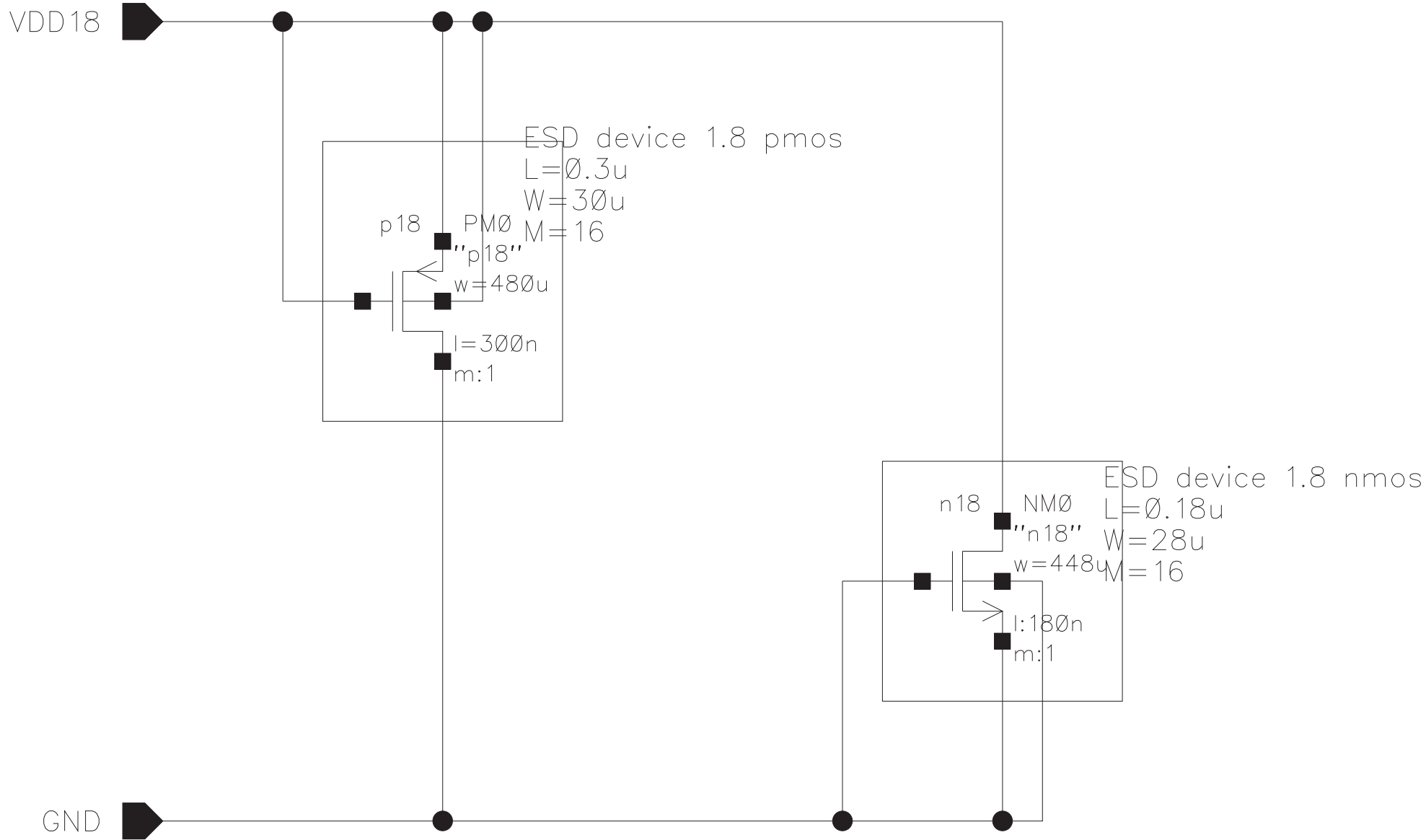




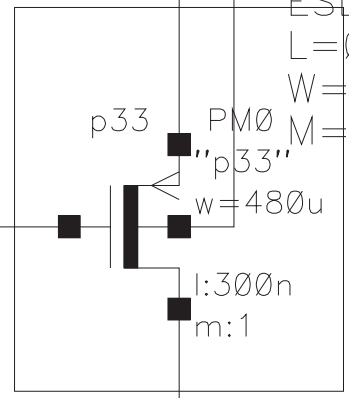


P+/Nwell diode  
 $L*W=\emptyset.5*1\emptyset$   
 $M=4$

N+/Psub diode  
 $L*W=\emptyset.5*1\emptyset$   
 $M=3$

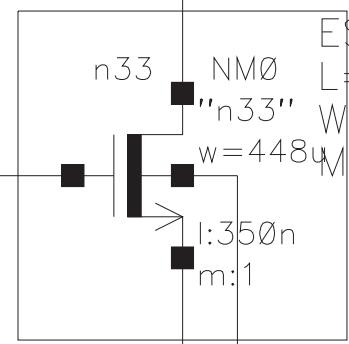


VDD\_IO

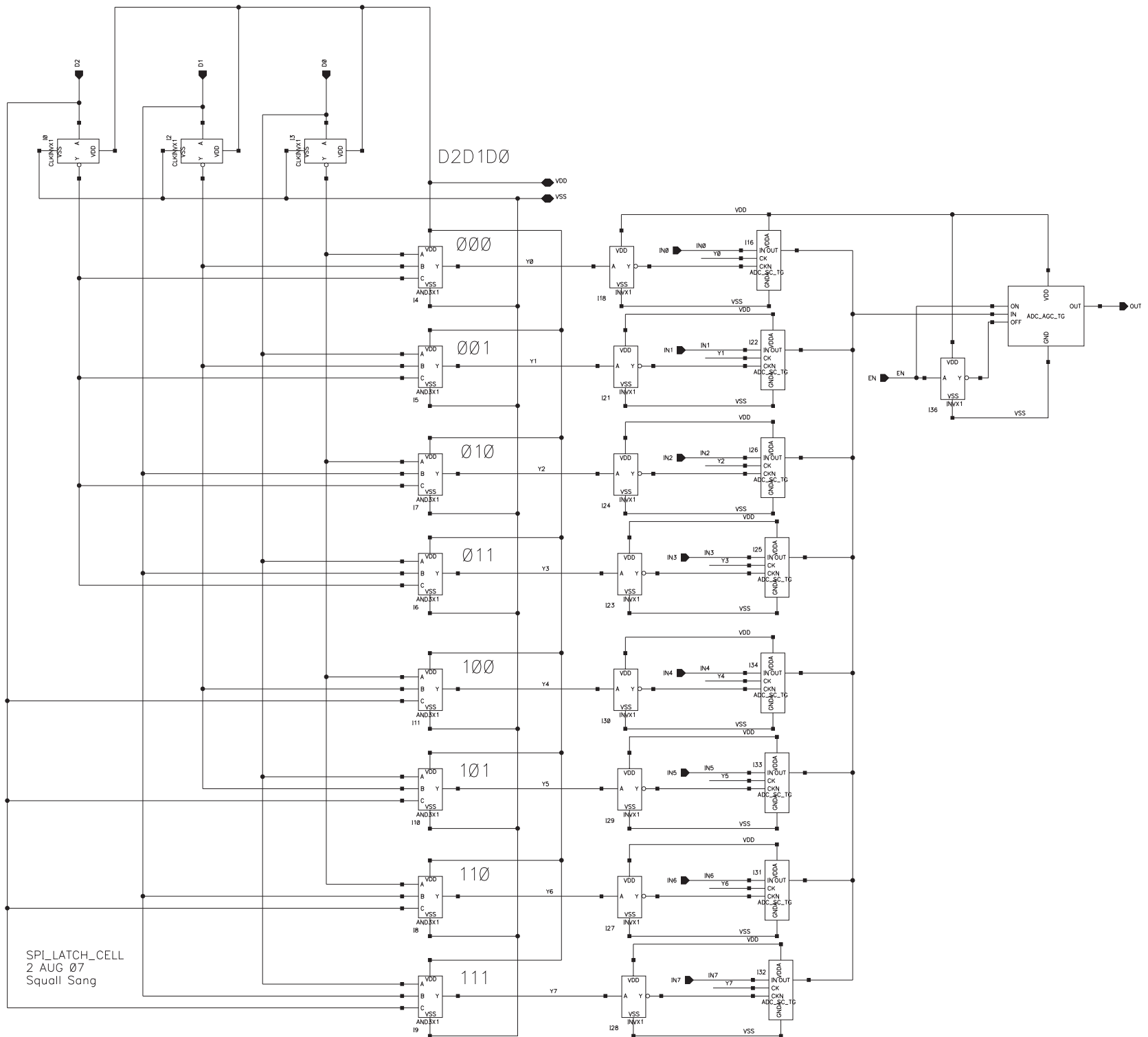


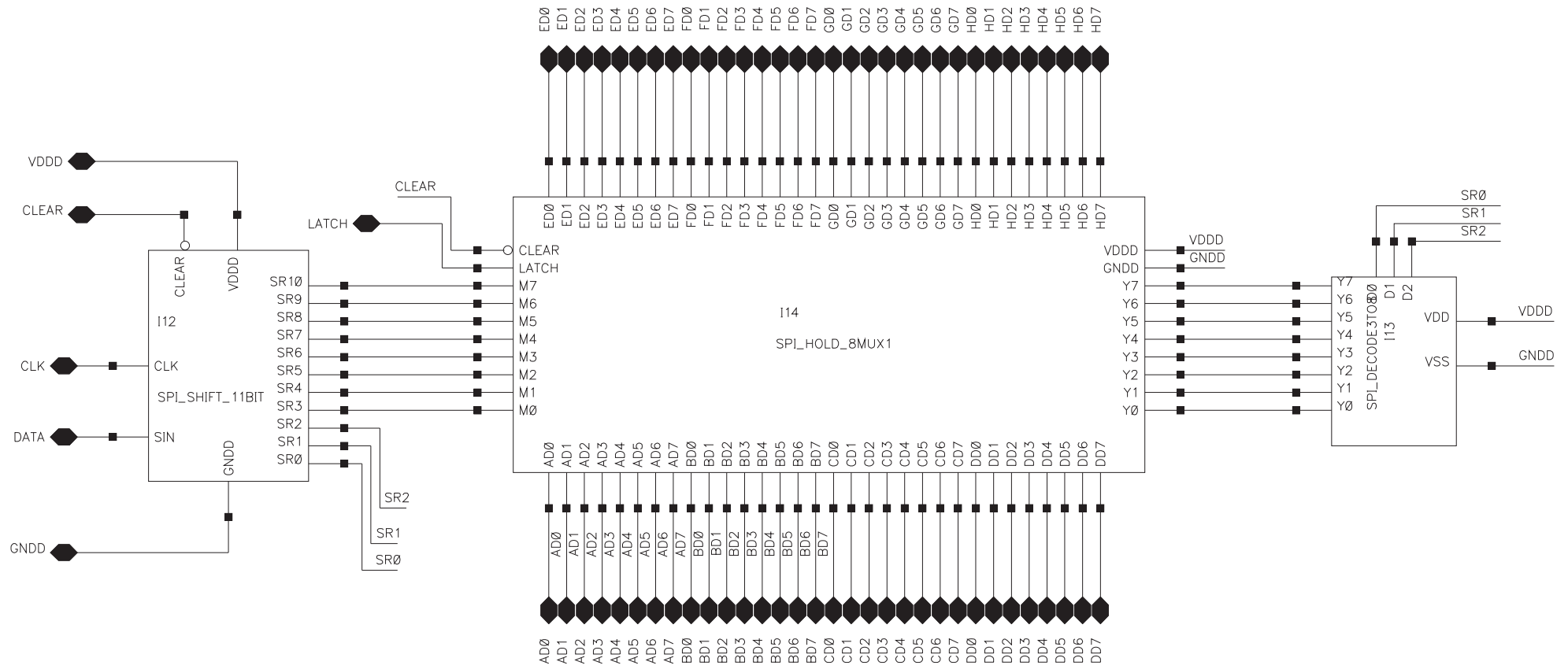
ESD device 3.3 pmos  
L=0.3u  
W=30u  
M=16

GND

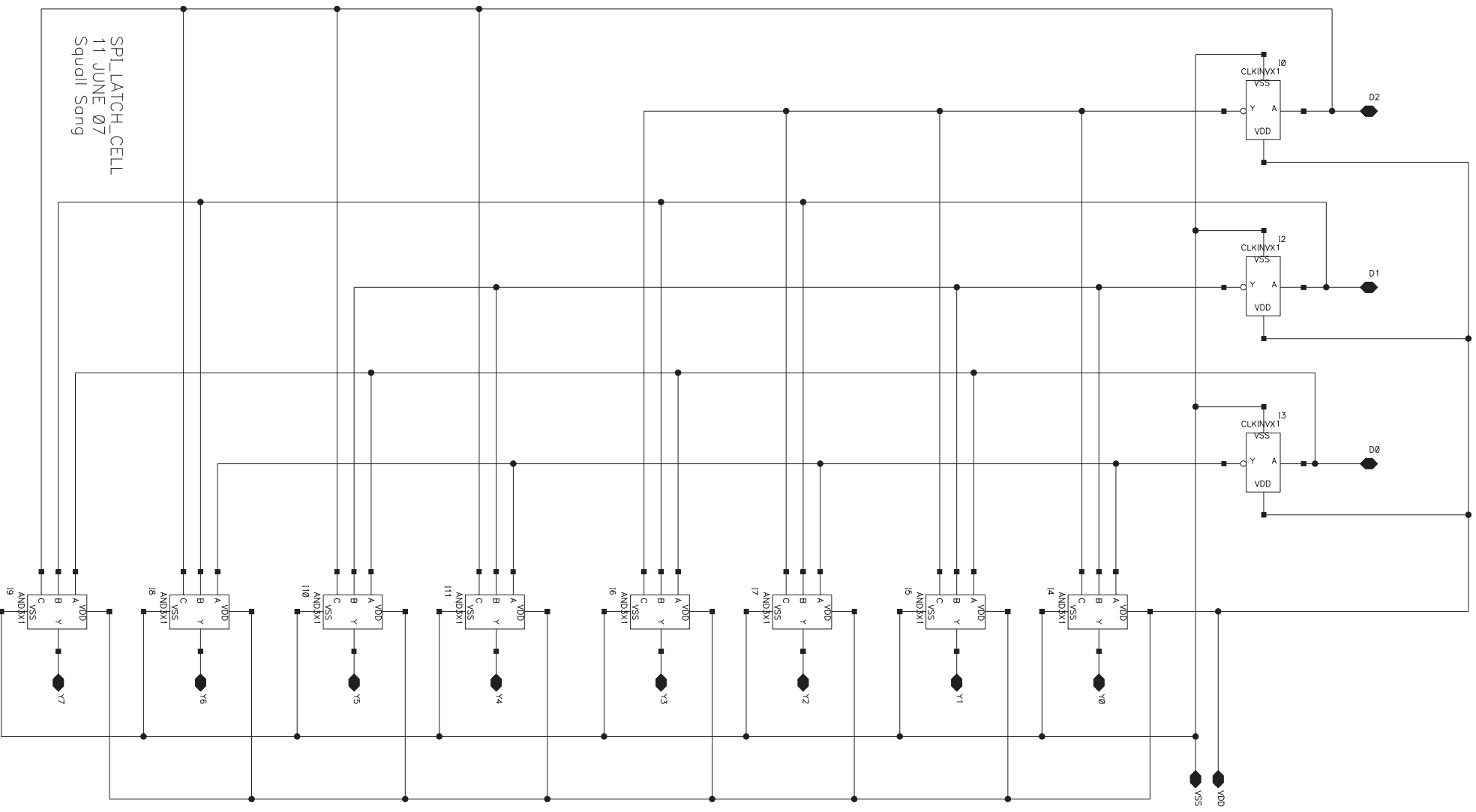


ESD device 3.3 nmos  
L=0.35u  
W=28u  
M=16

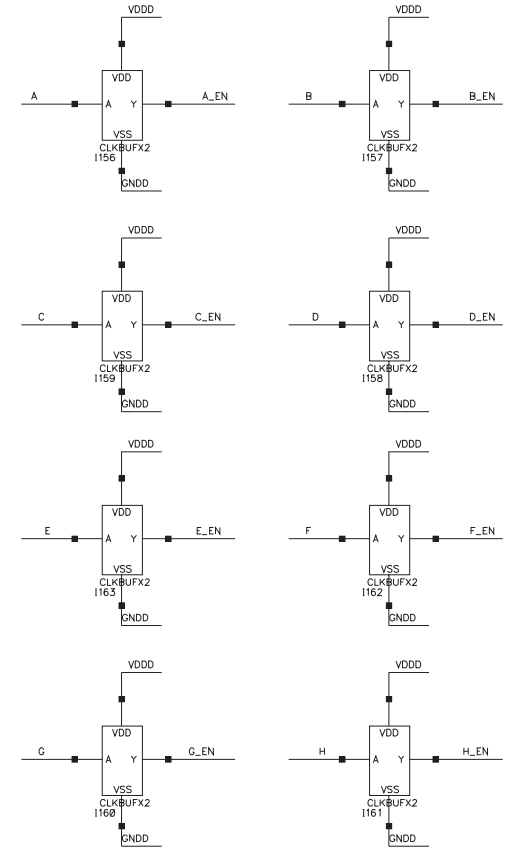
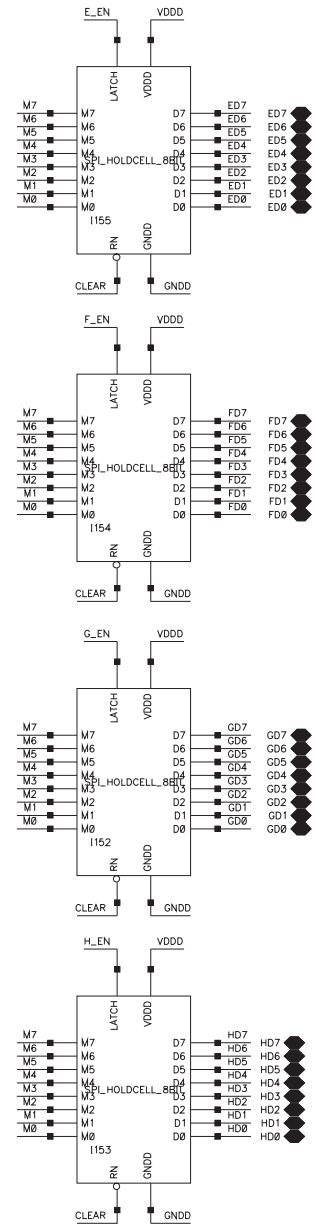
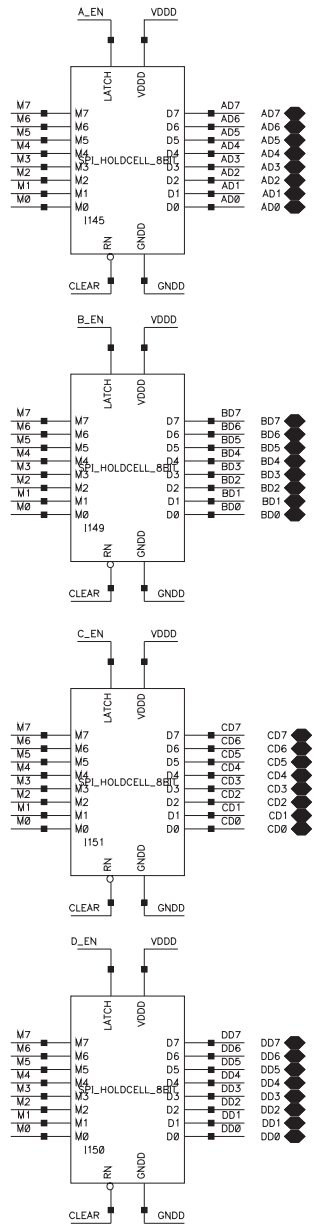
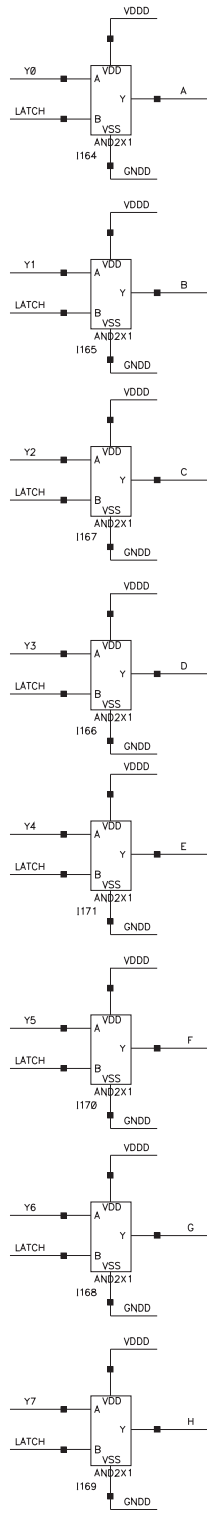




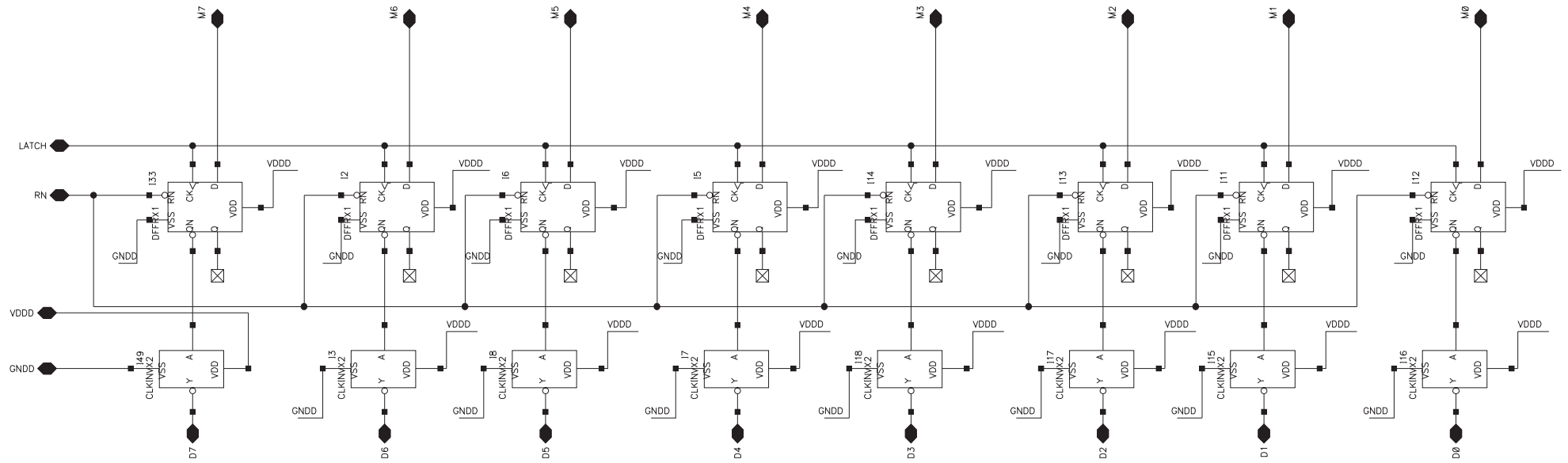




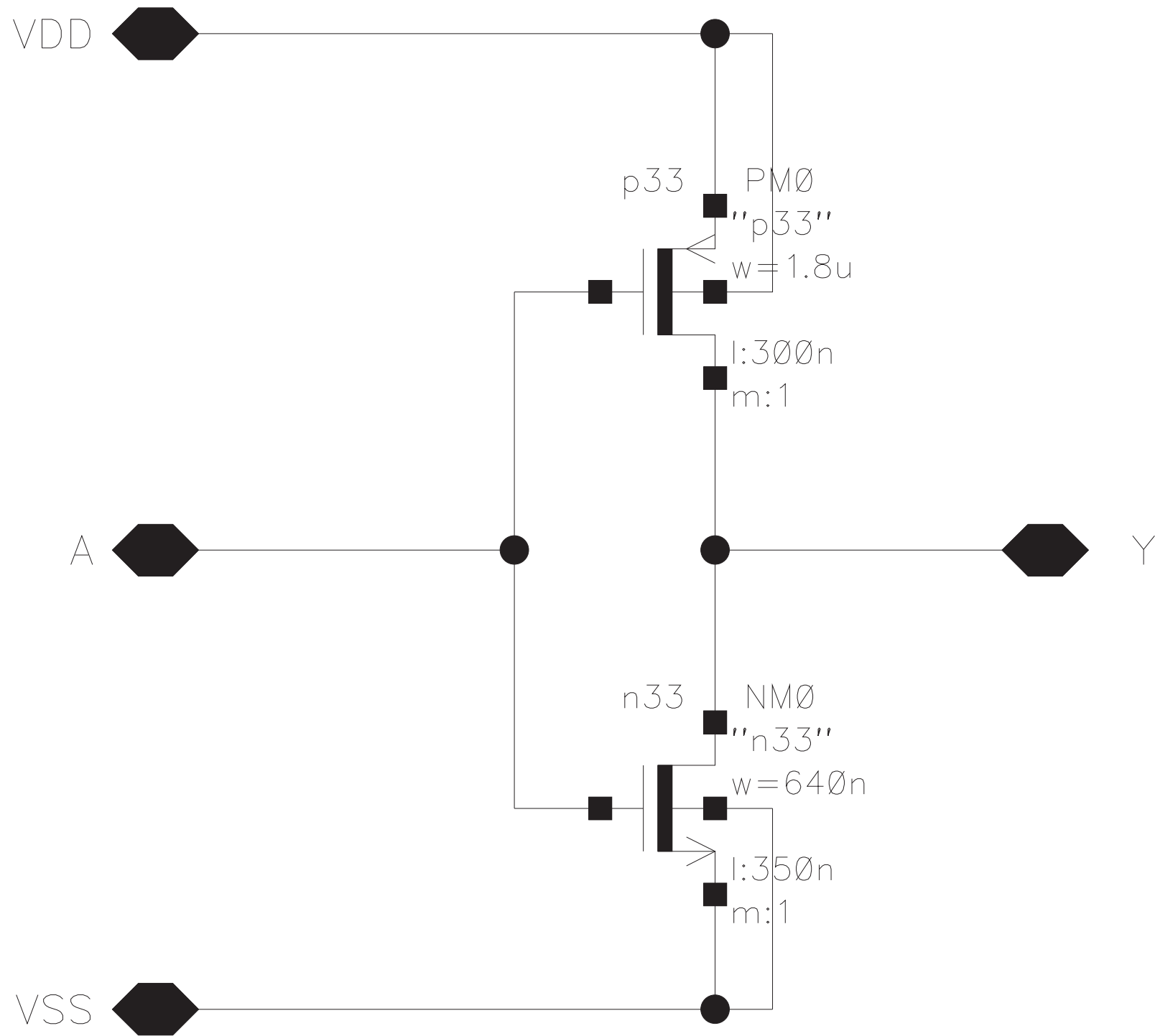
- VDD
- GNDD
- LATCH
- CLEAR
- Y0
- Y1
- Y2
- Y3
- Y4
- Y5
- Y6
- Y7
- M0
- M1
- M2
- M3
- M4
- M5
- M6
- M7

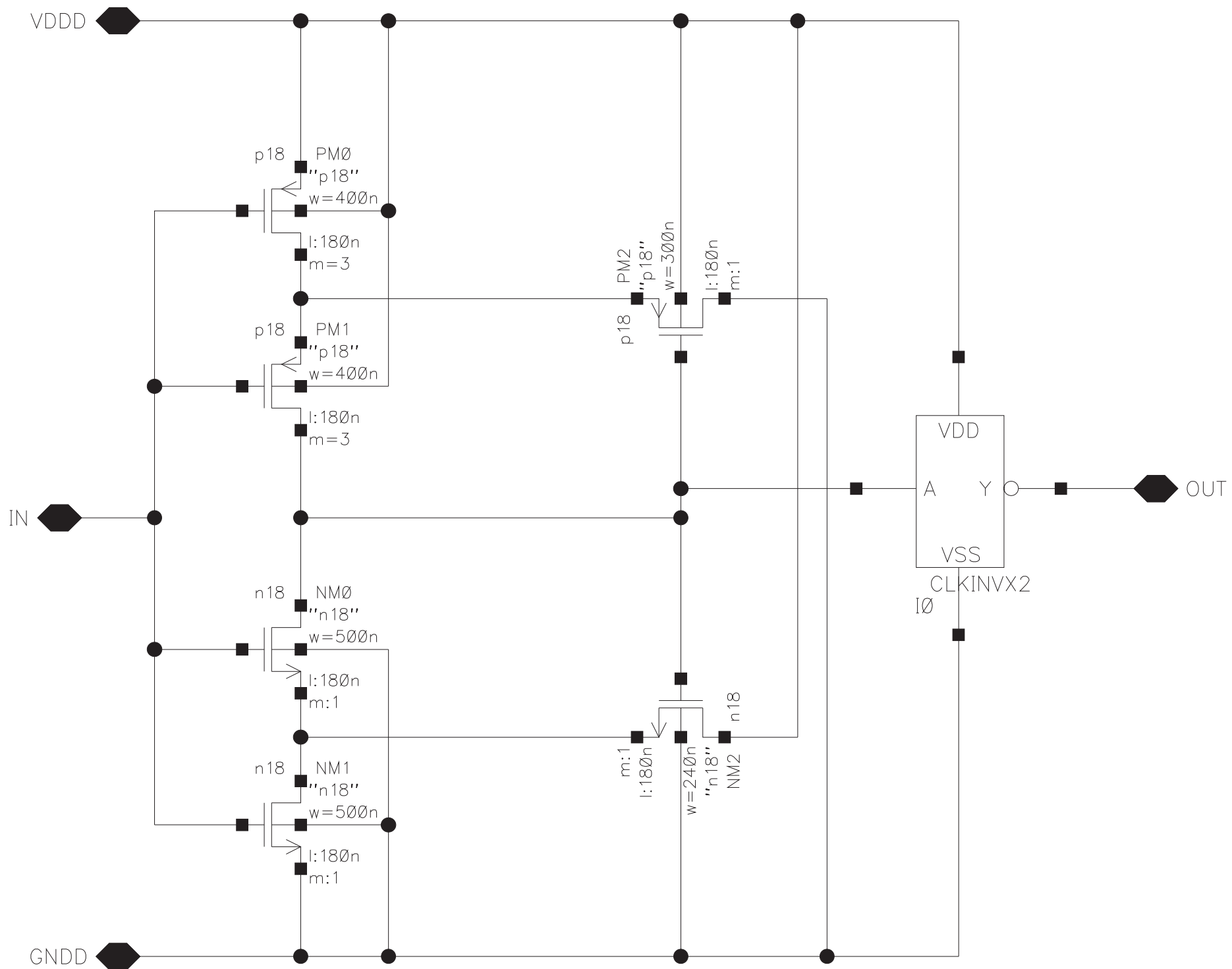


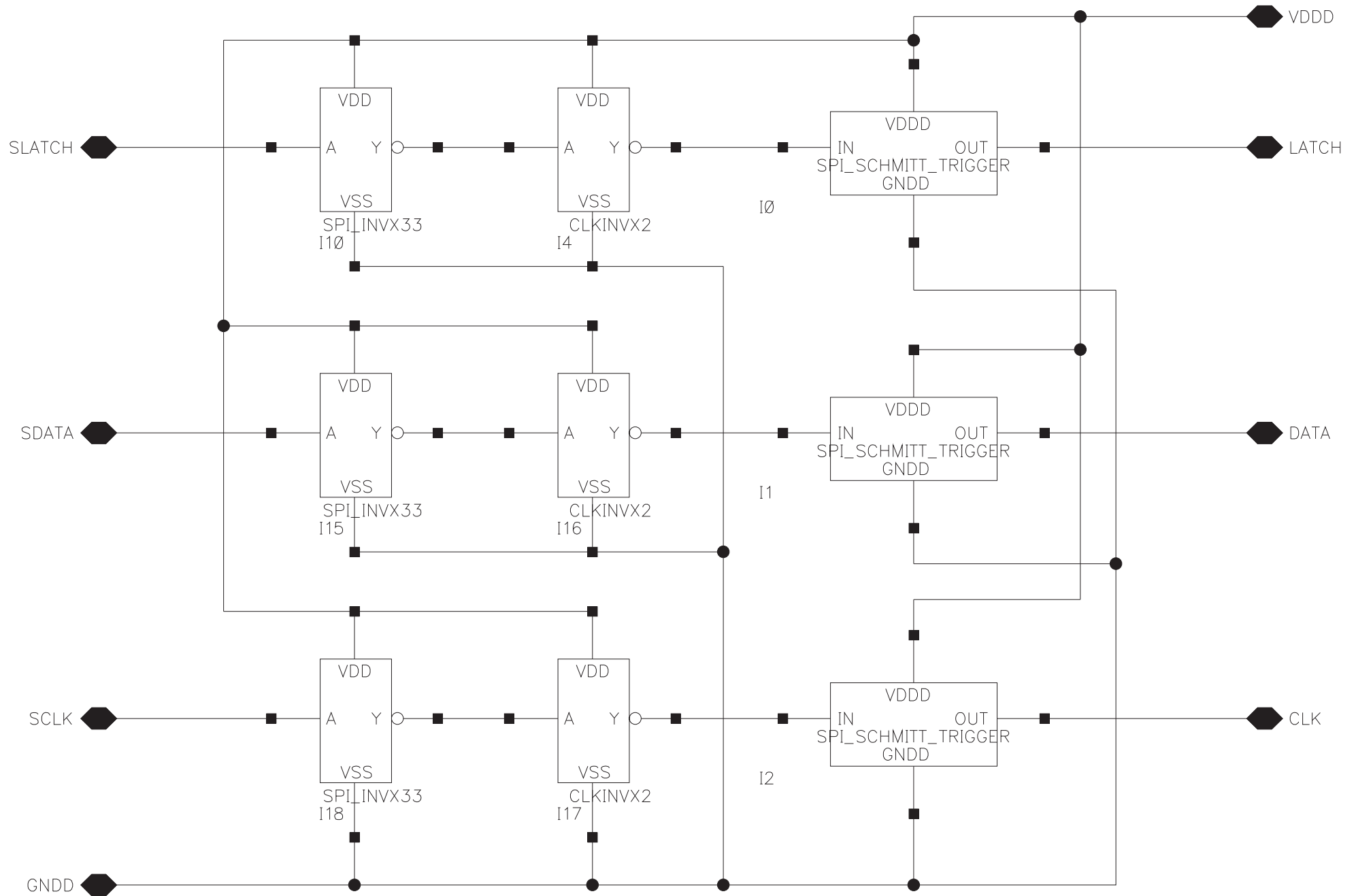
SPI HOLD STAGE 8MUX1  
11 JUNE 07  
Squall Sang

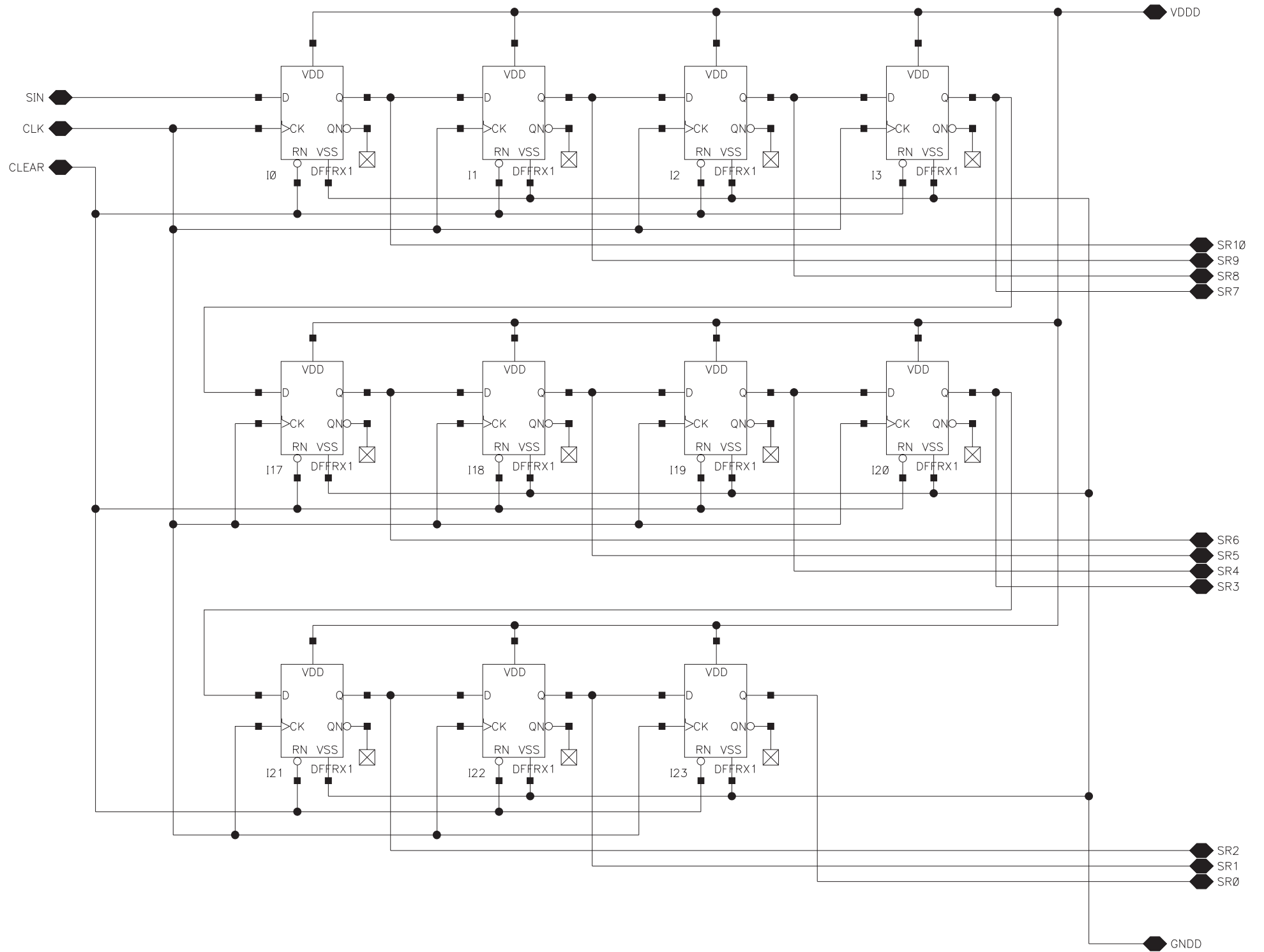


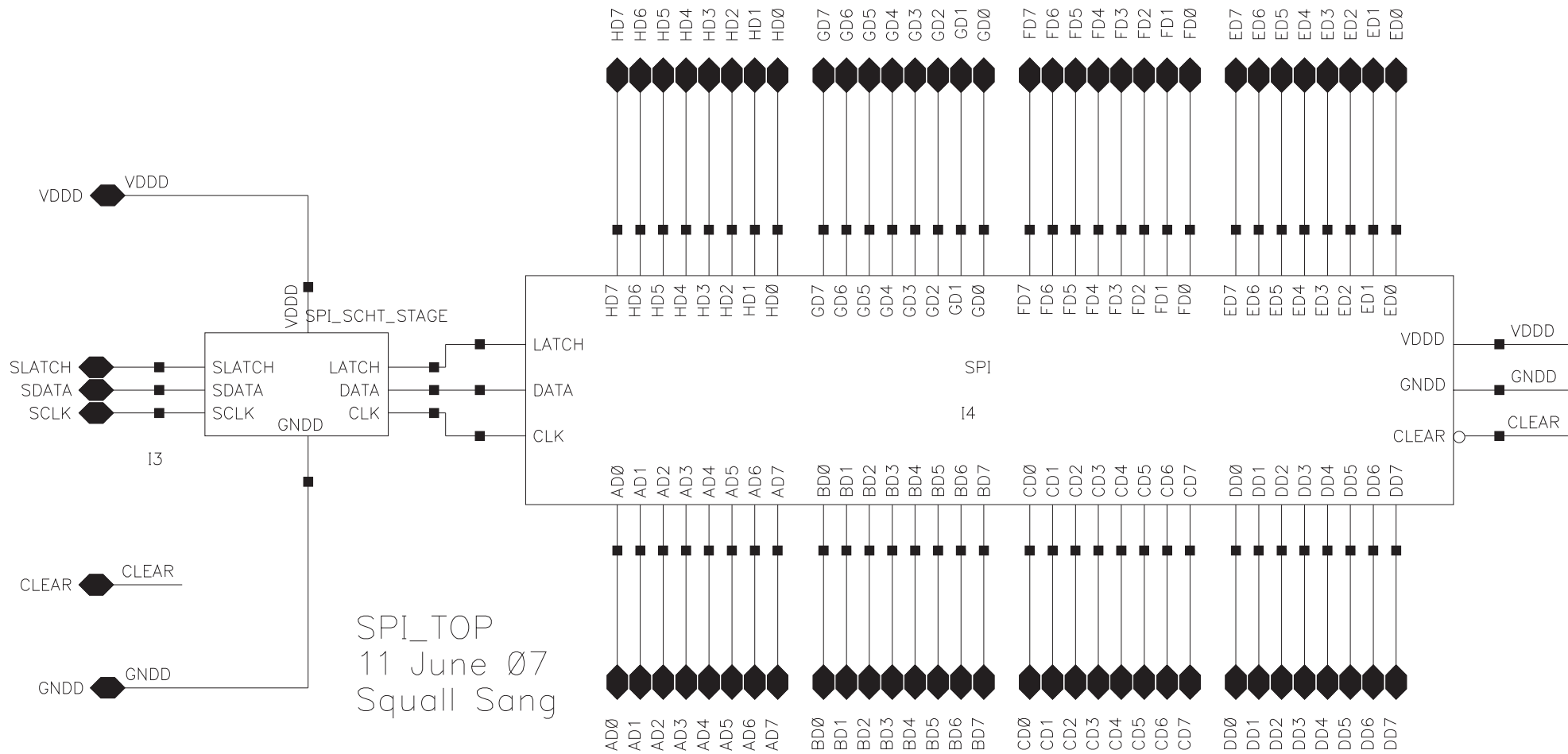
SPI HOLD CELL 8BIT  
 12 JUNE 07  
 Squall Sang





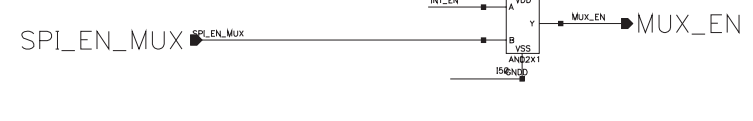
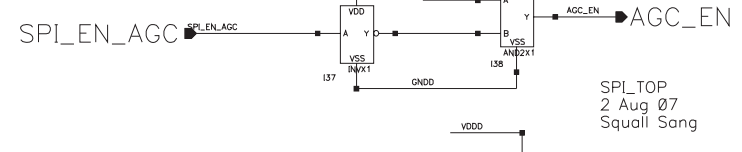
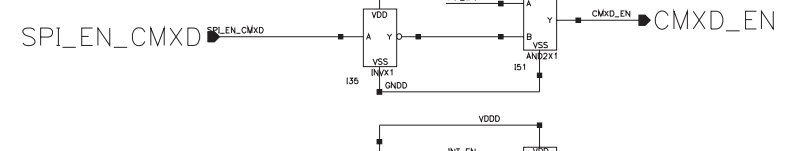
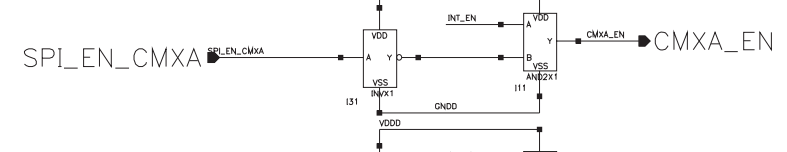
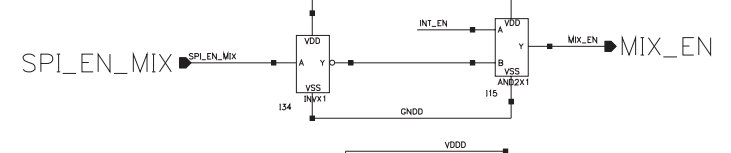
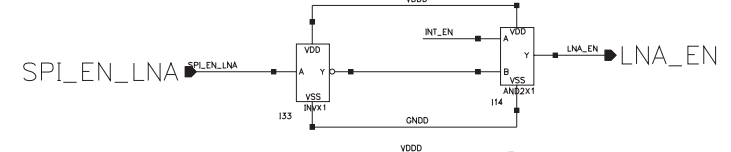
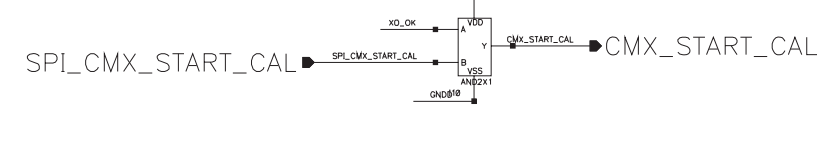
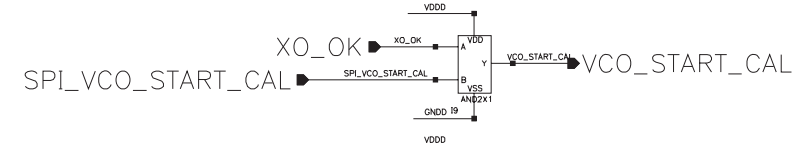
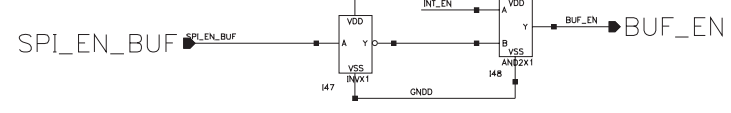
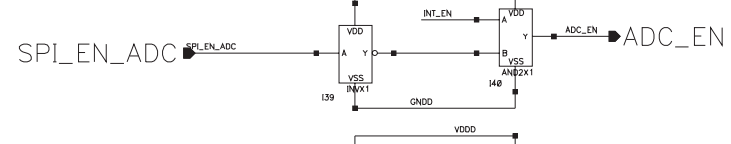
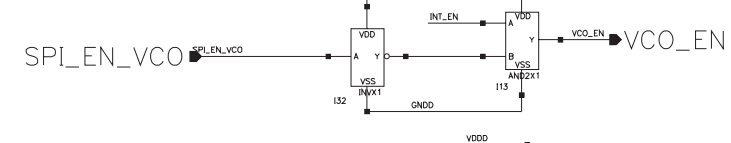
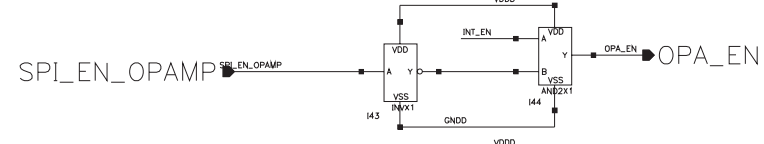
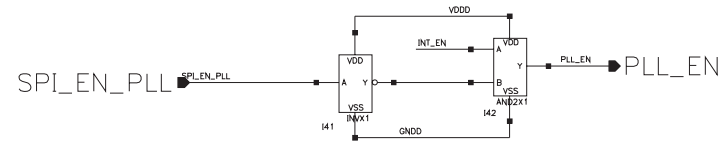
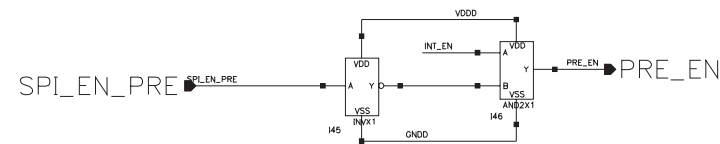
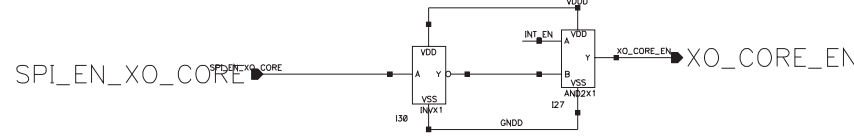
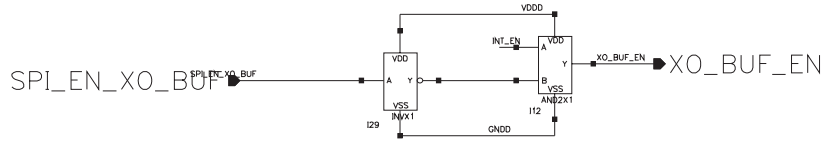
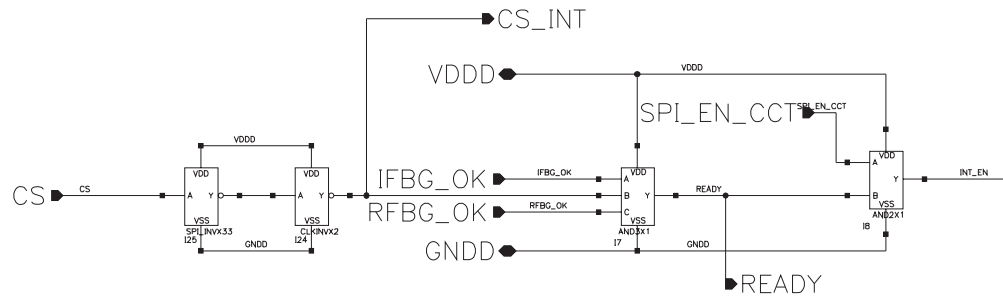




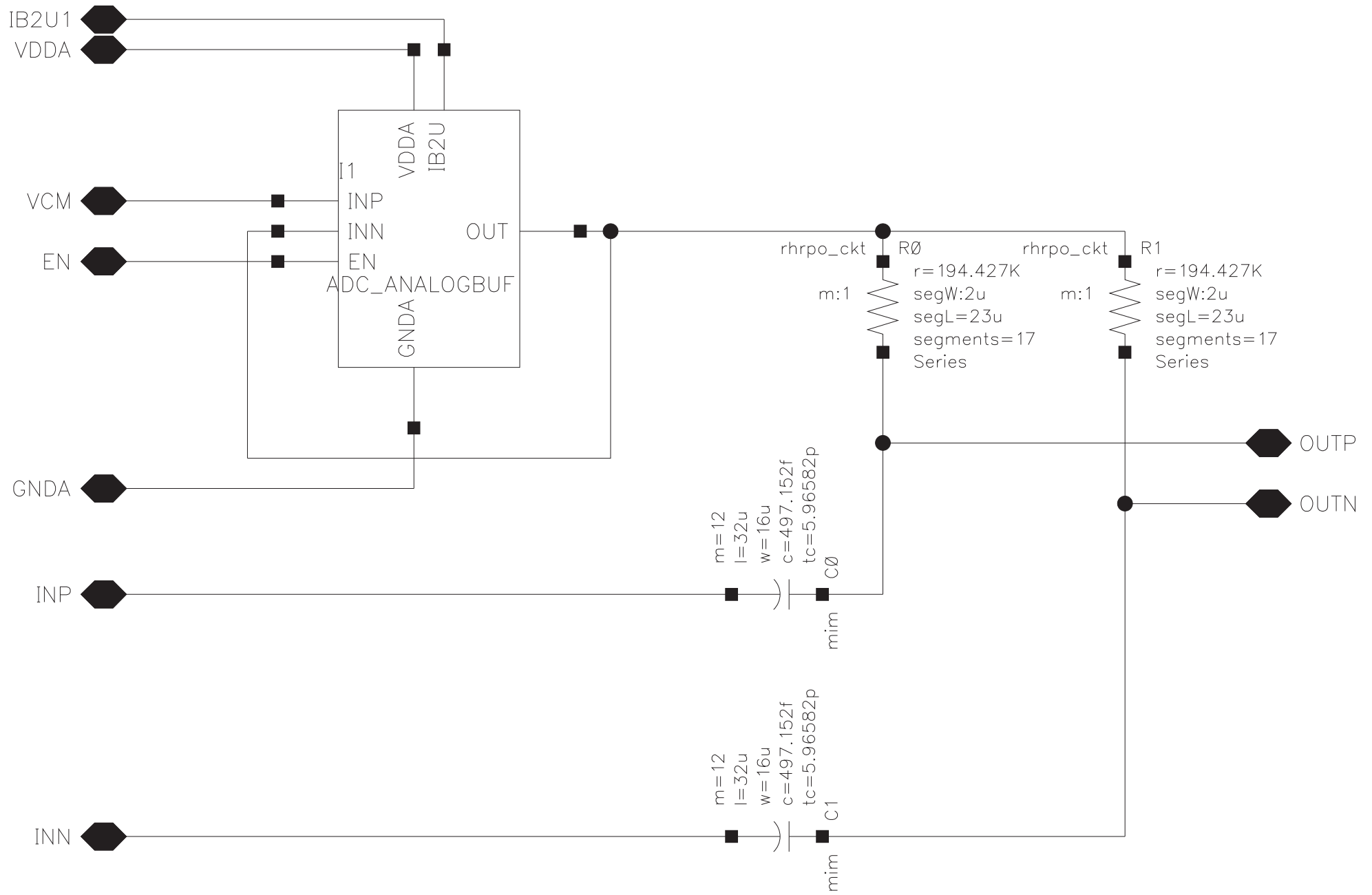


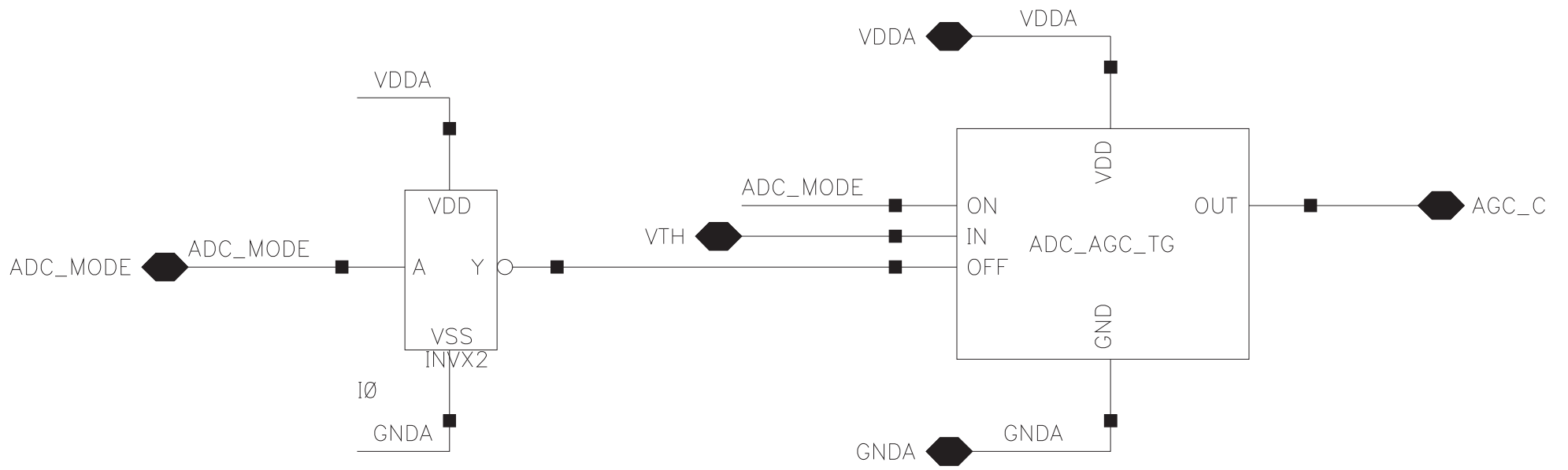
SPI\_TOP  
 11 June 07  
 Squall Sang

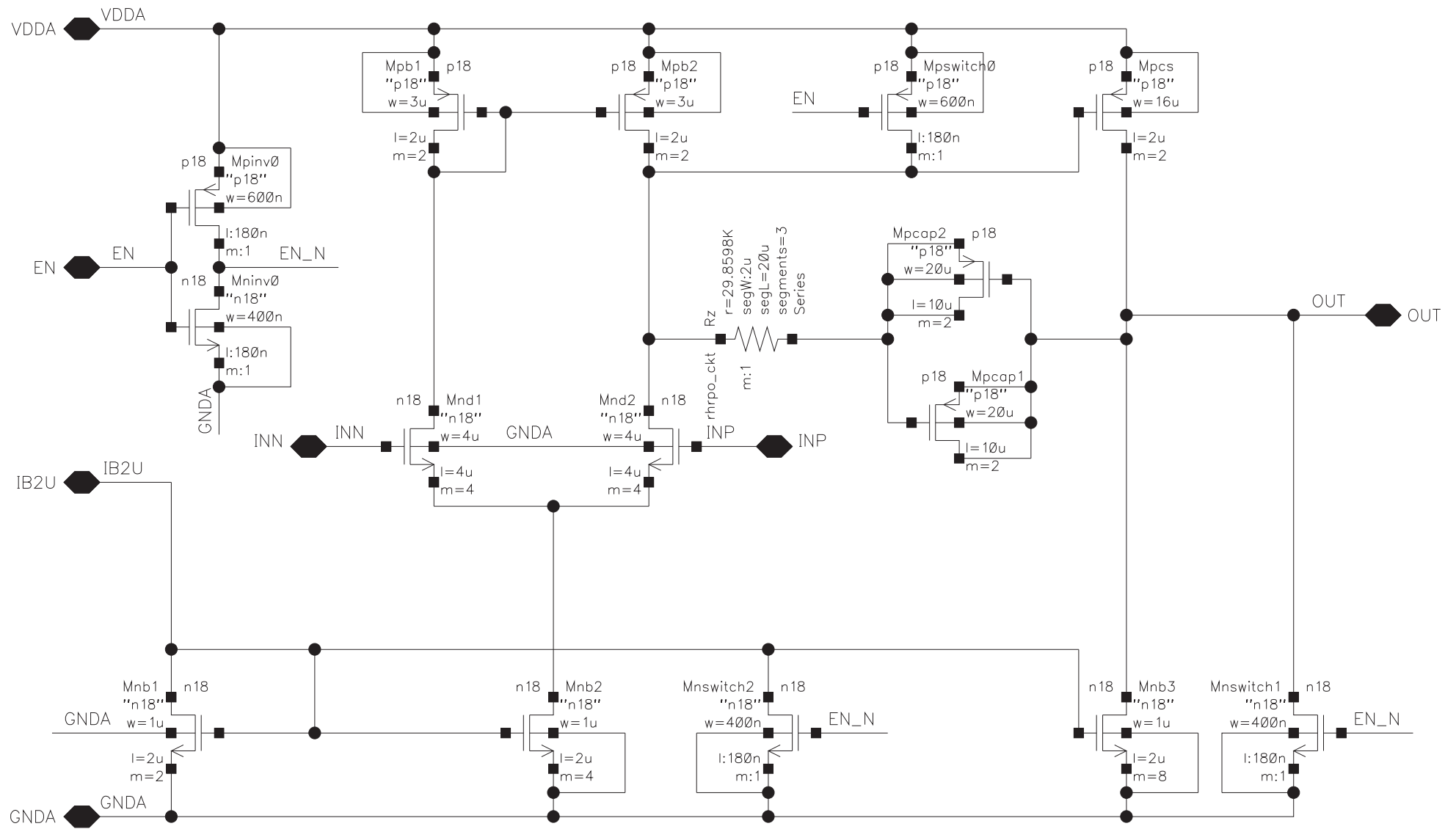


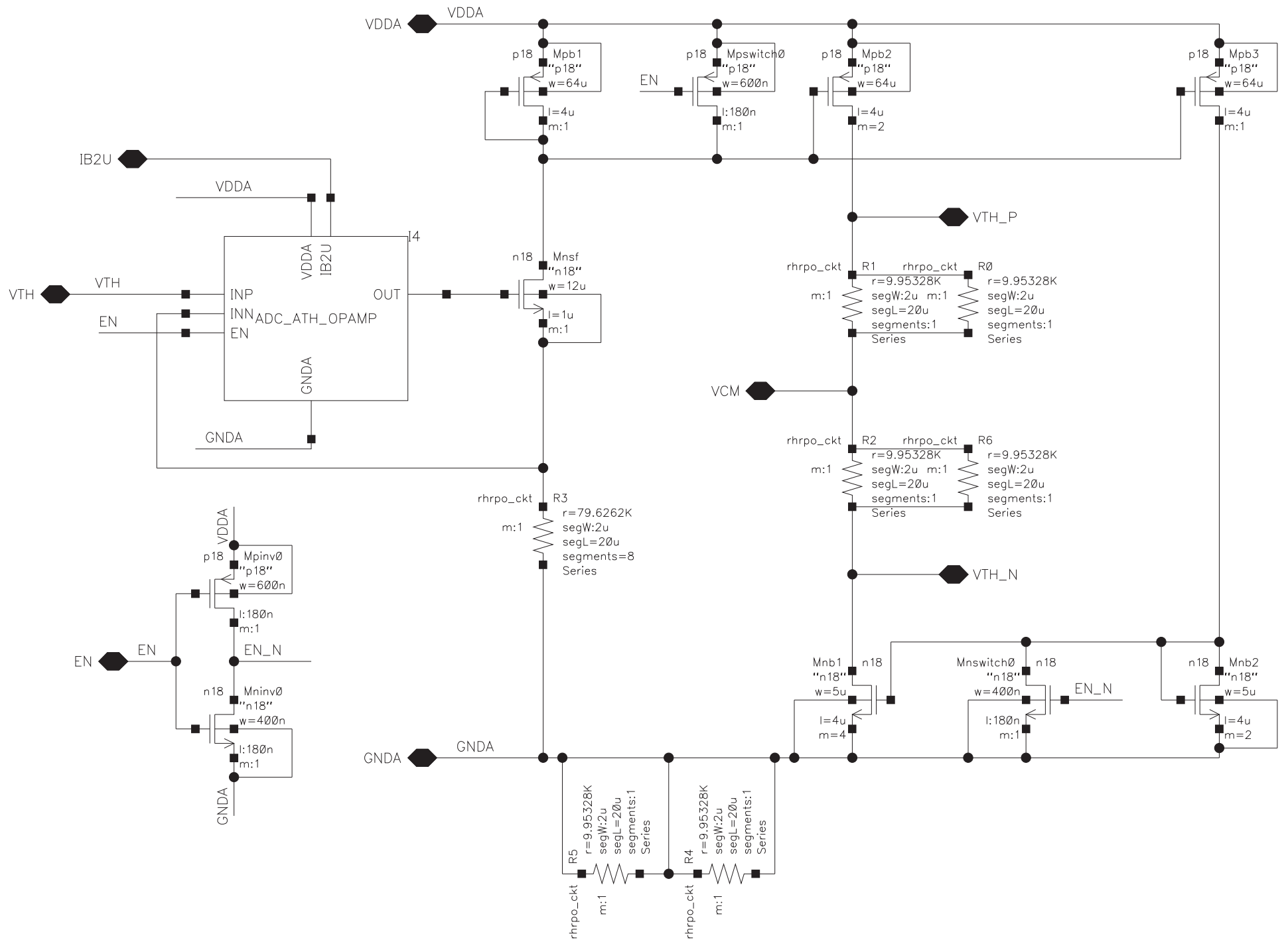


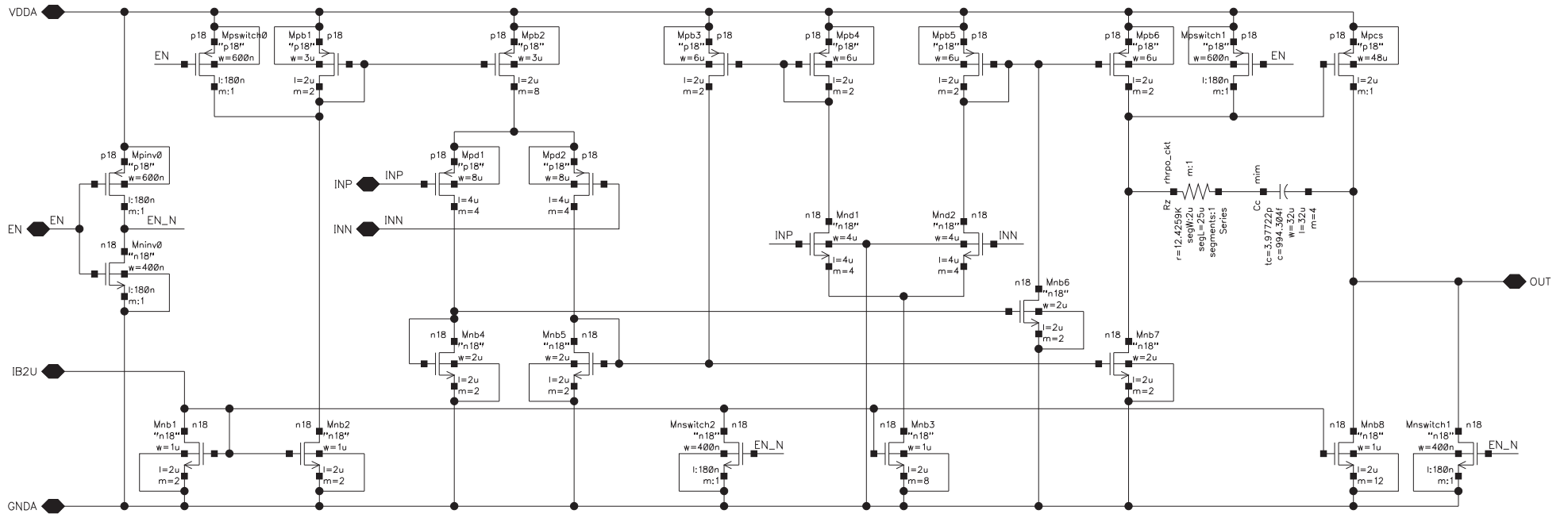
SPL\_TOP  
2 Aug 07  
Squall Sang

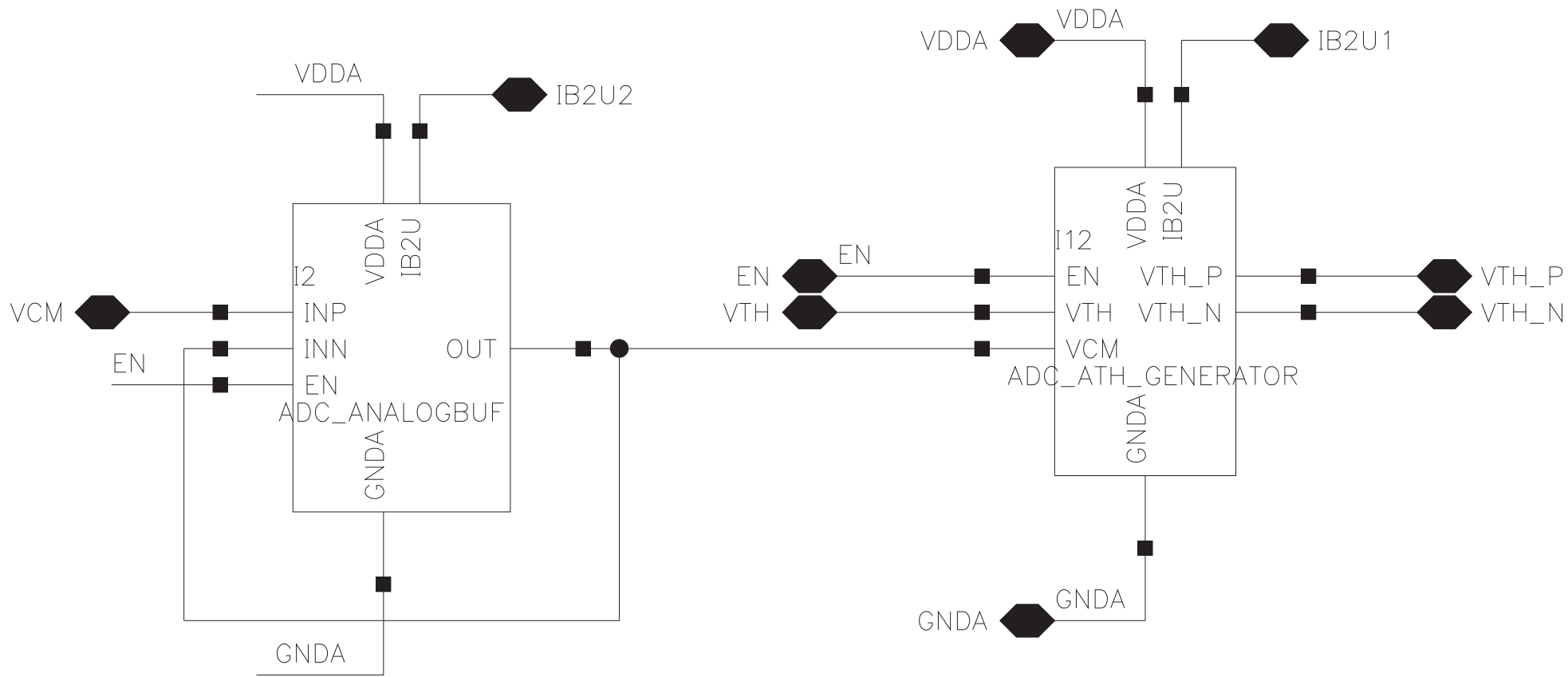


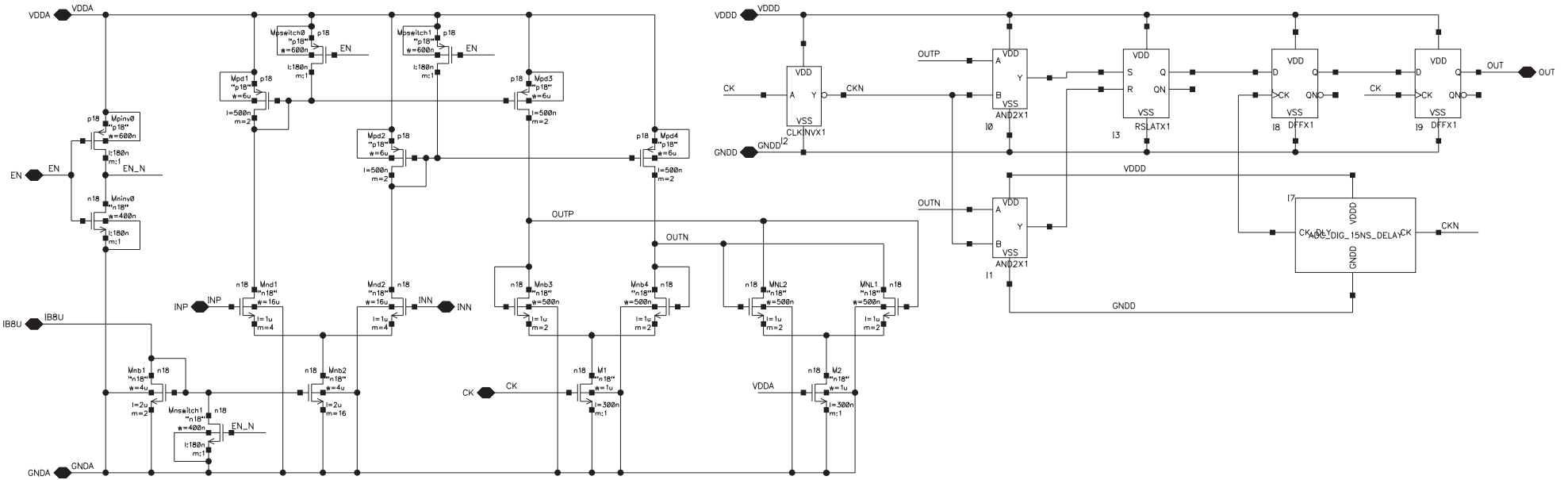




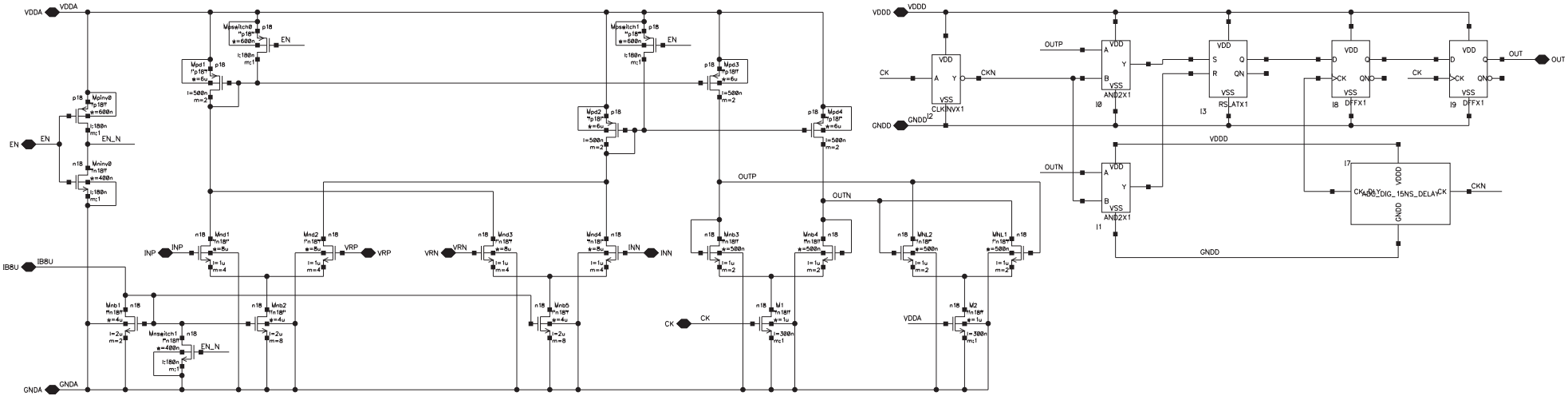




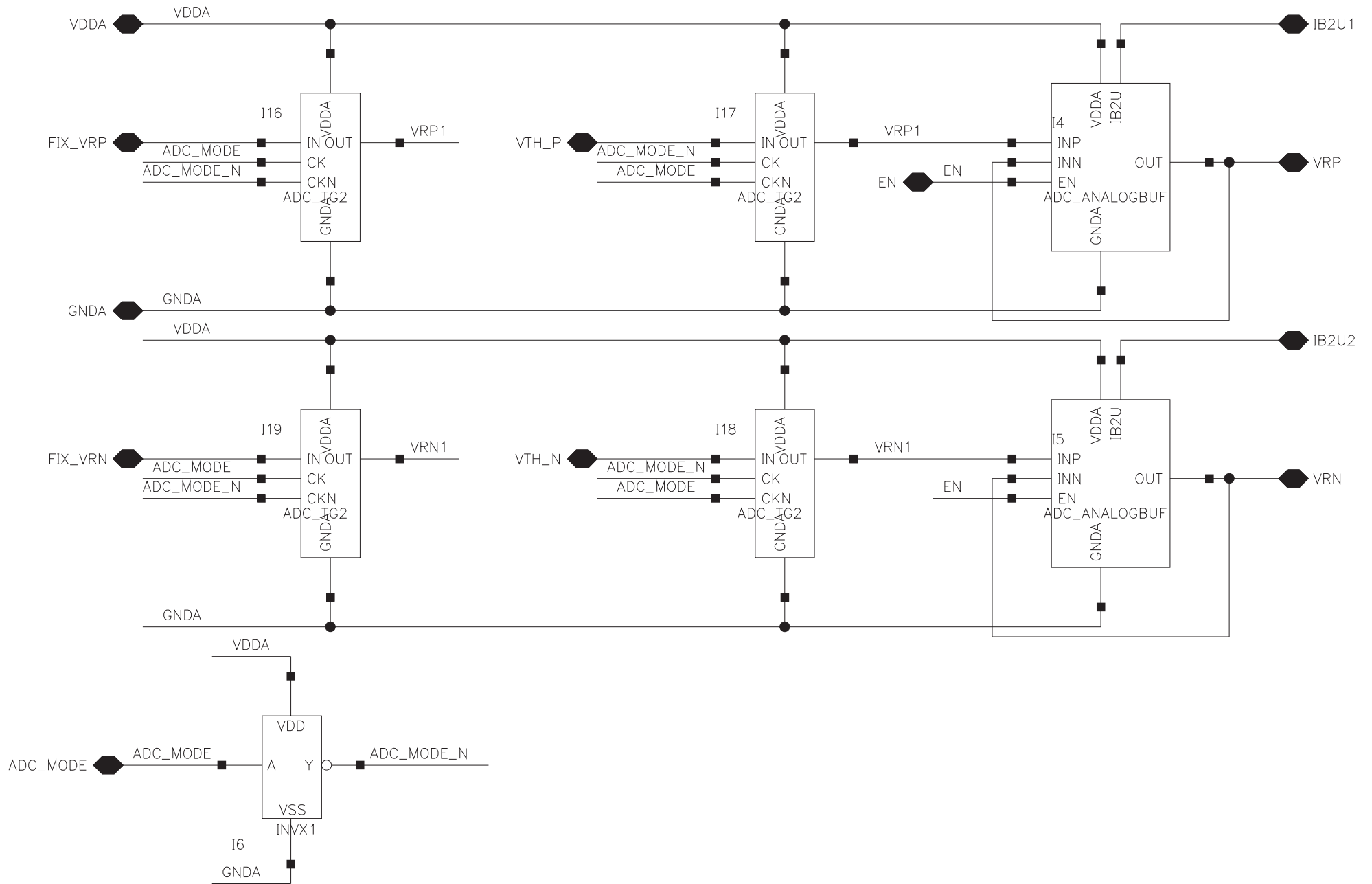




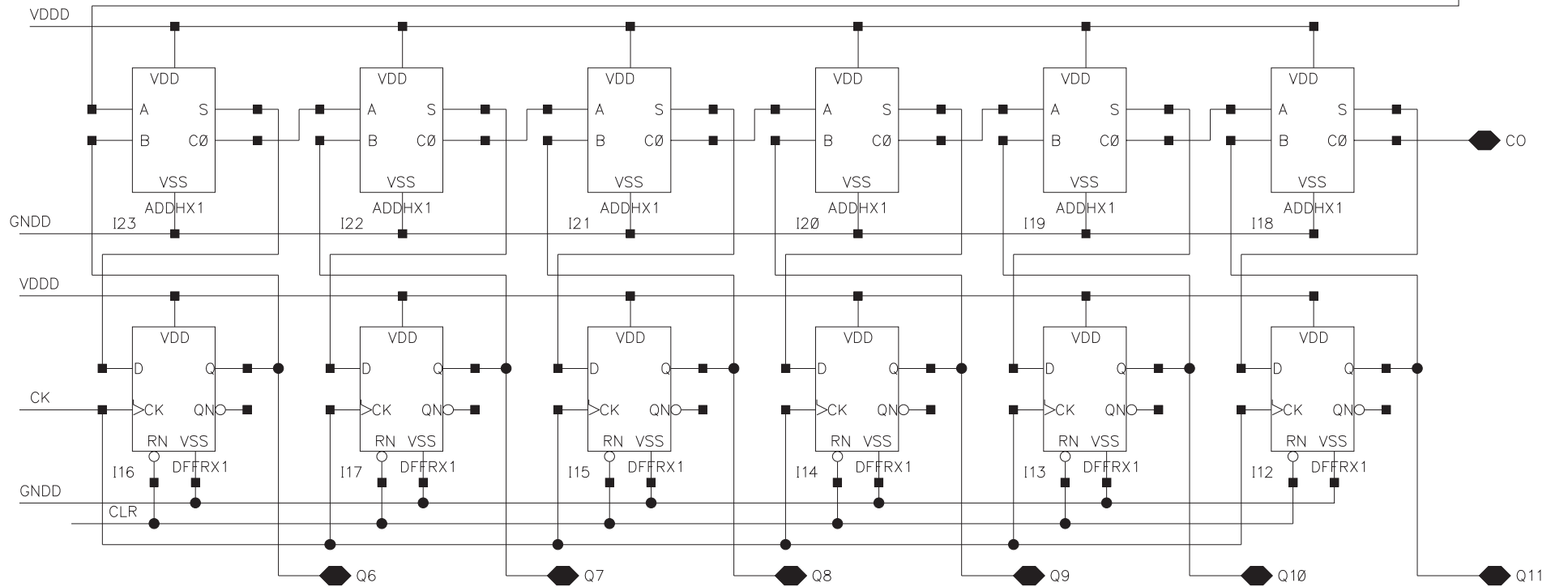
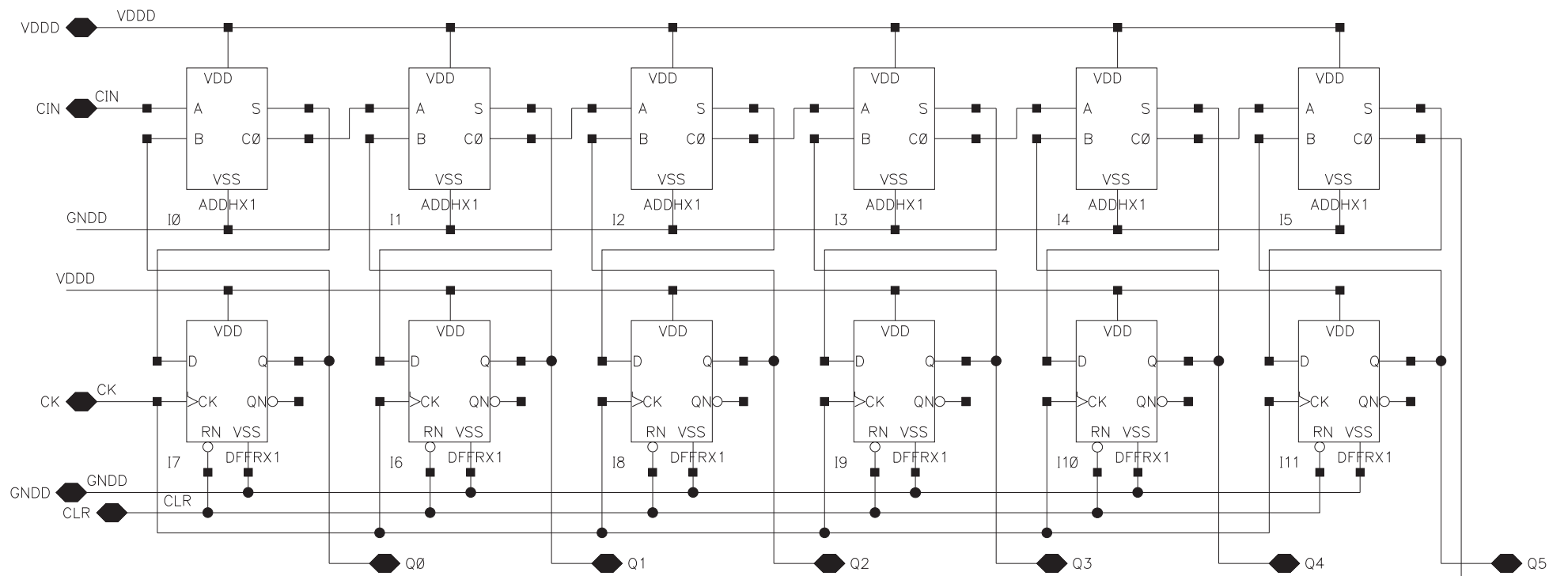


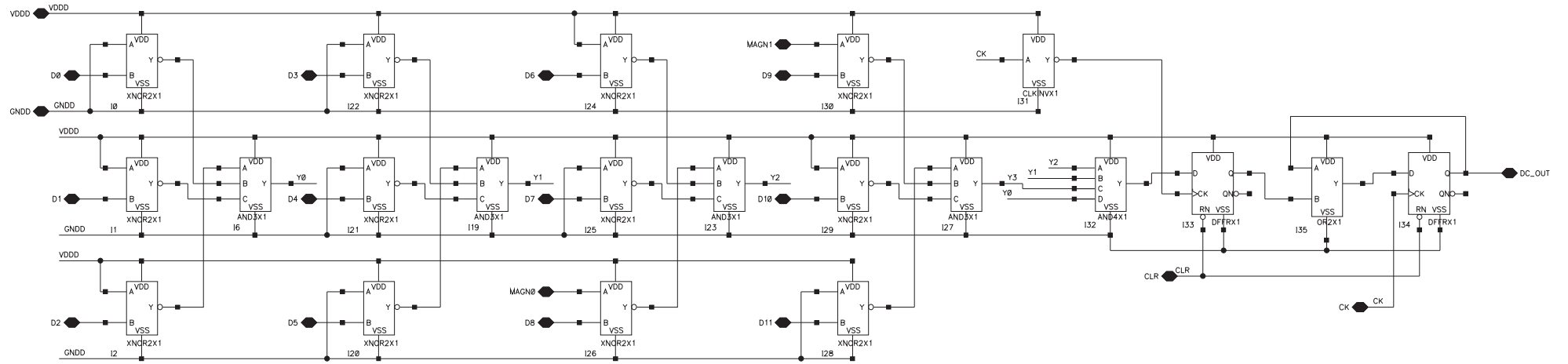




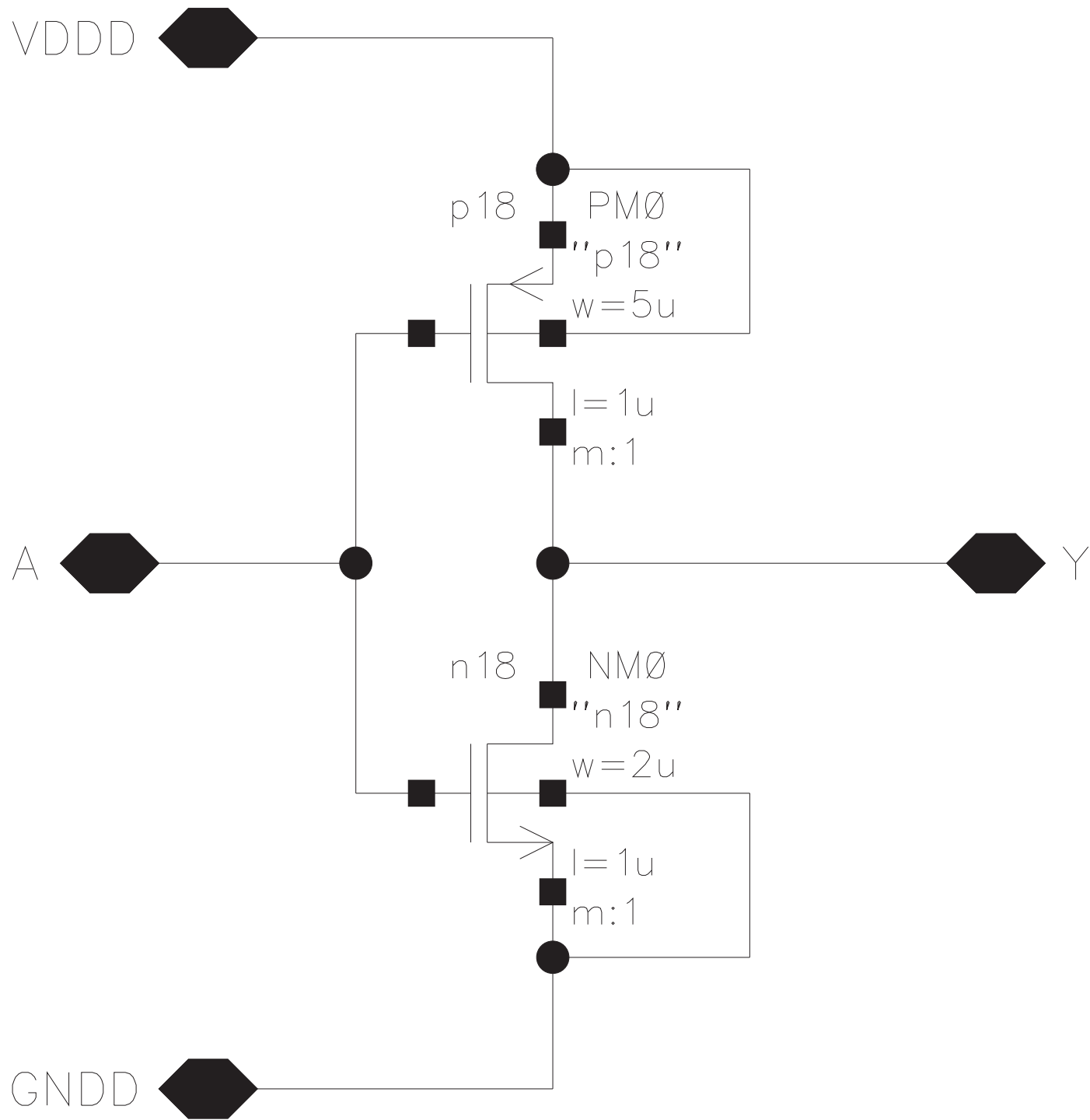




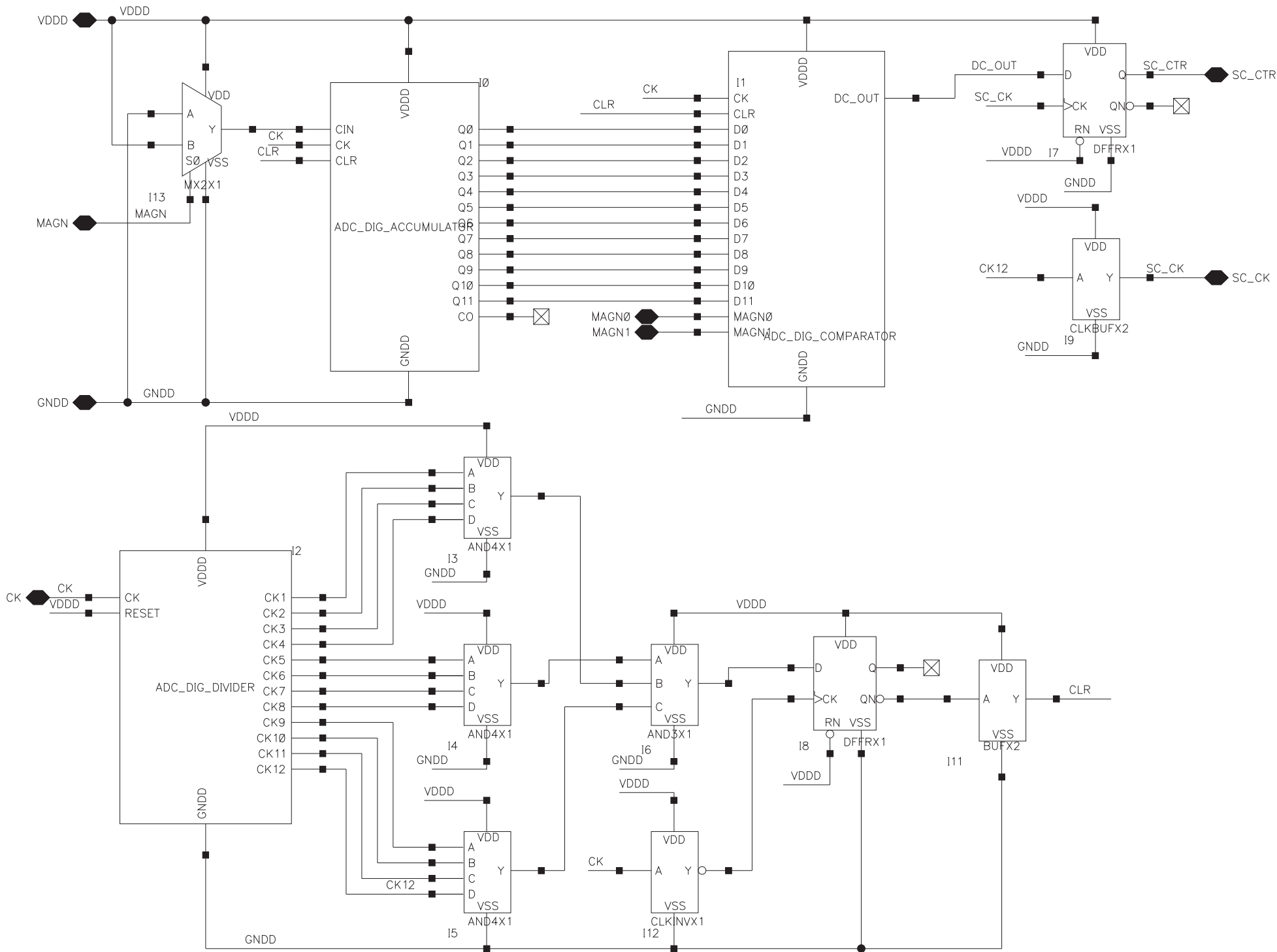


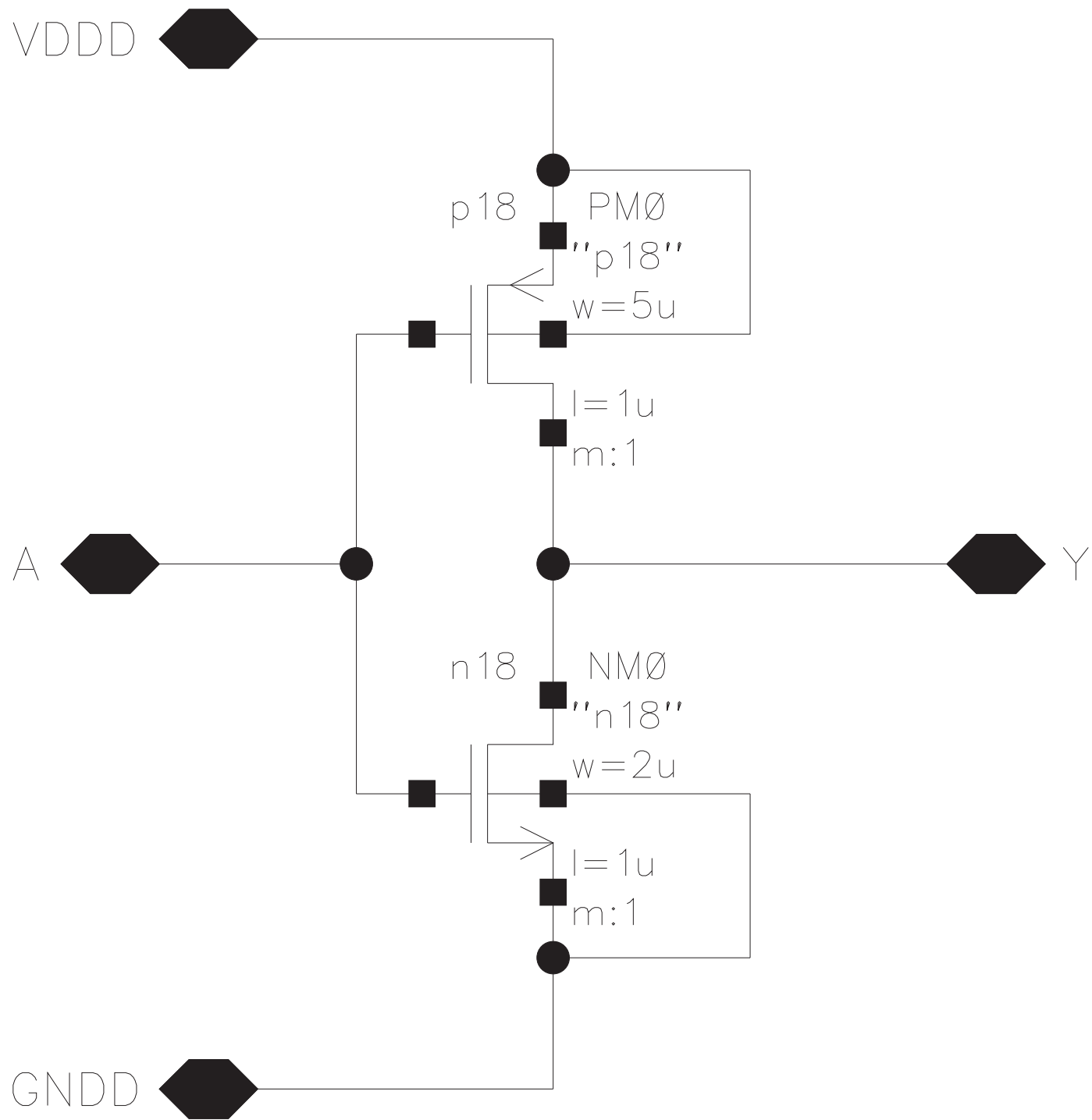


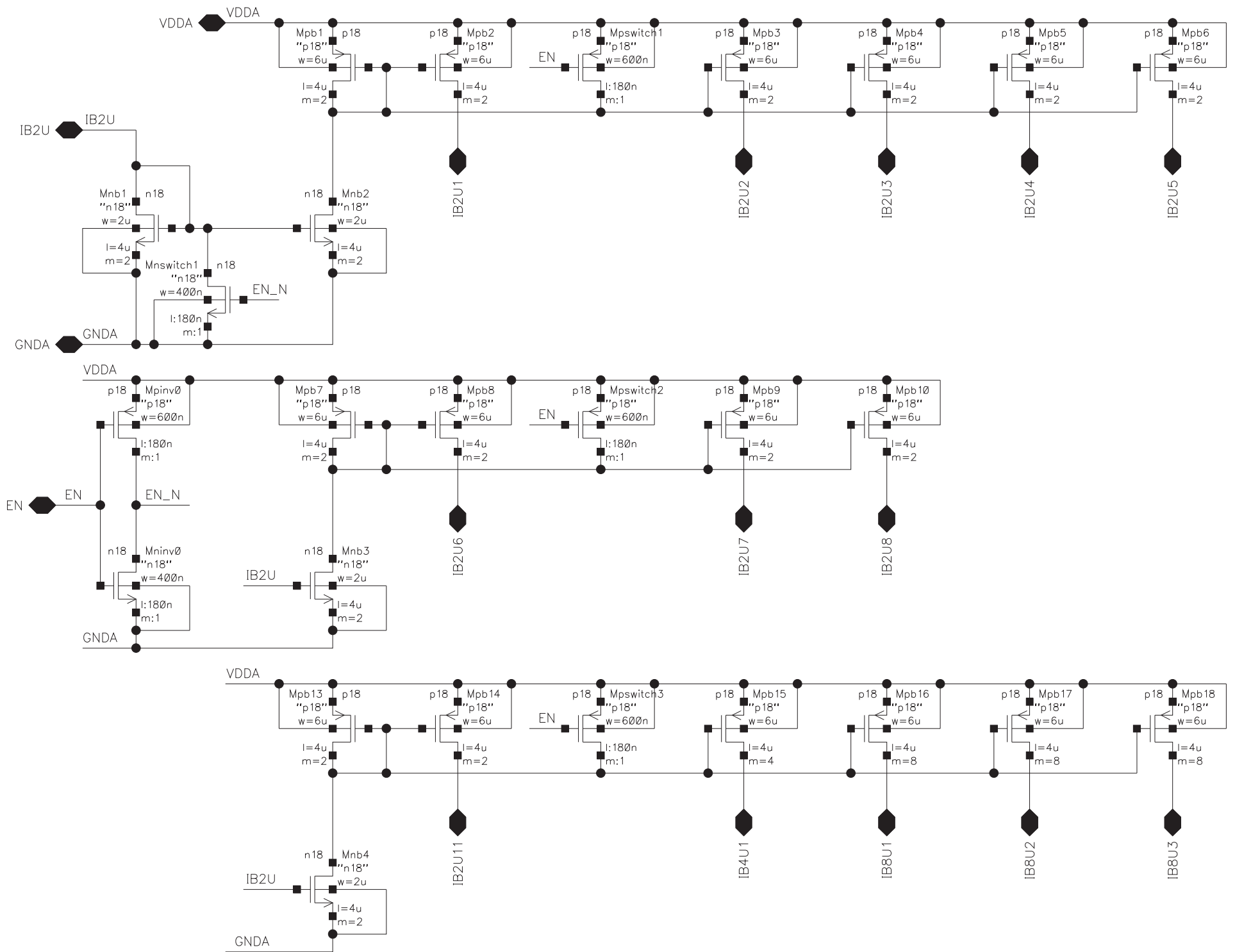


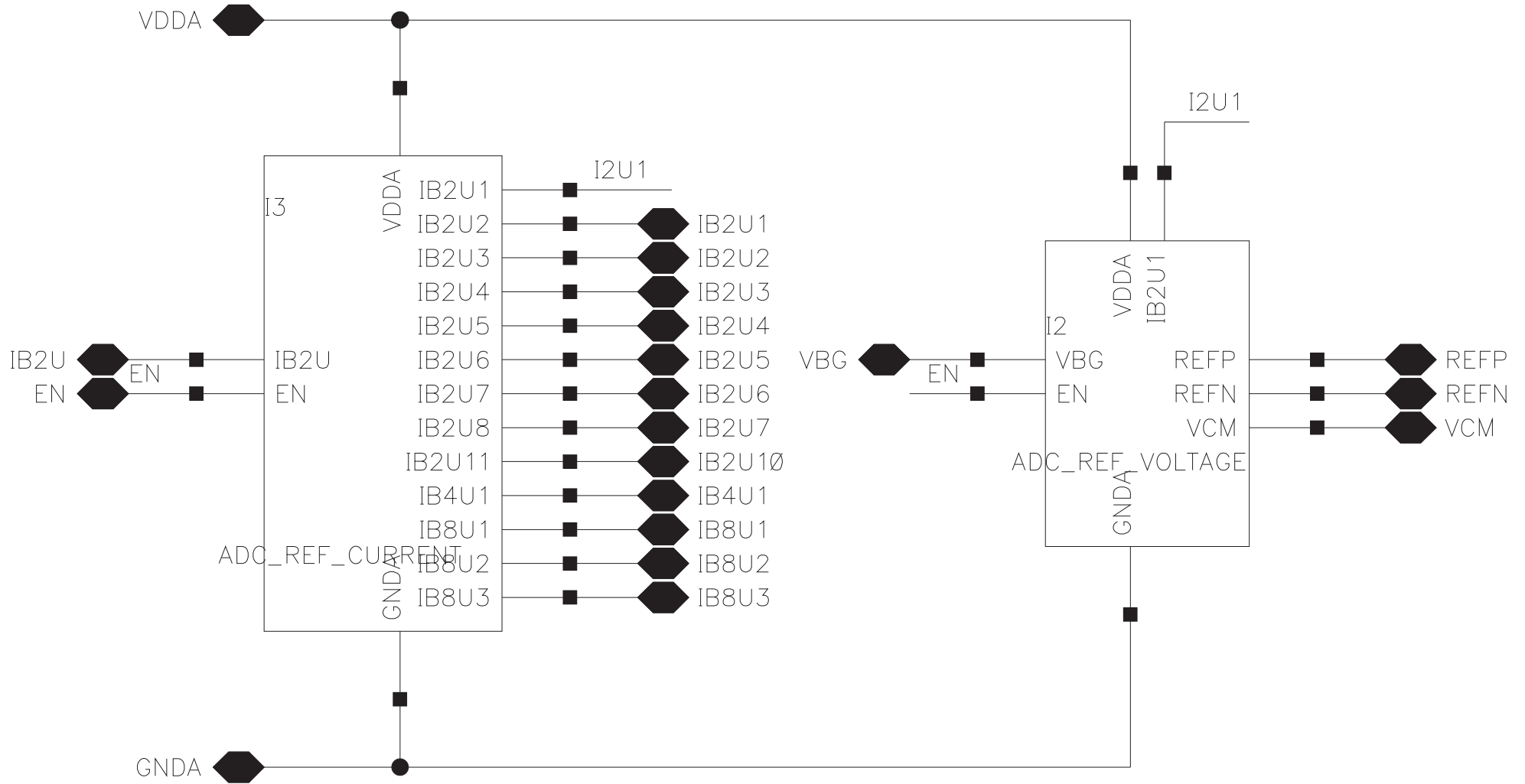


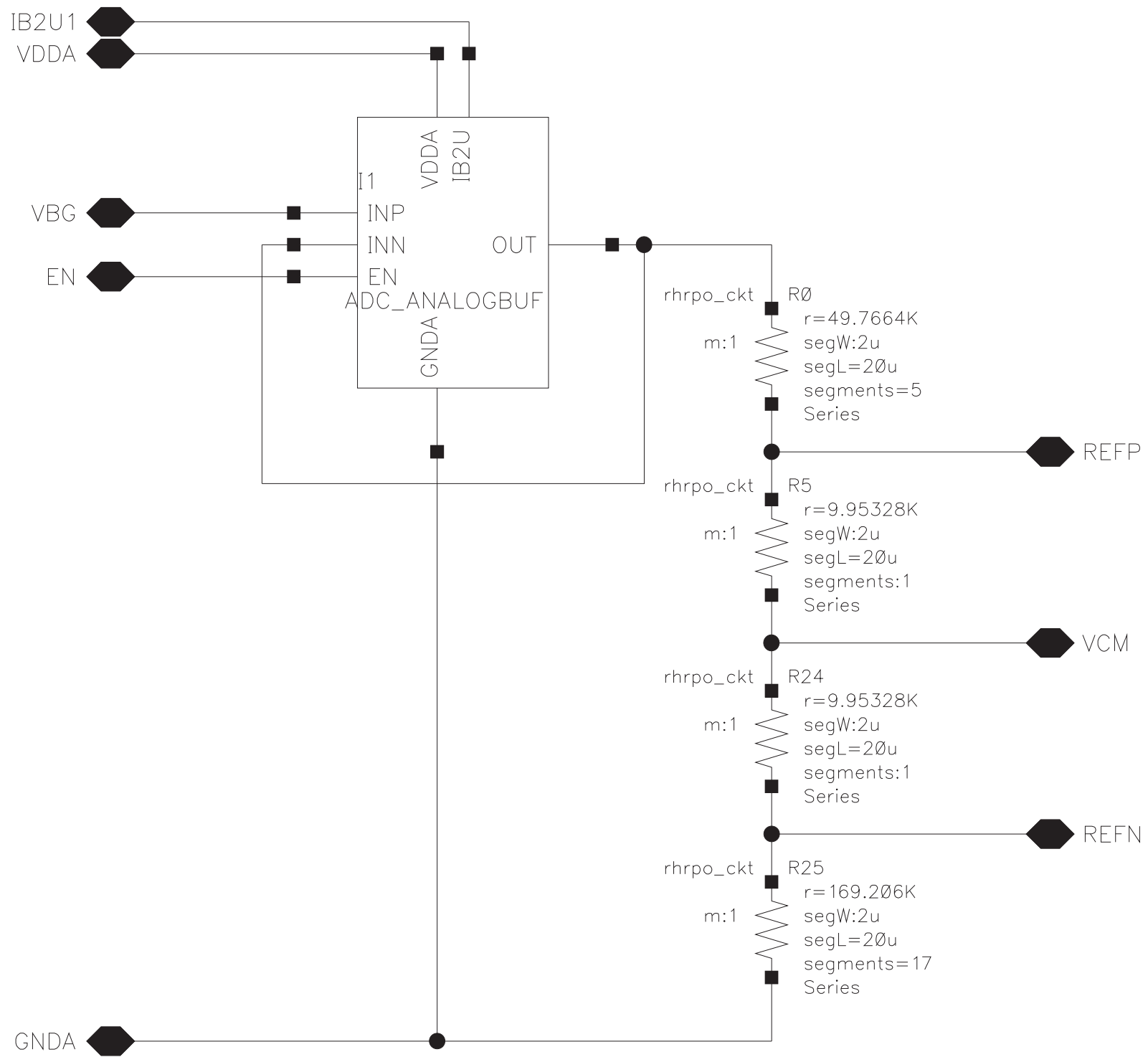


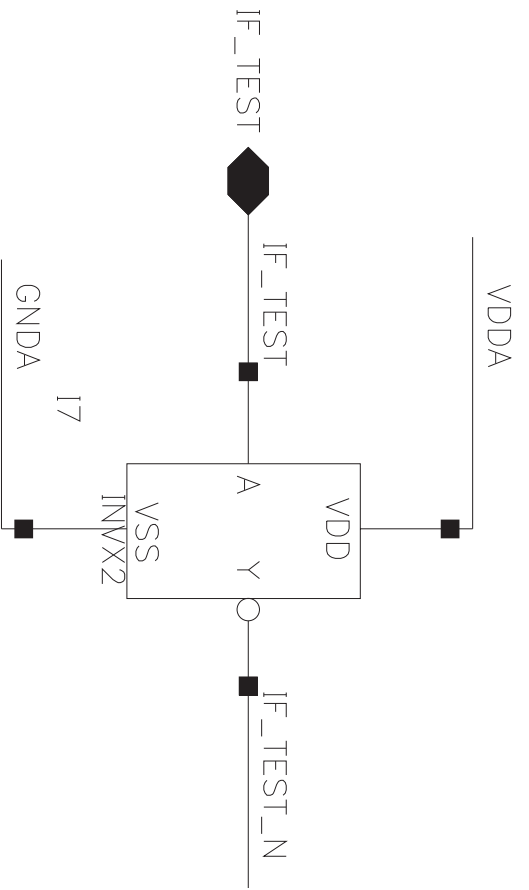
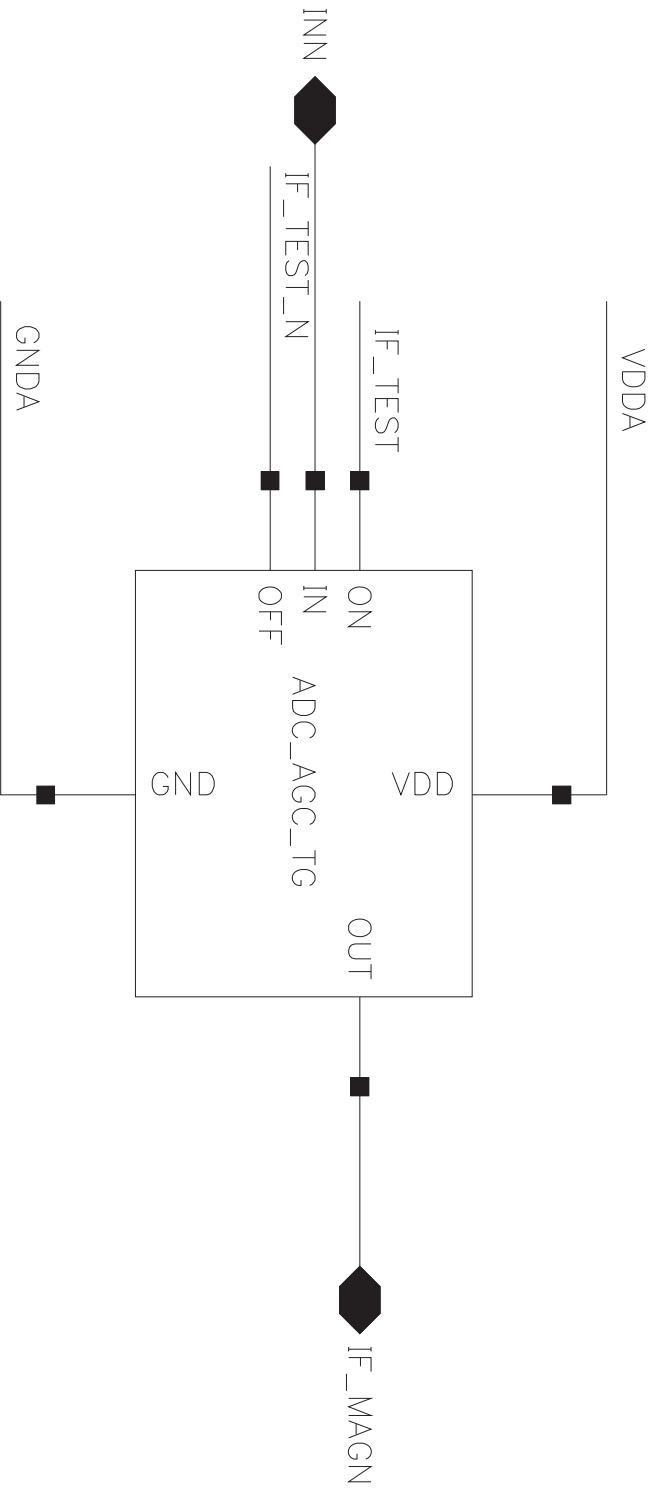
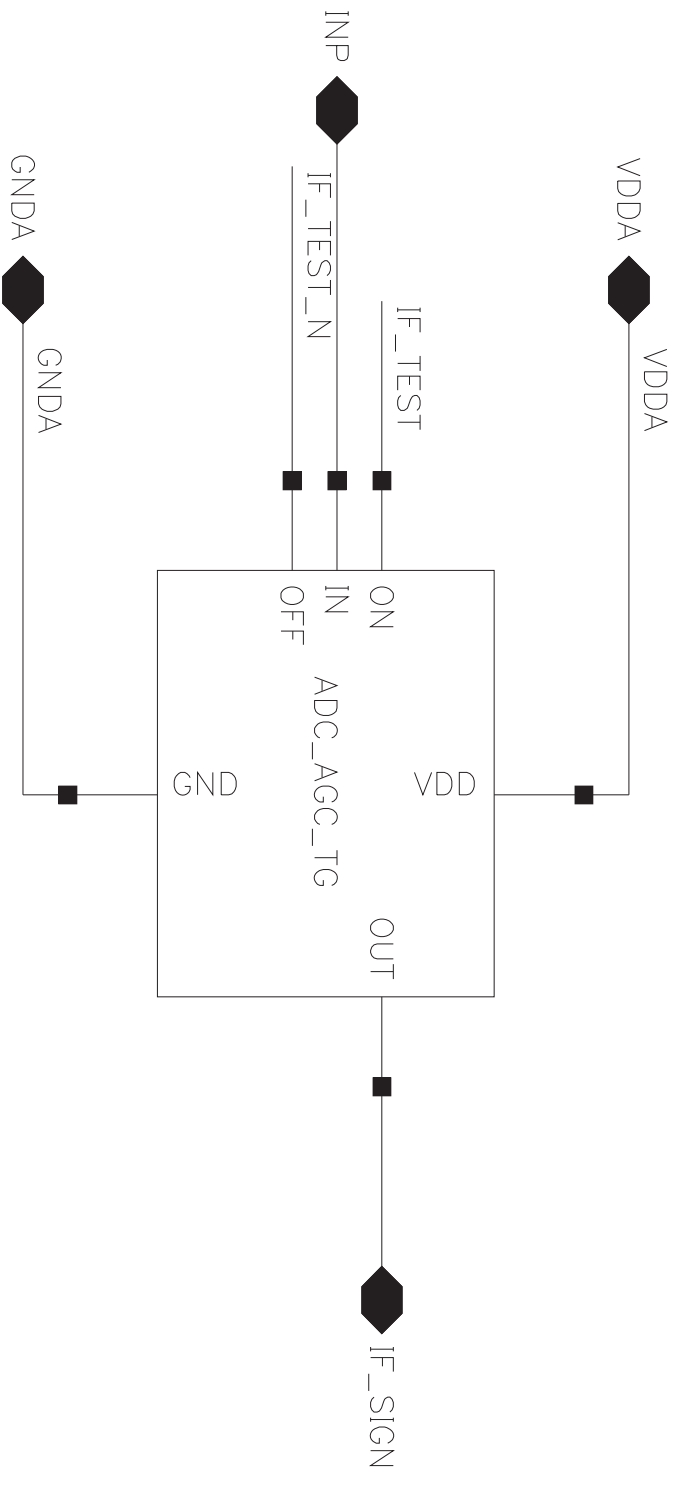


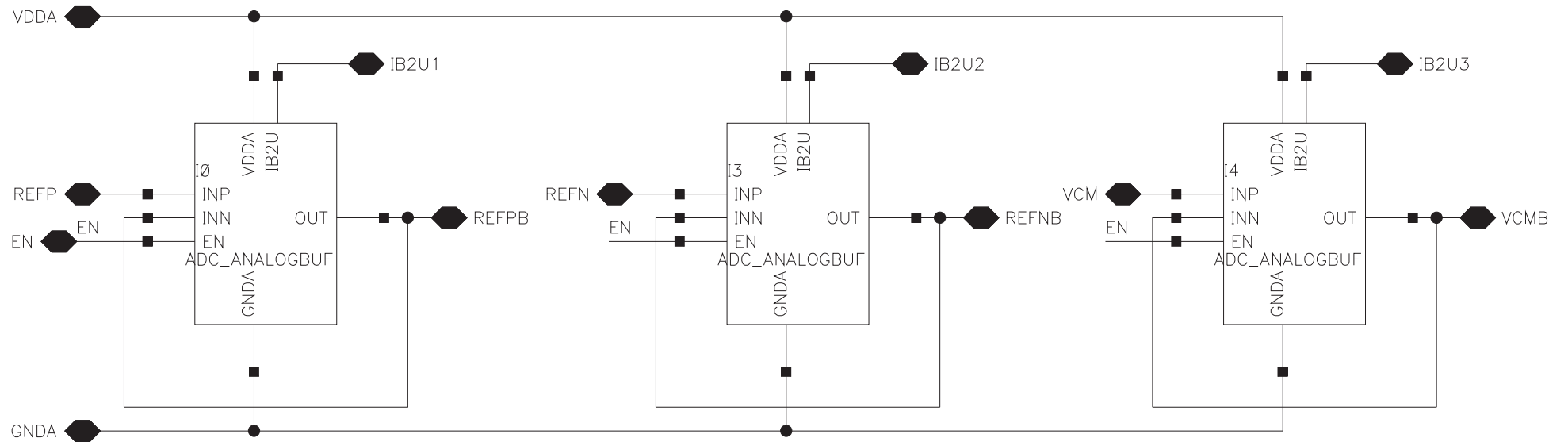


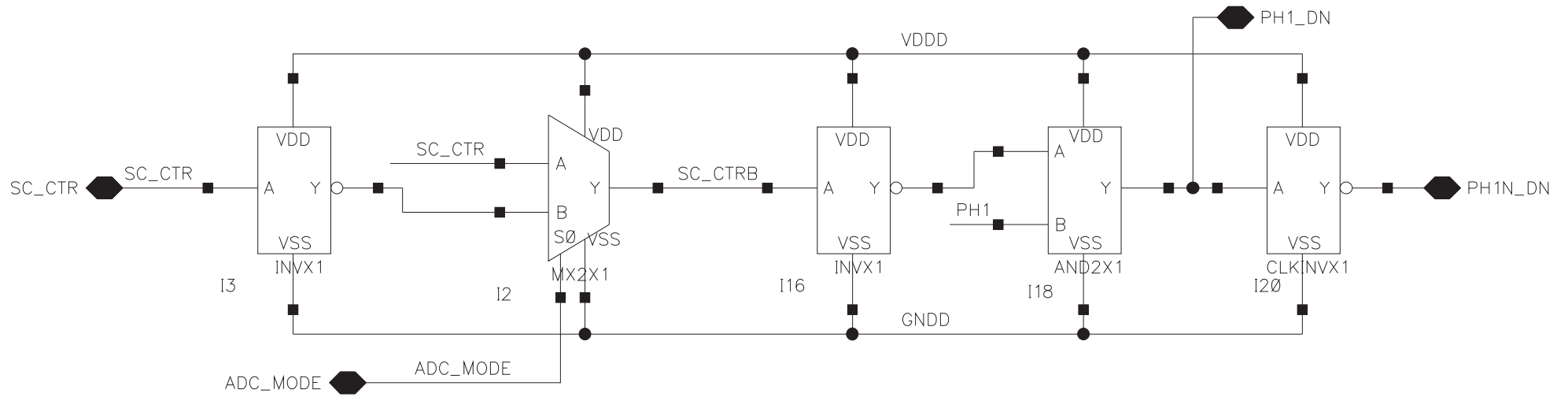
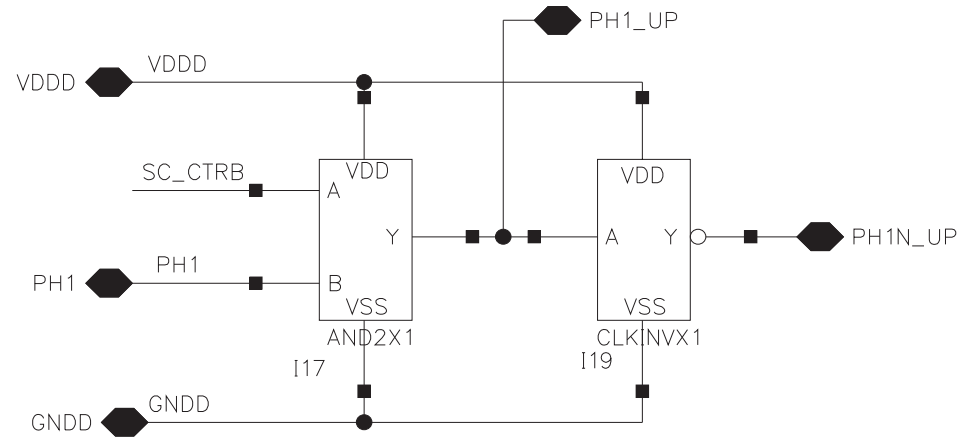




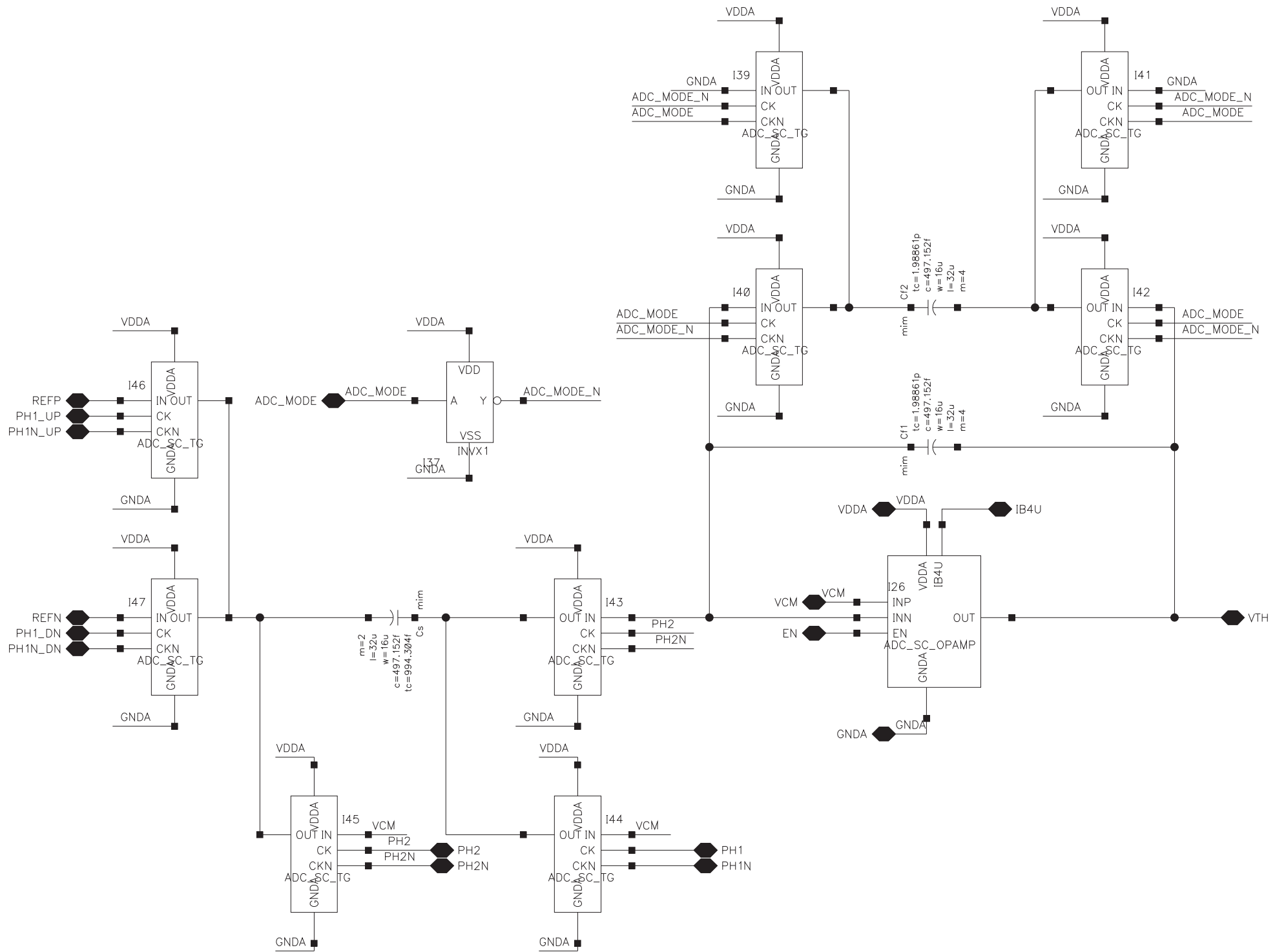


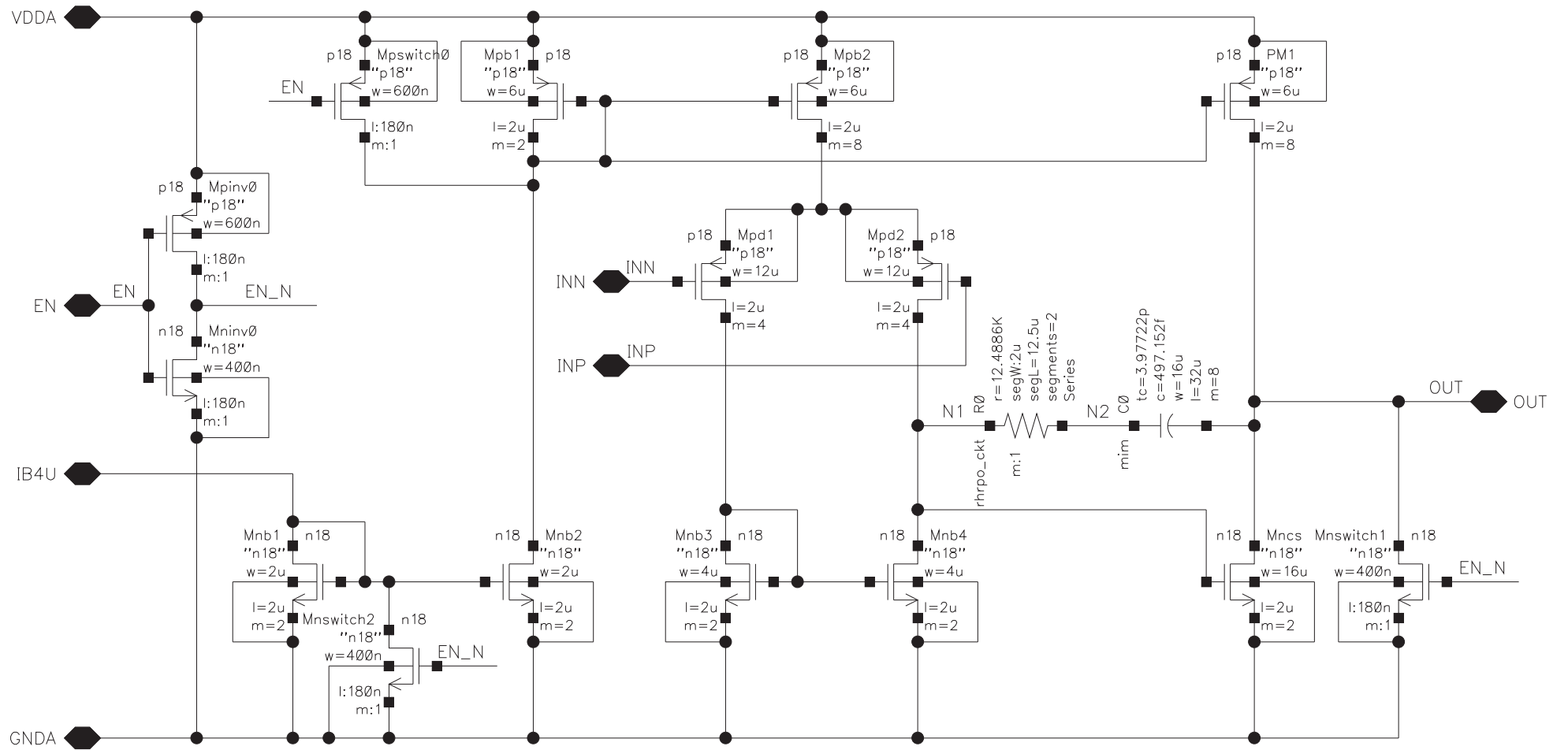


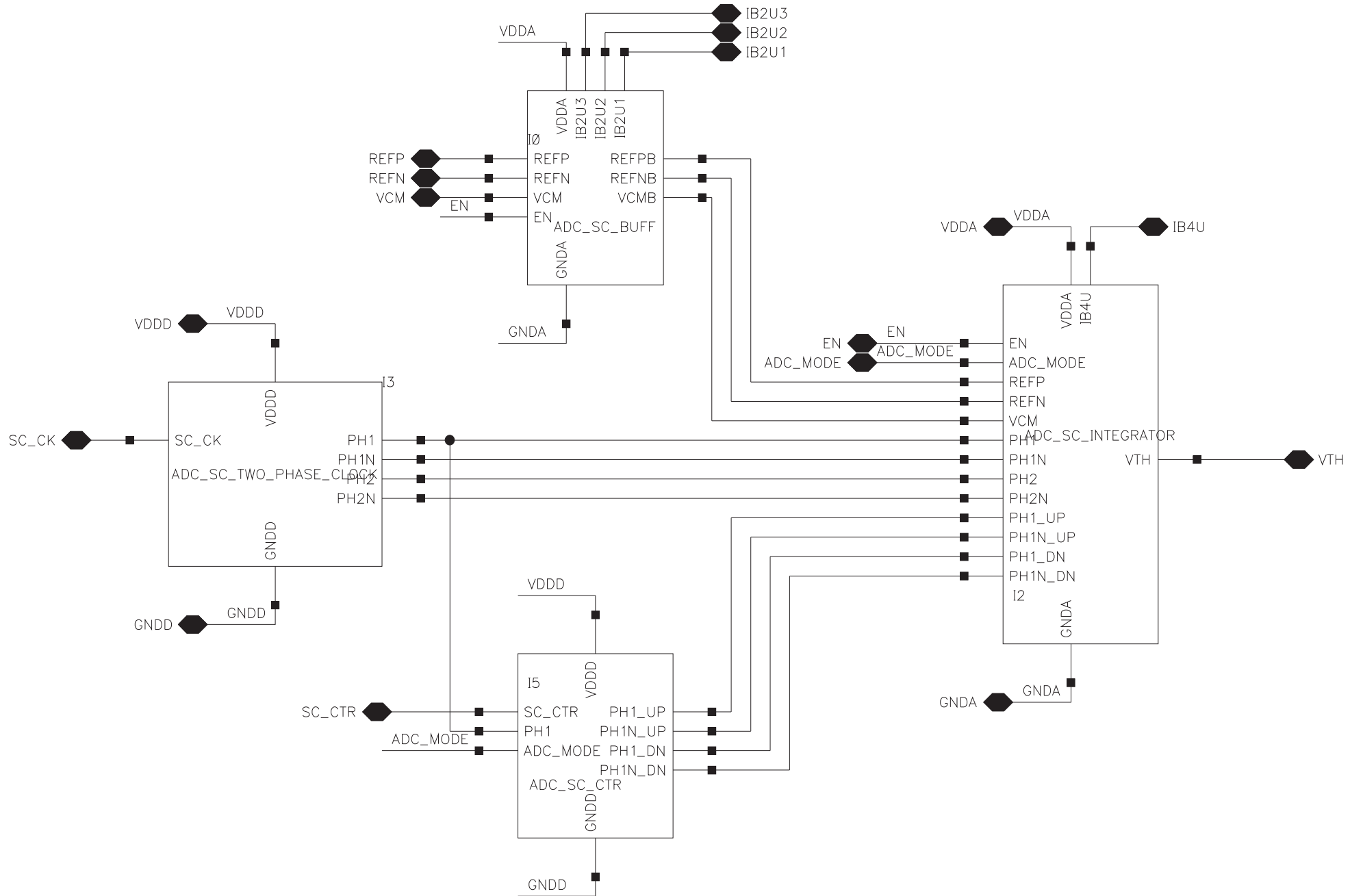


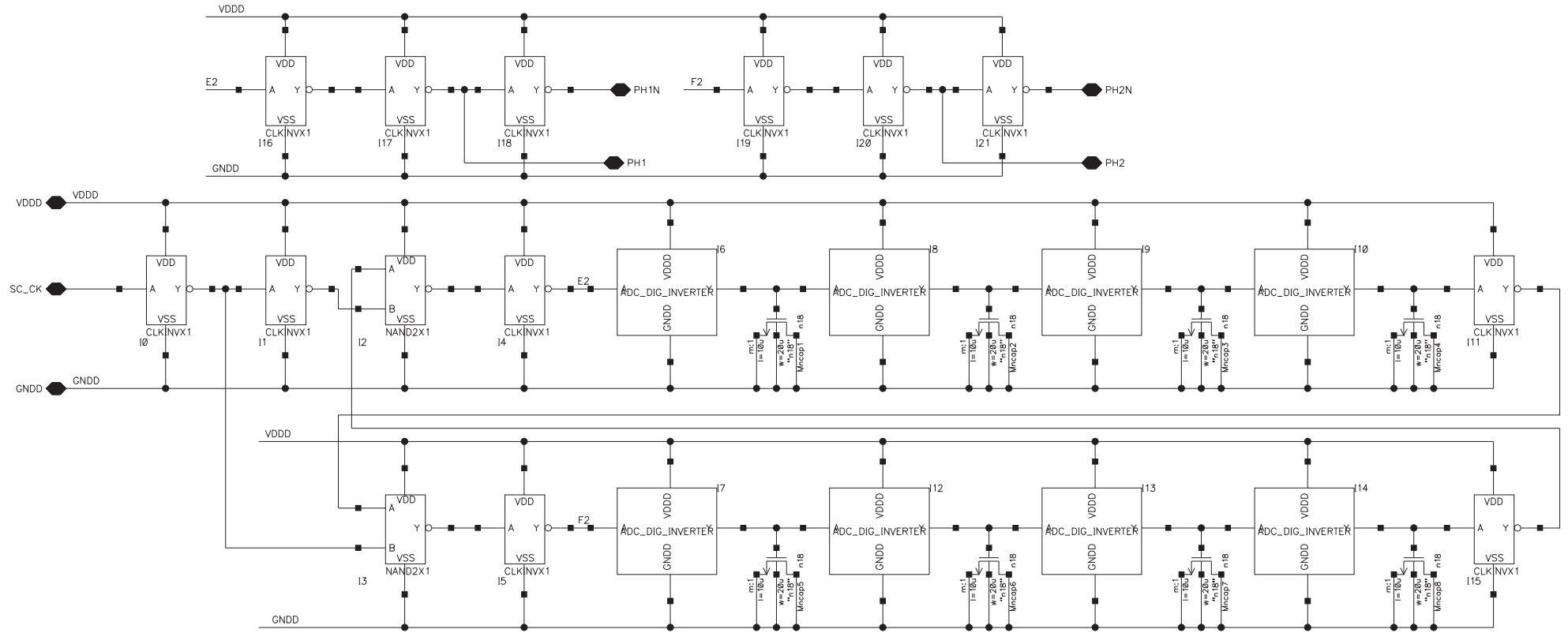


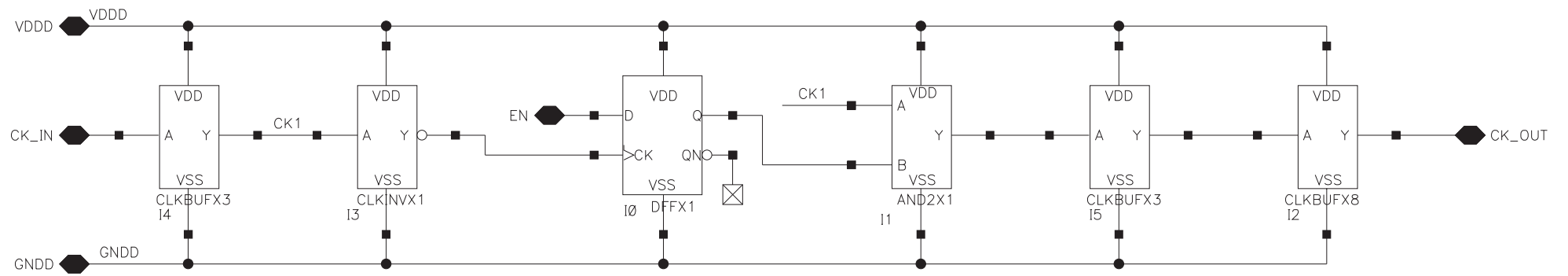




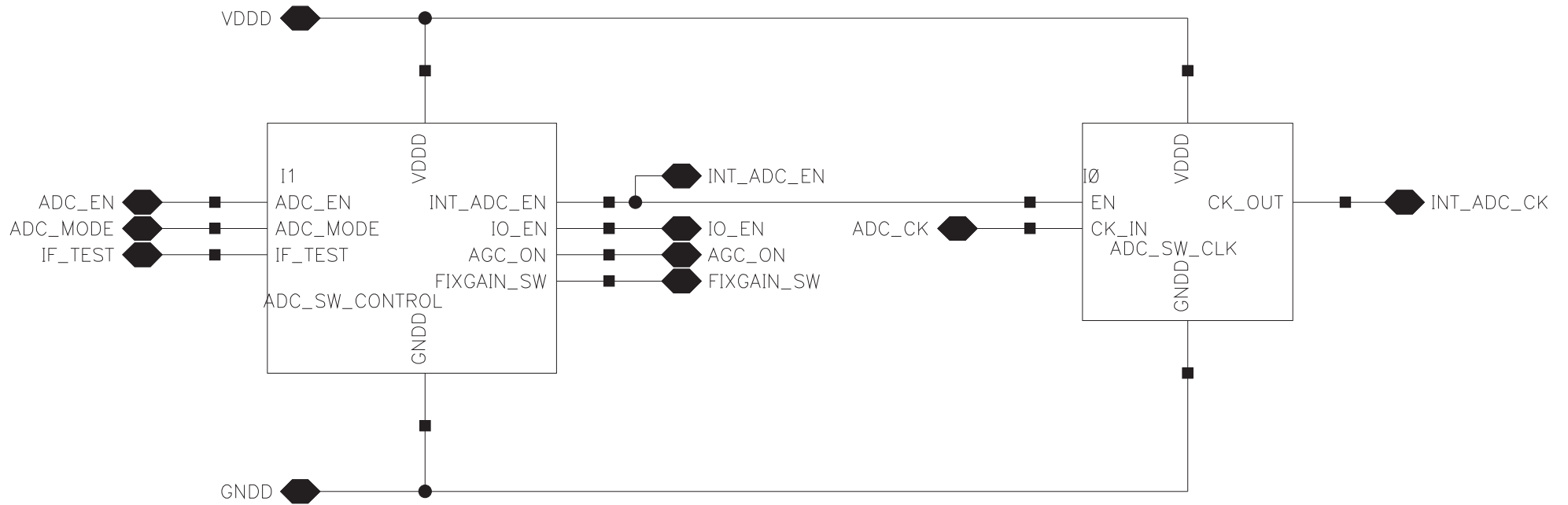


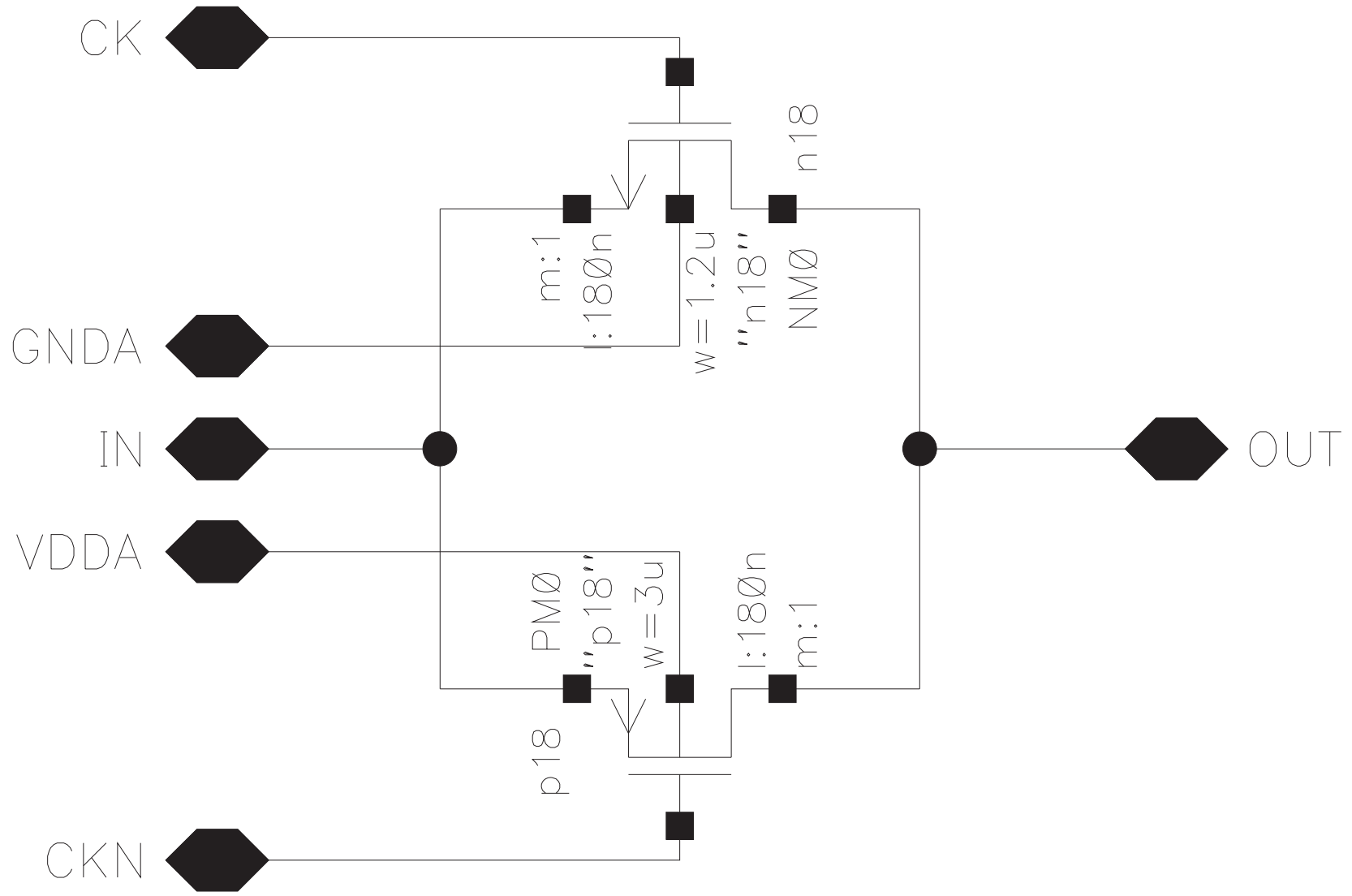




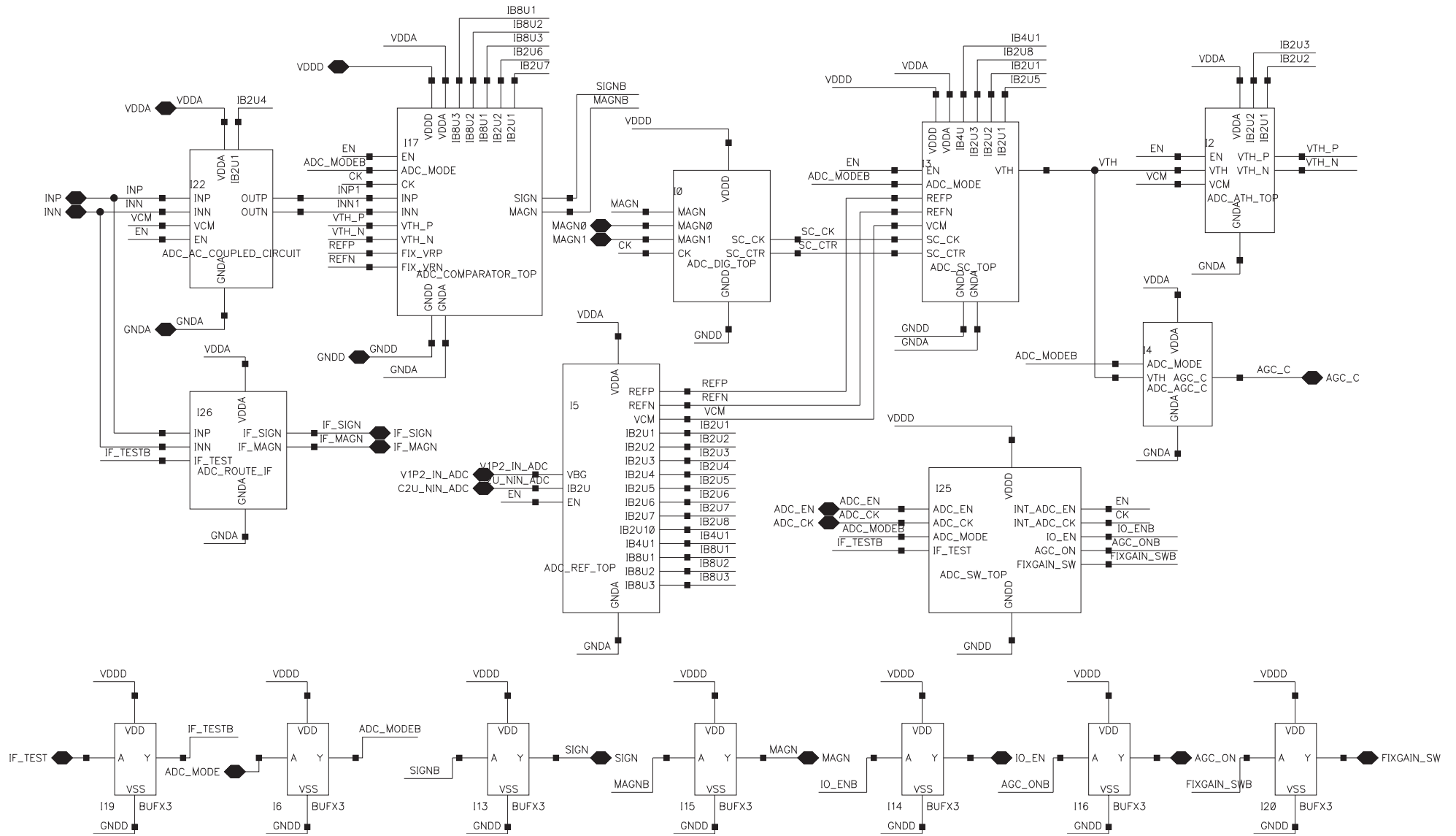


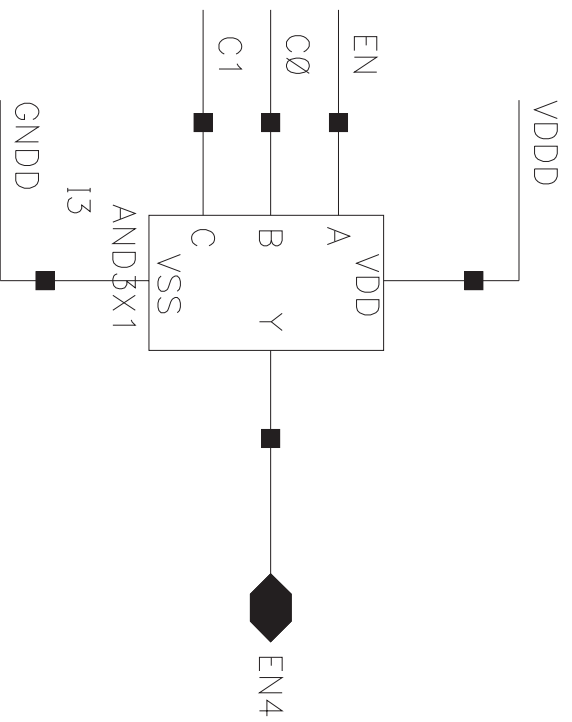
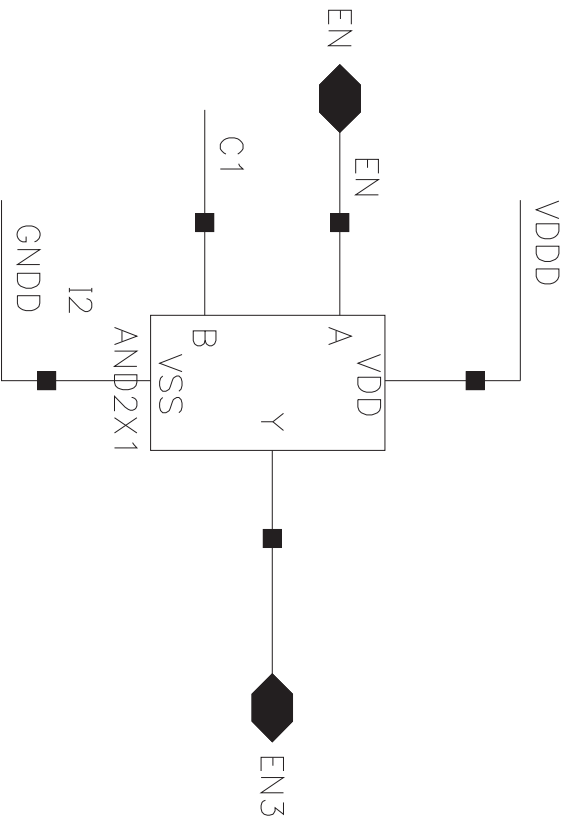
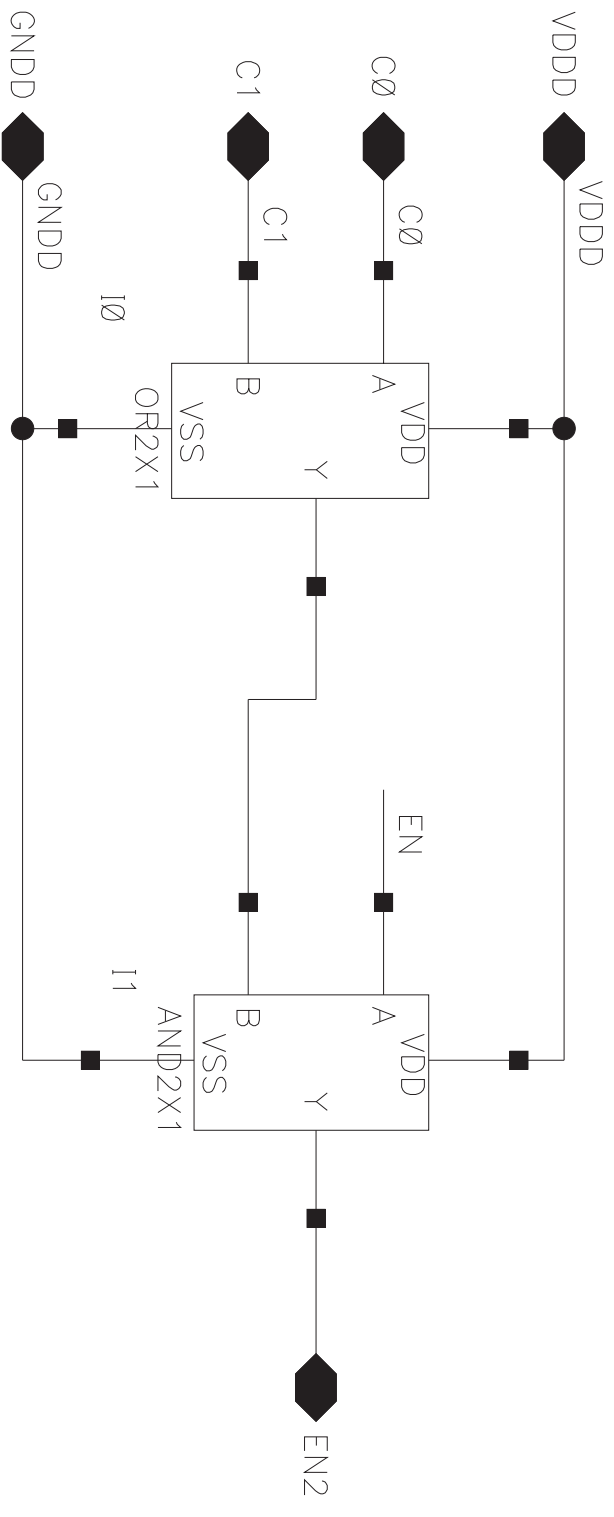


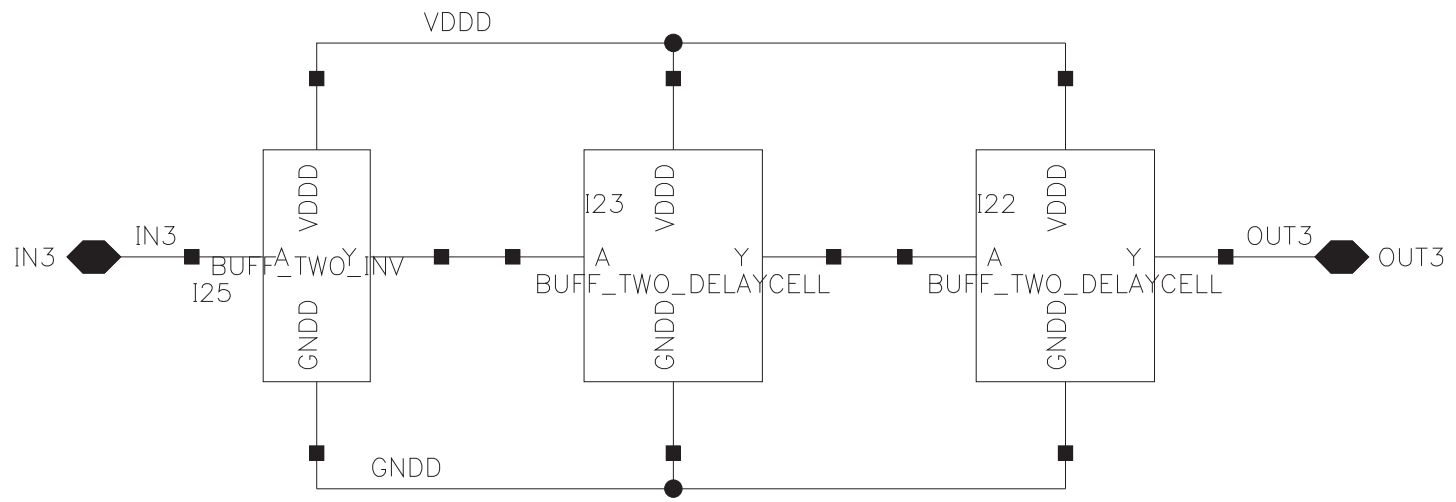
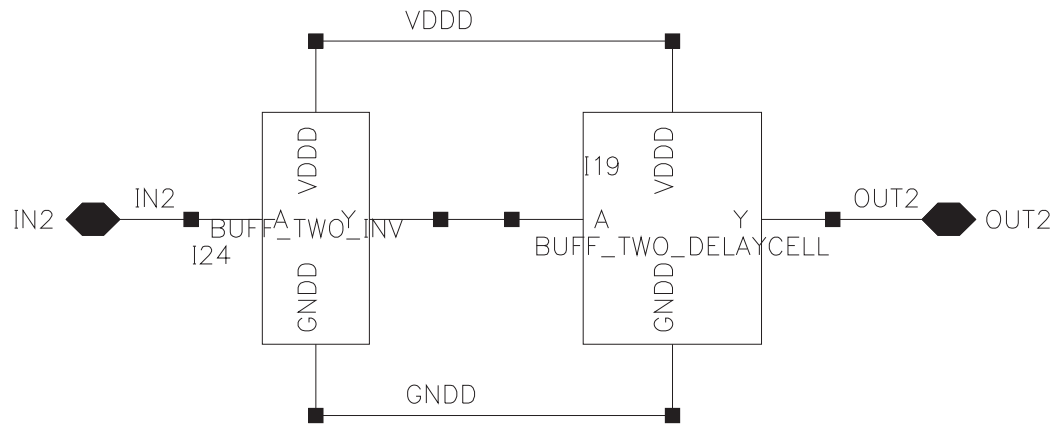
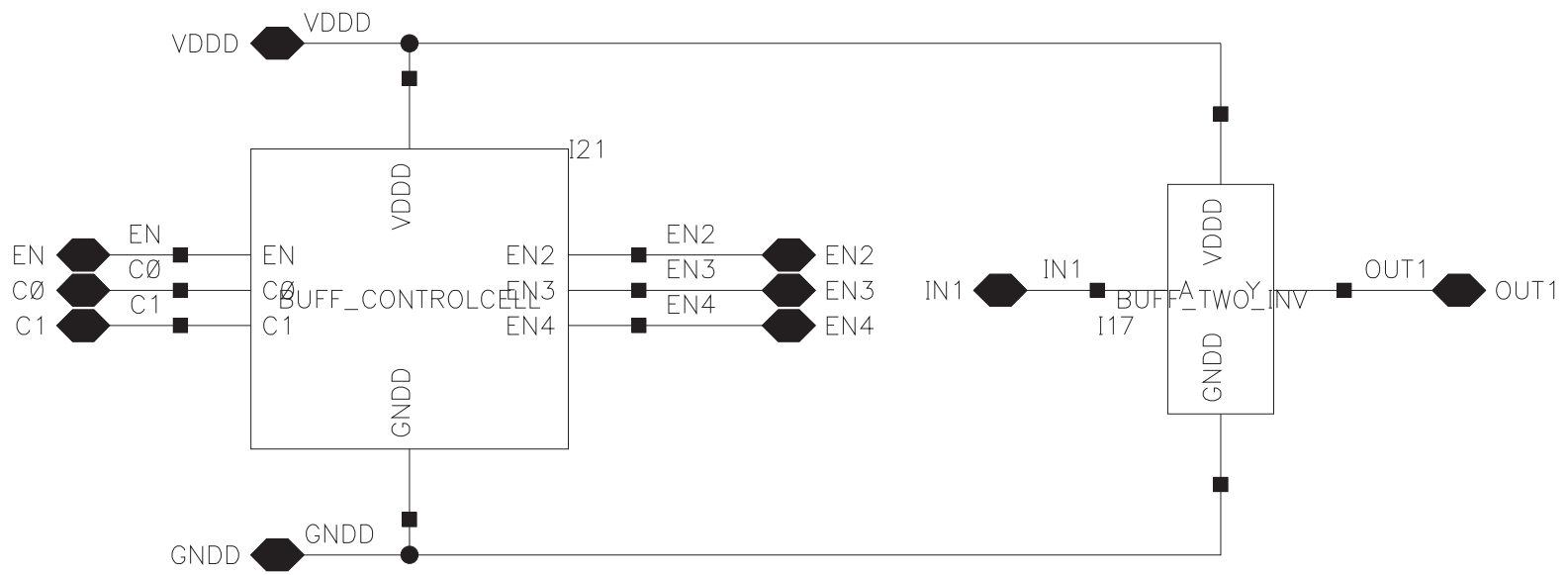


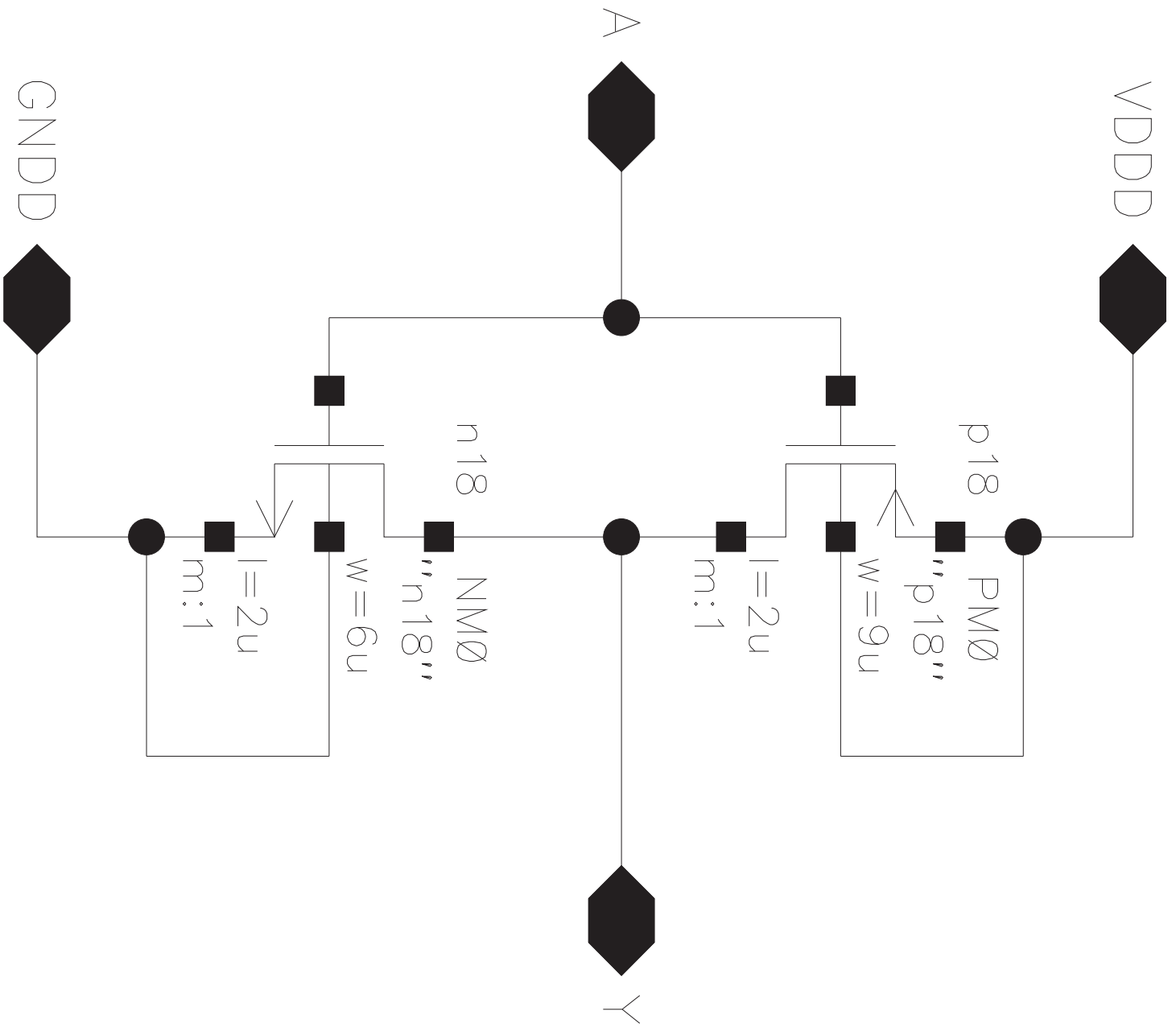


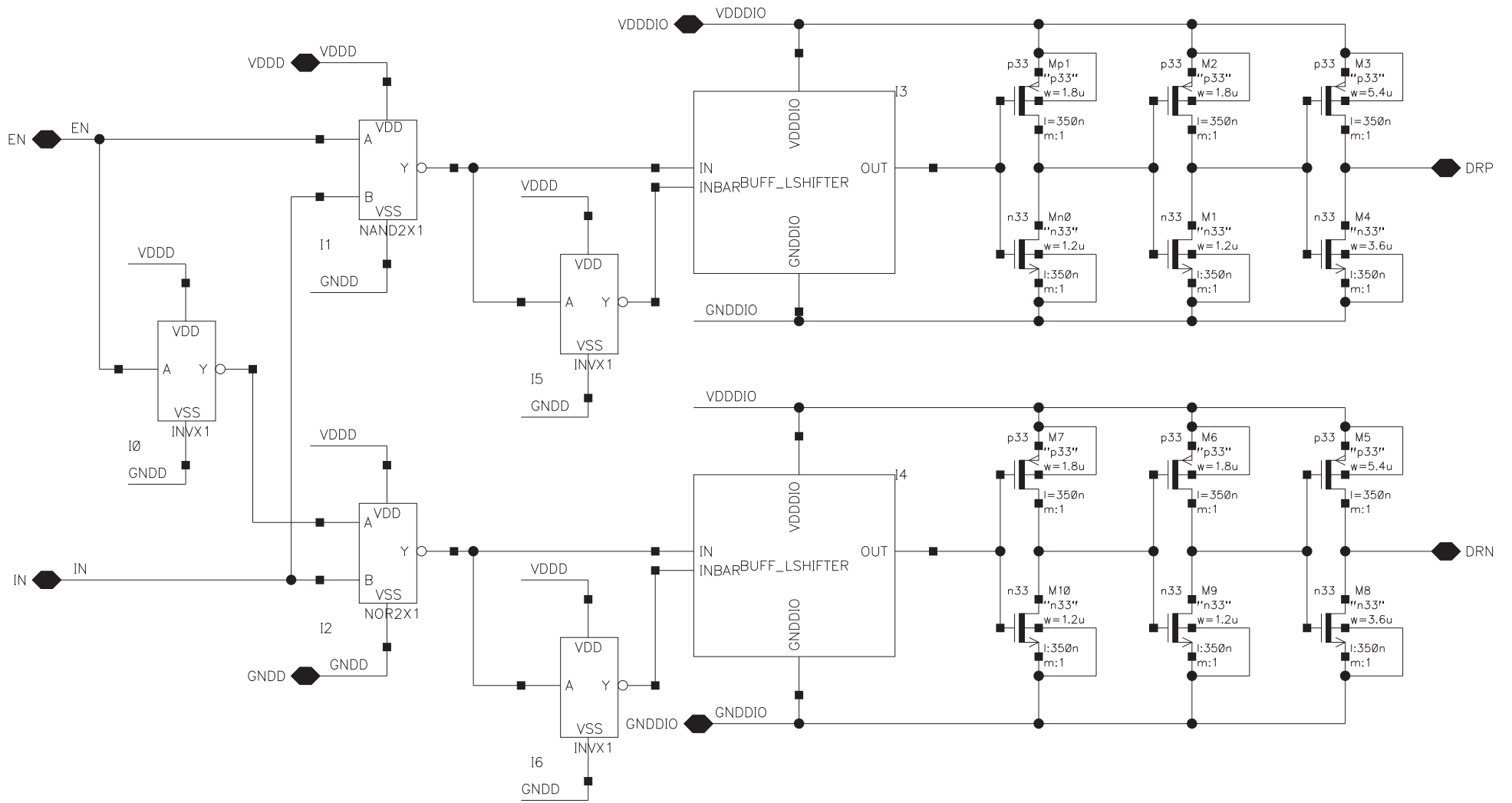


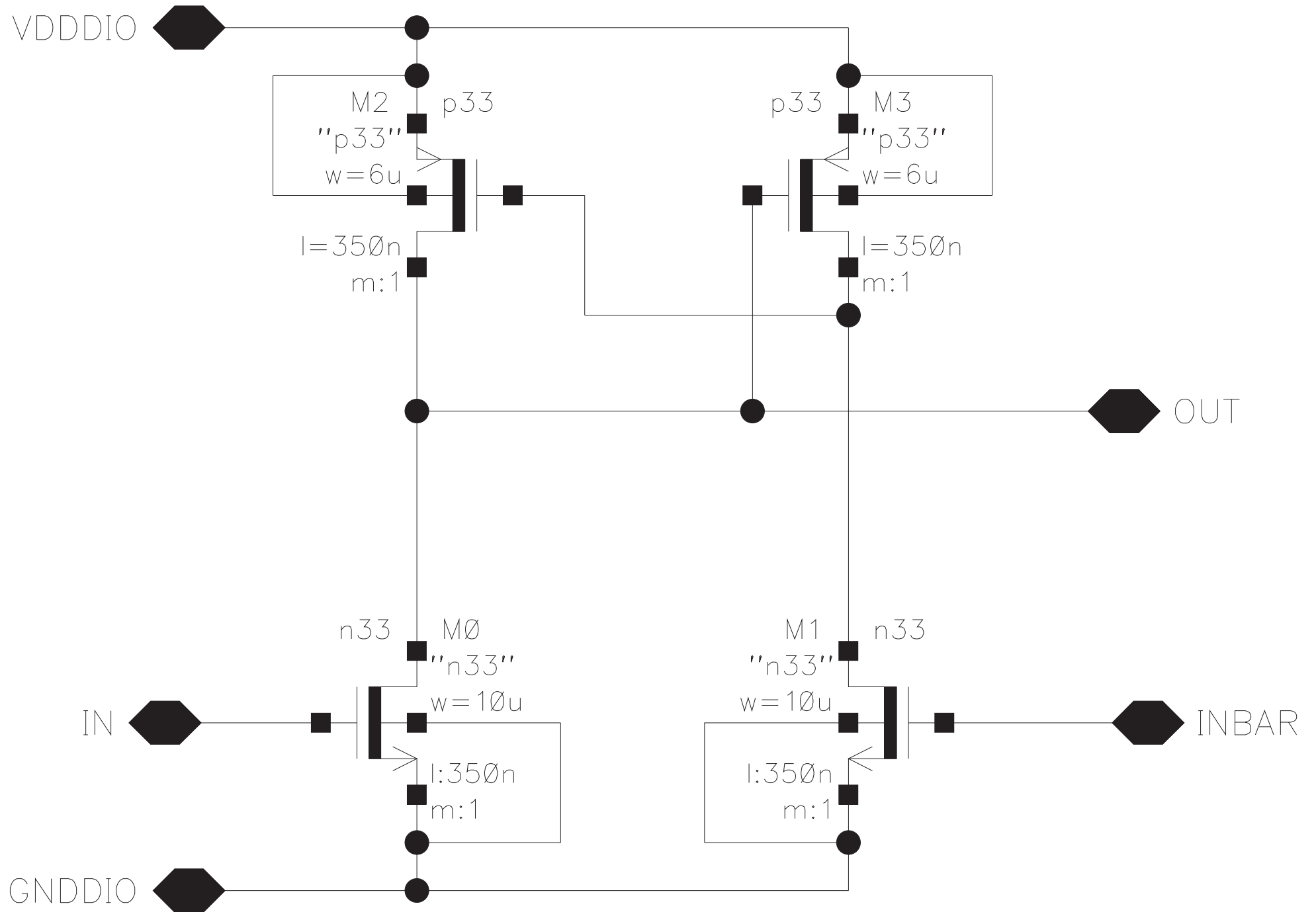


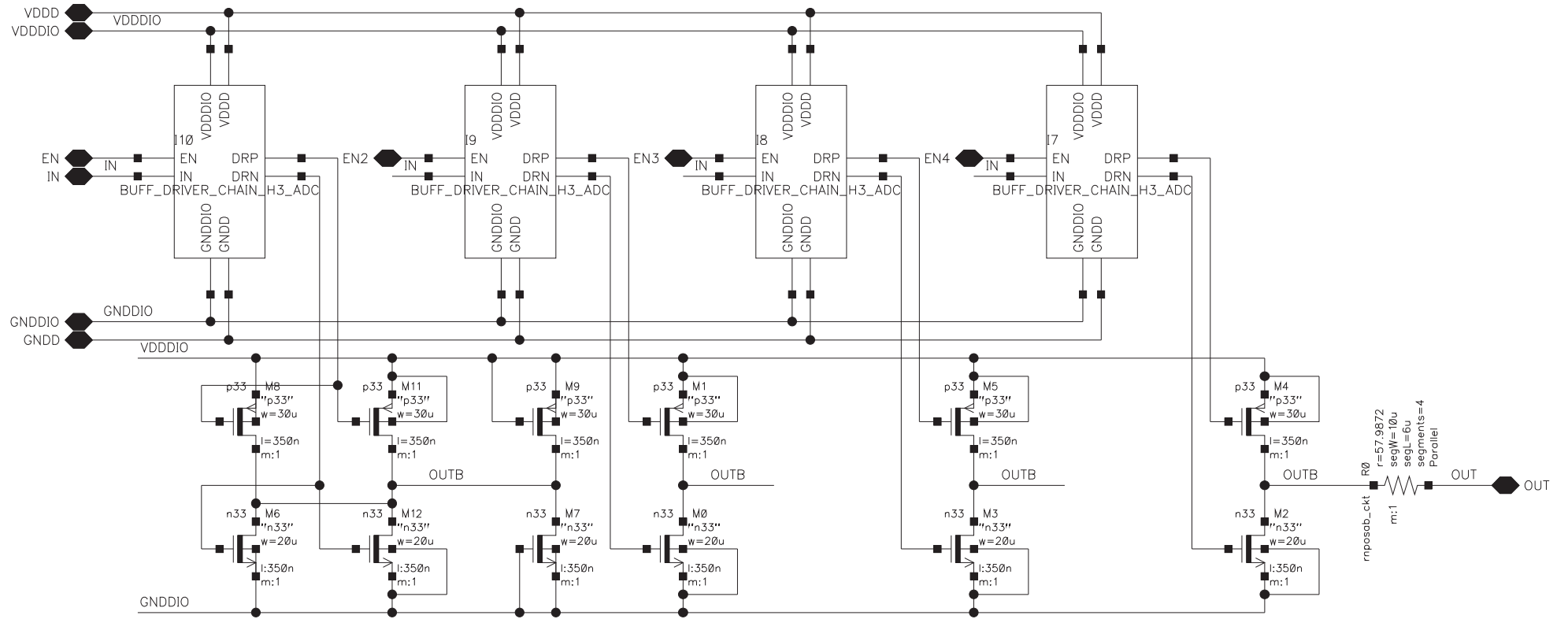


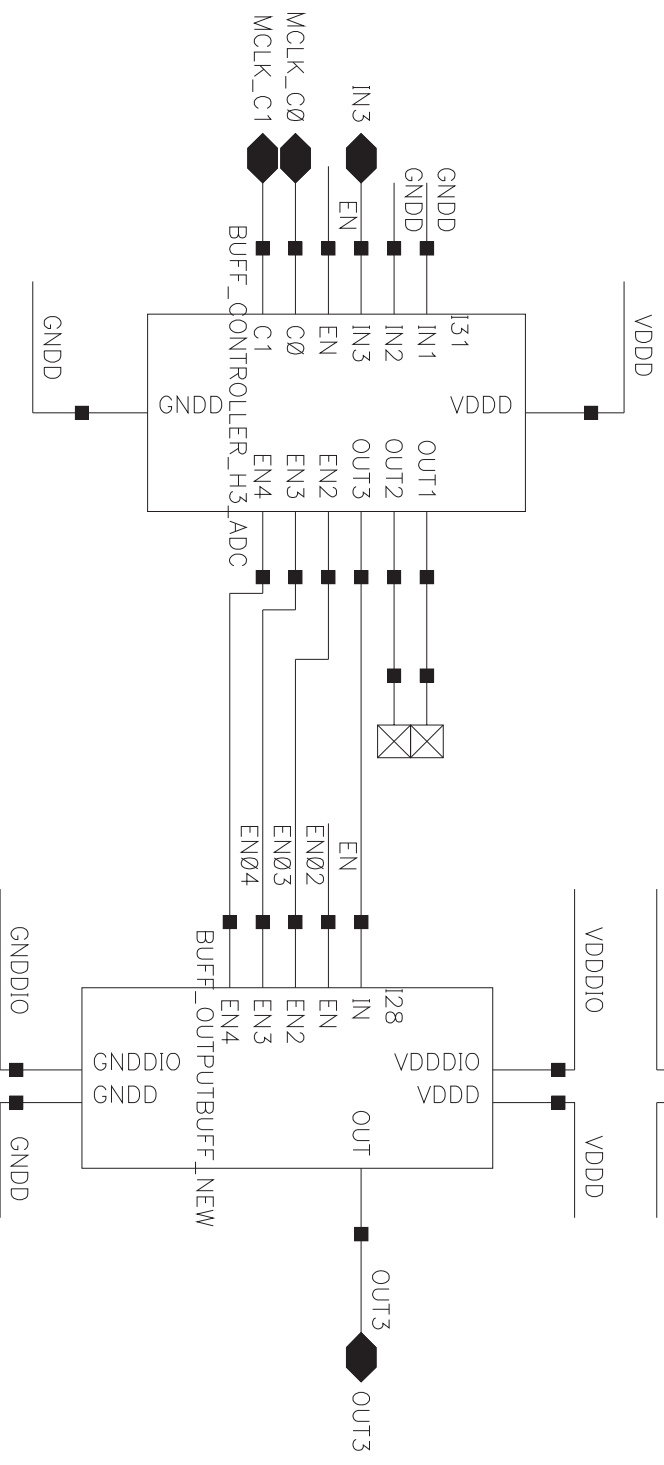
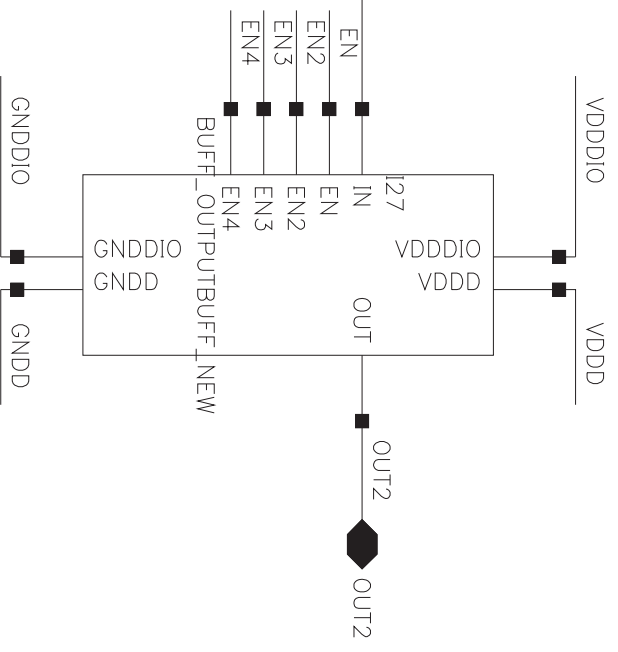
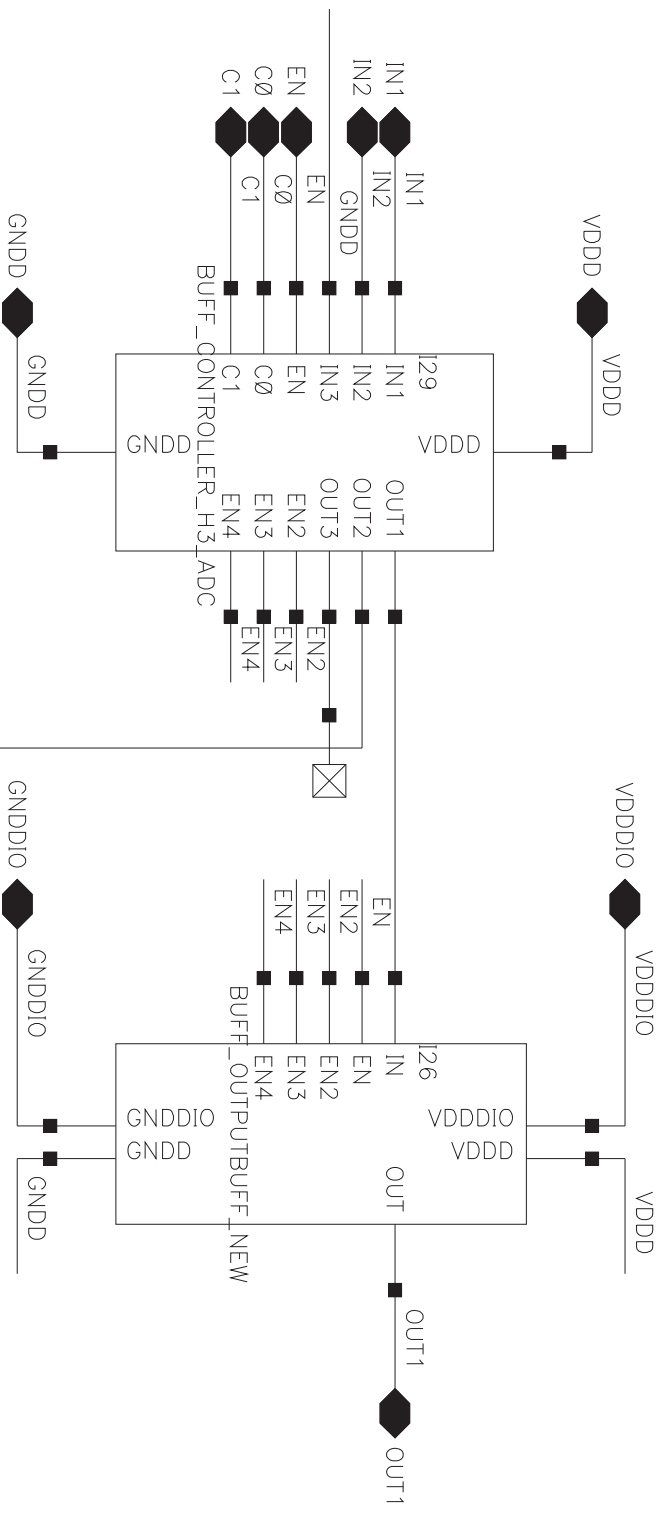




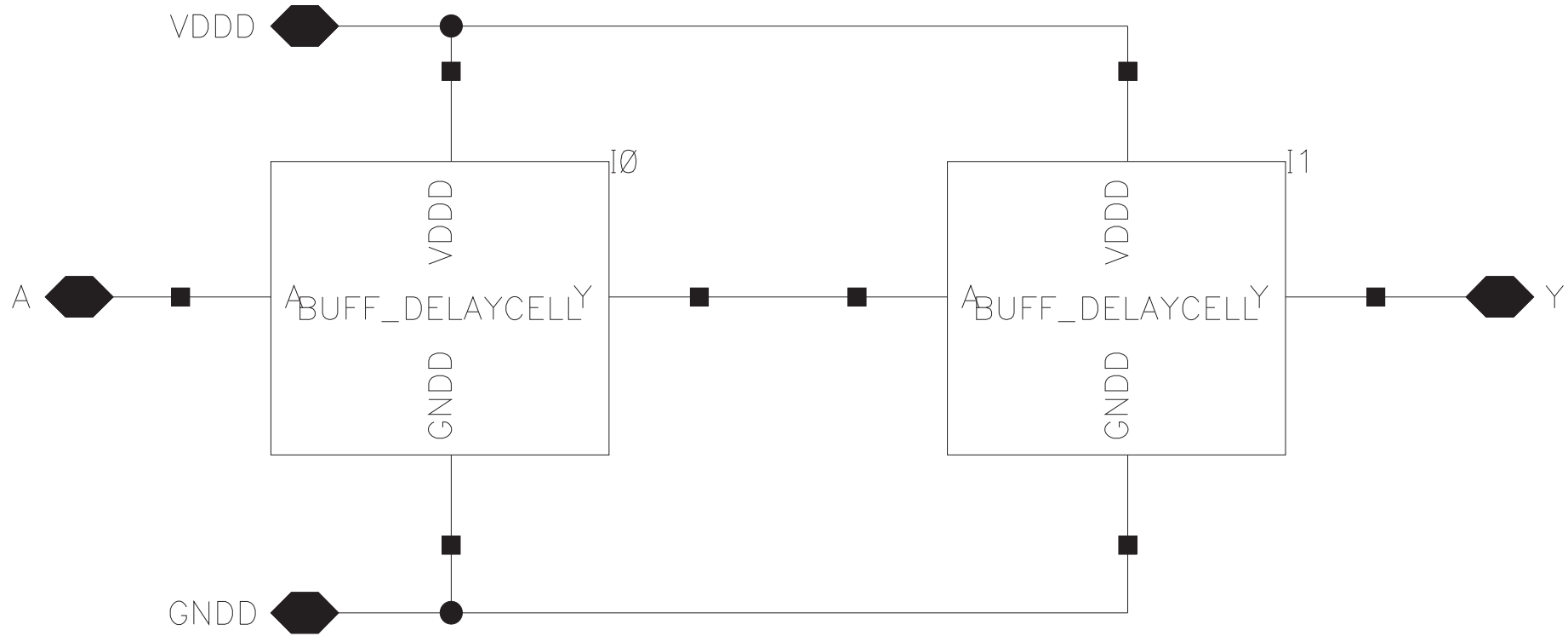


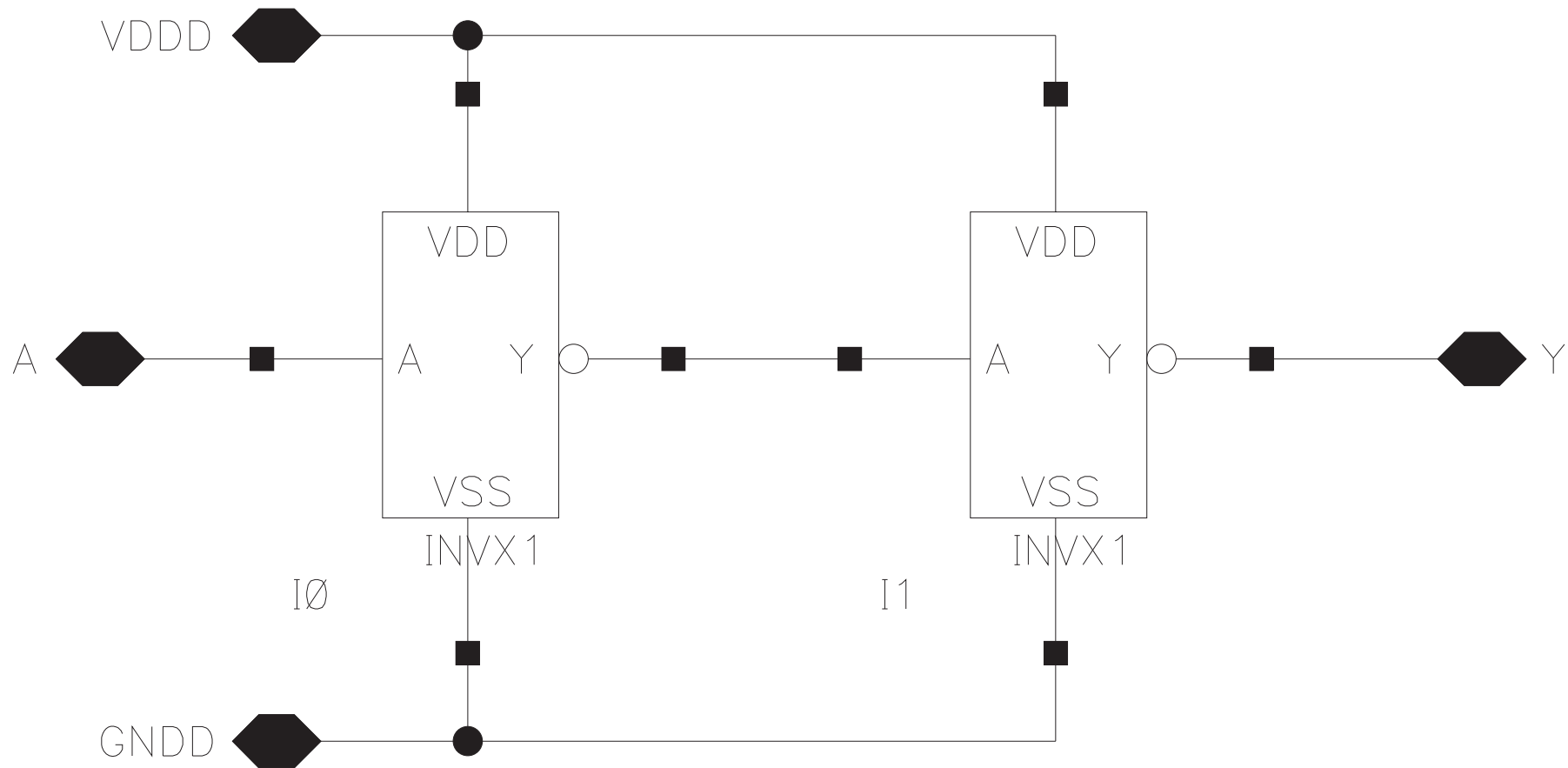


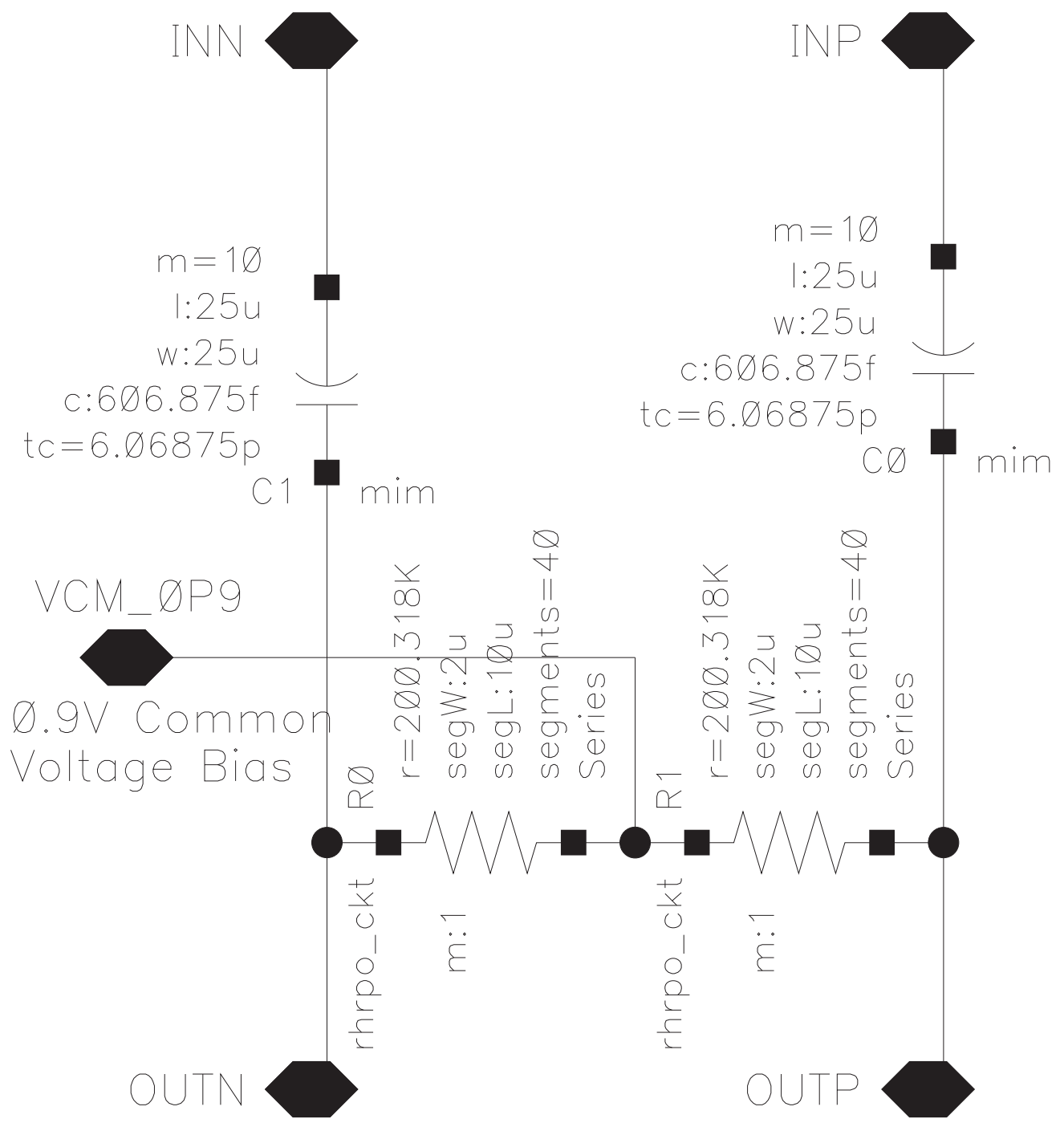


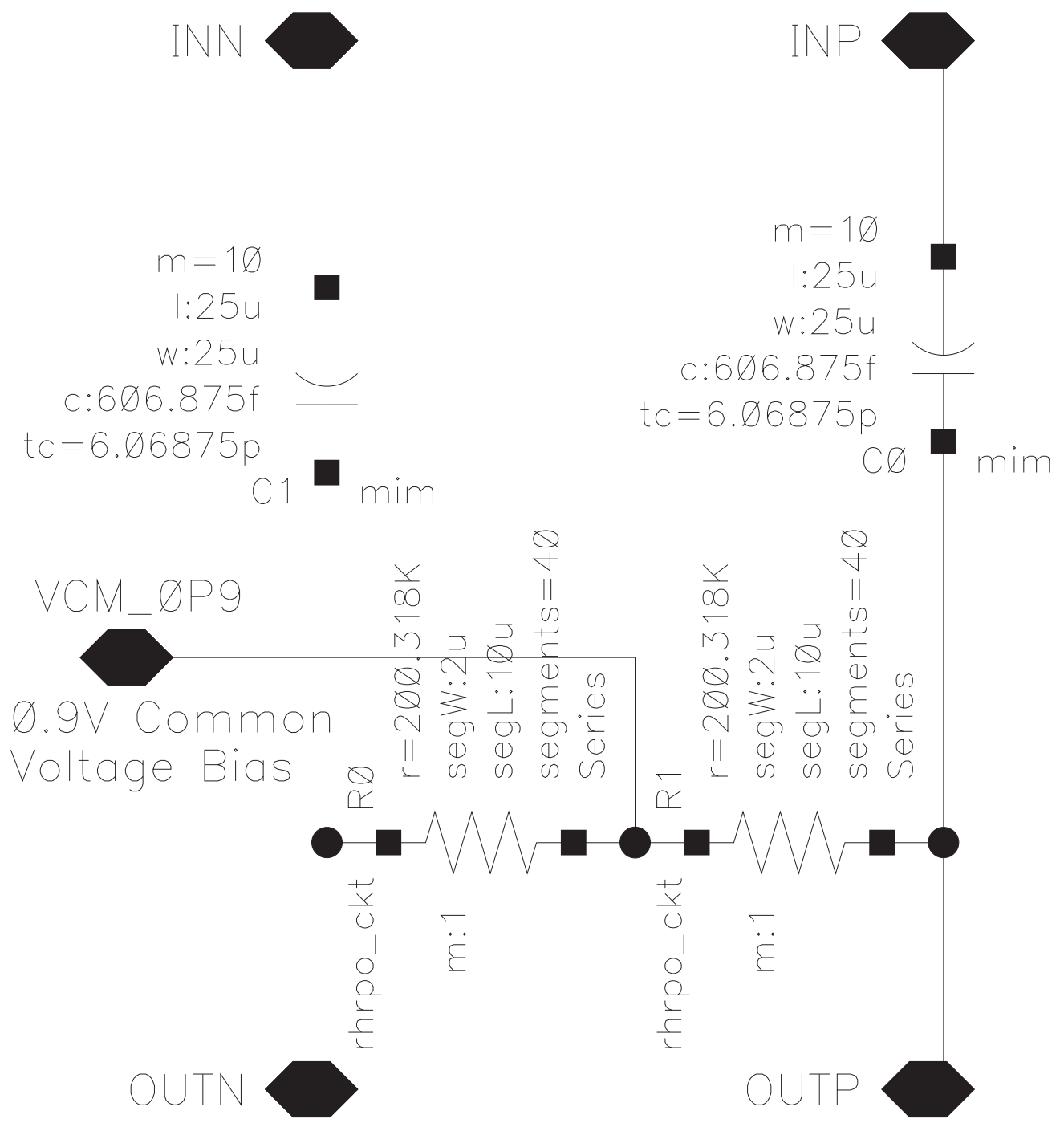


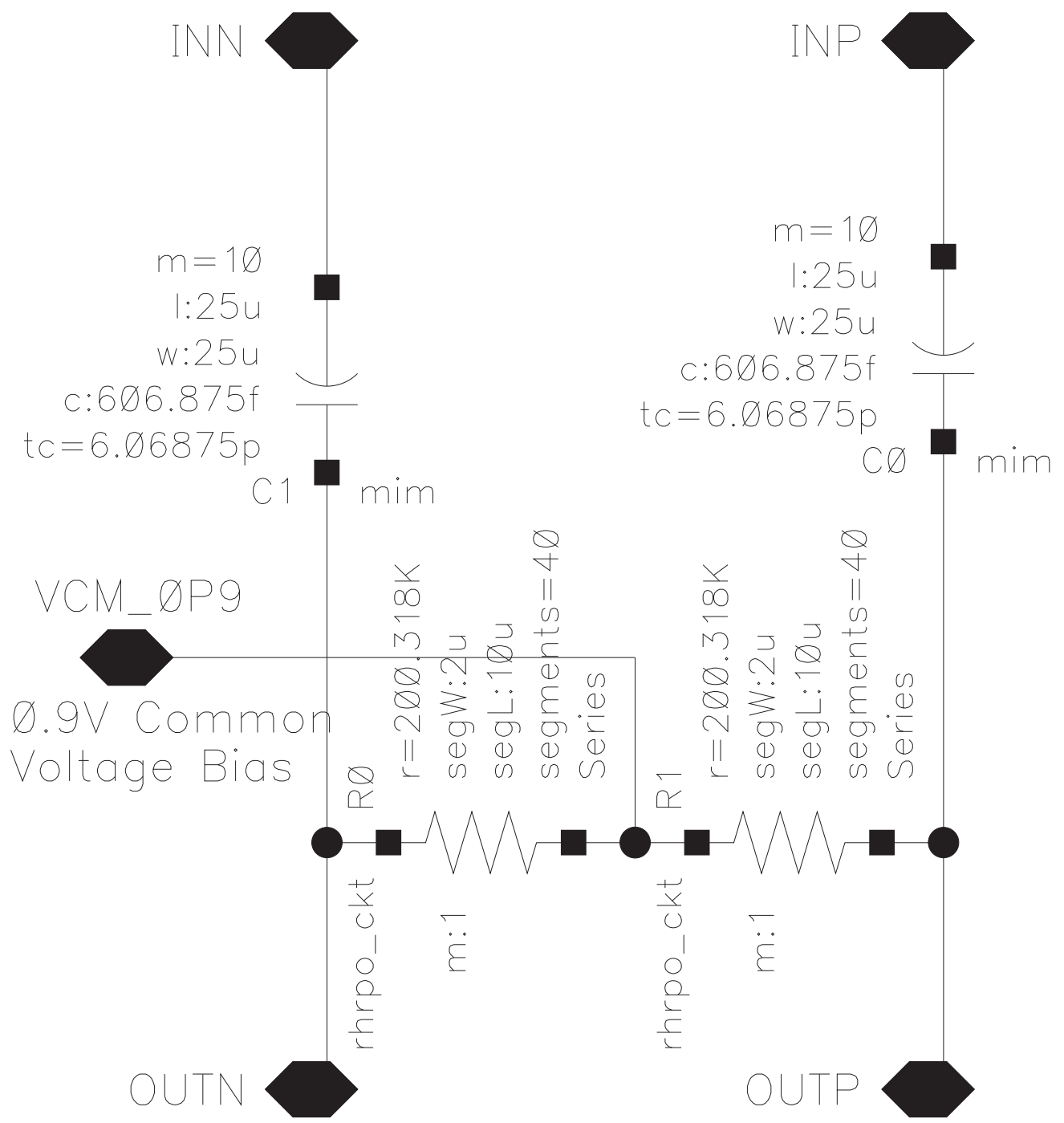


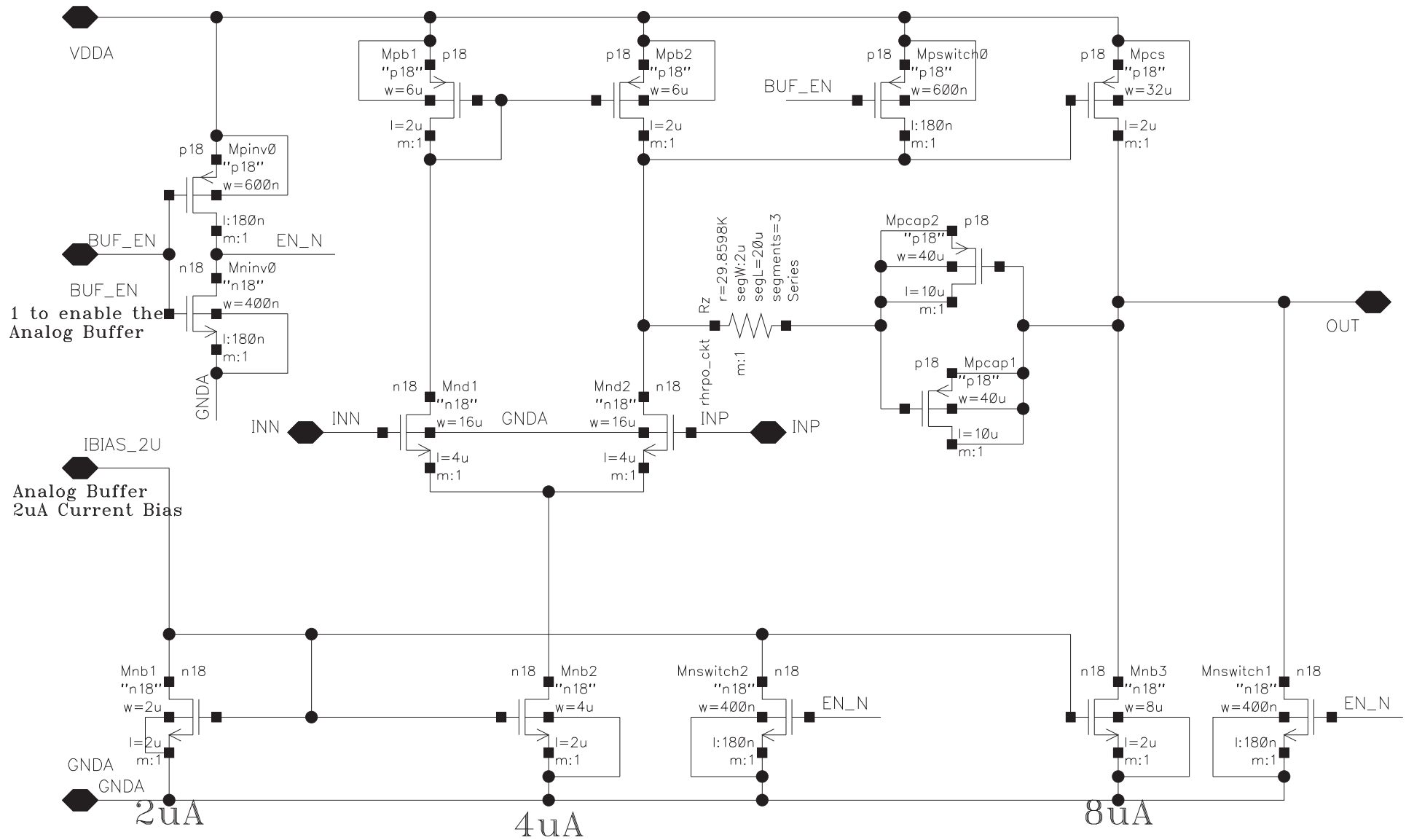


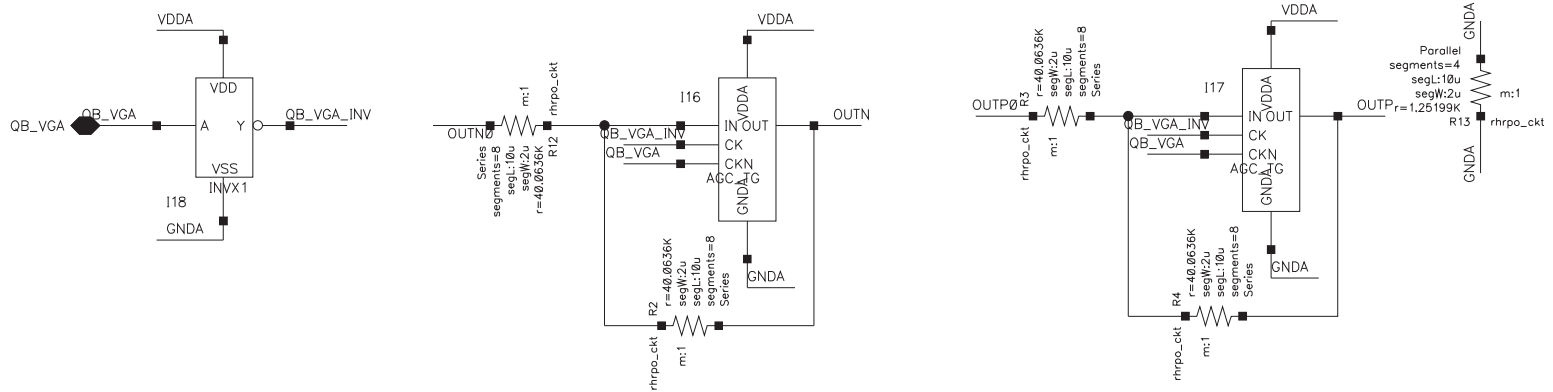
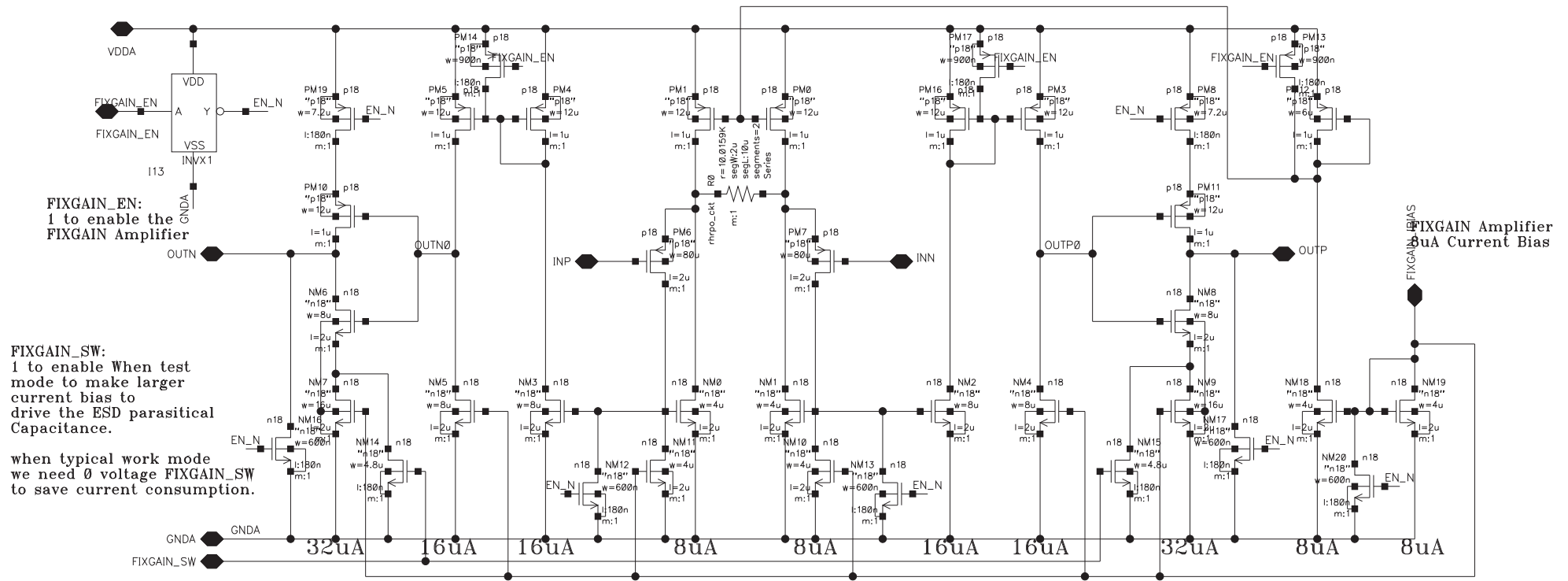


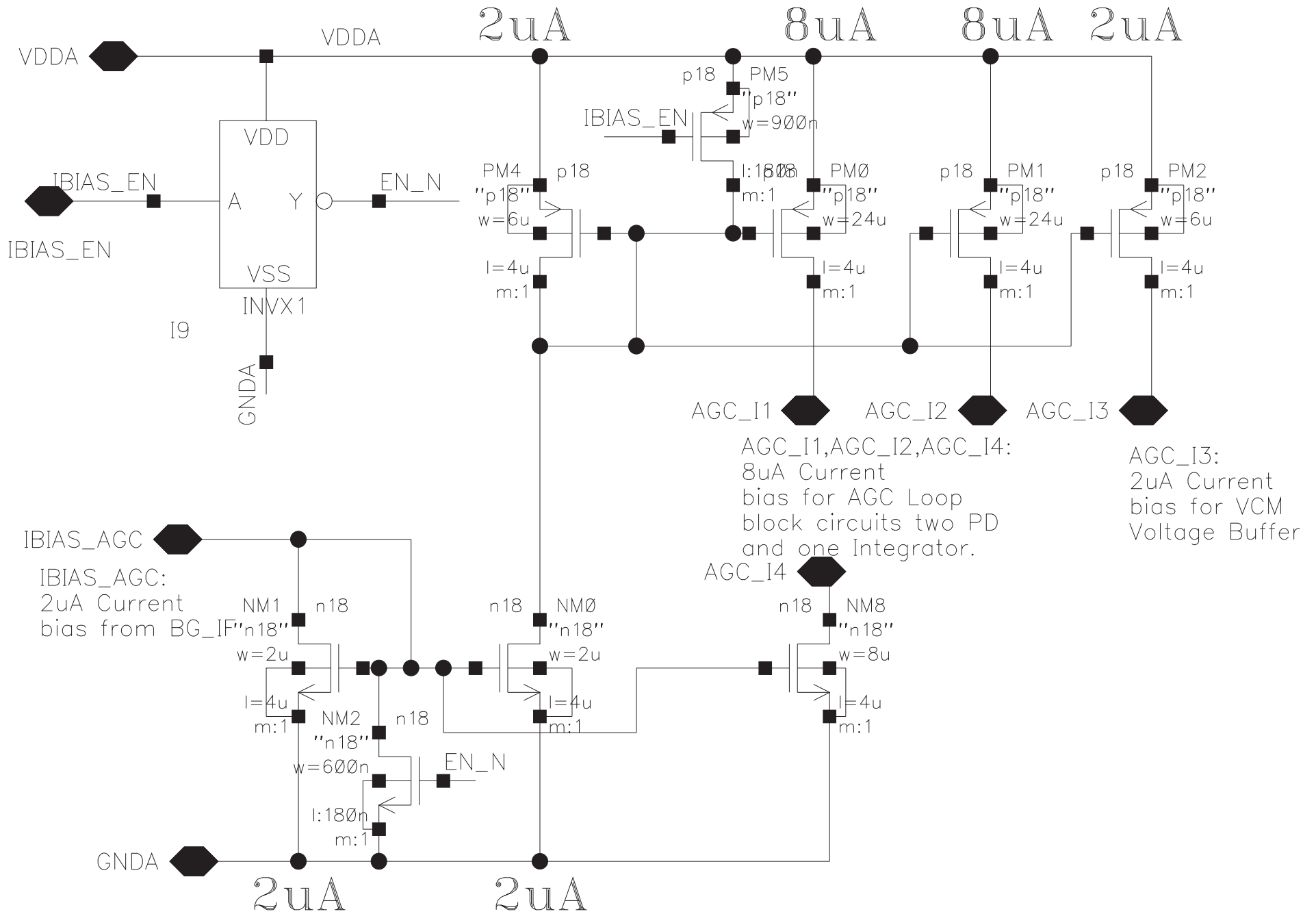




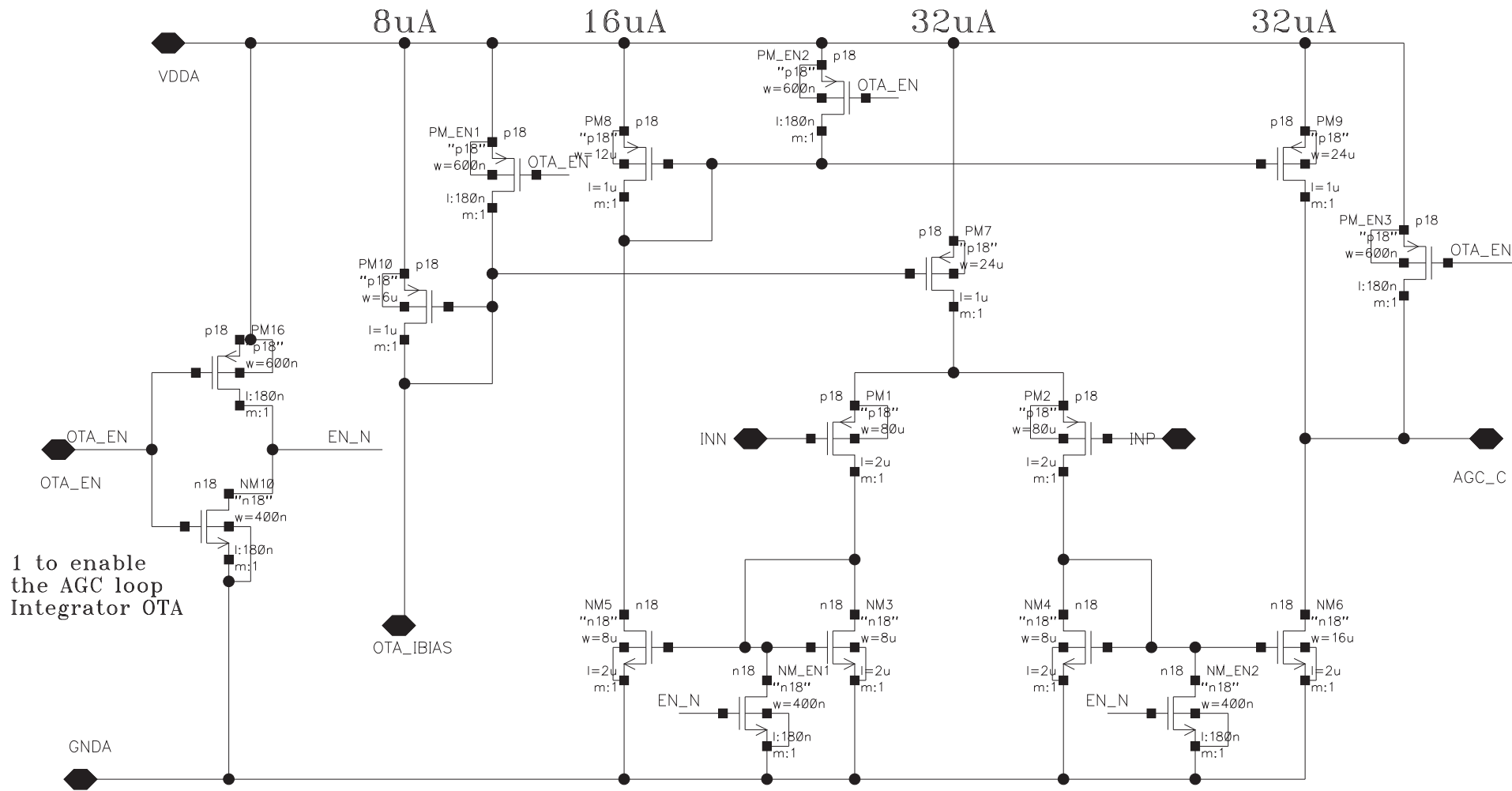




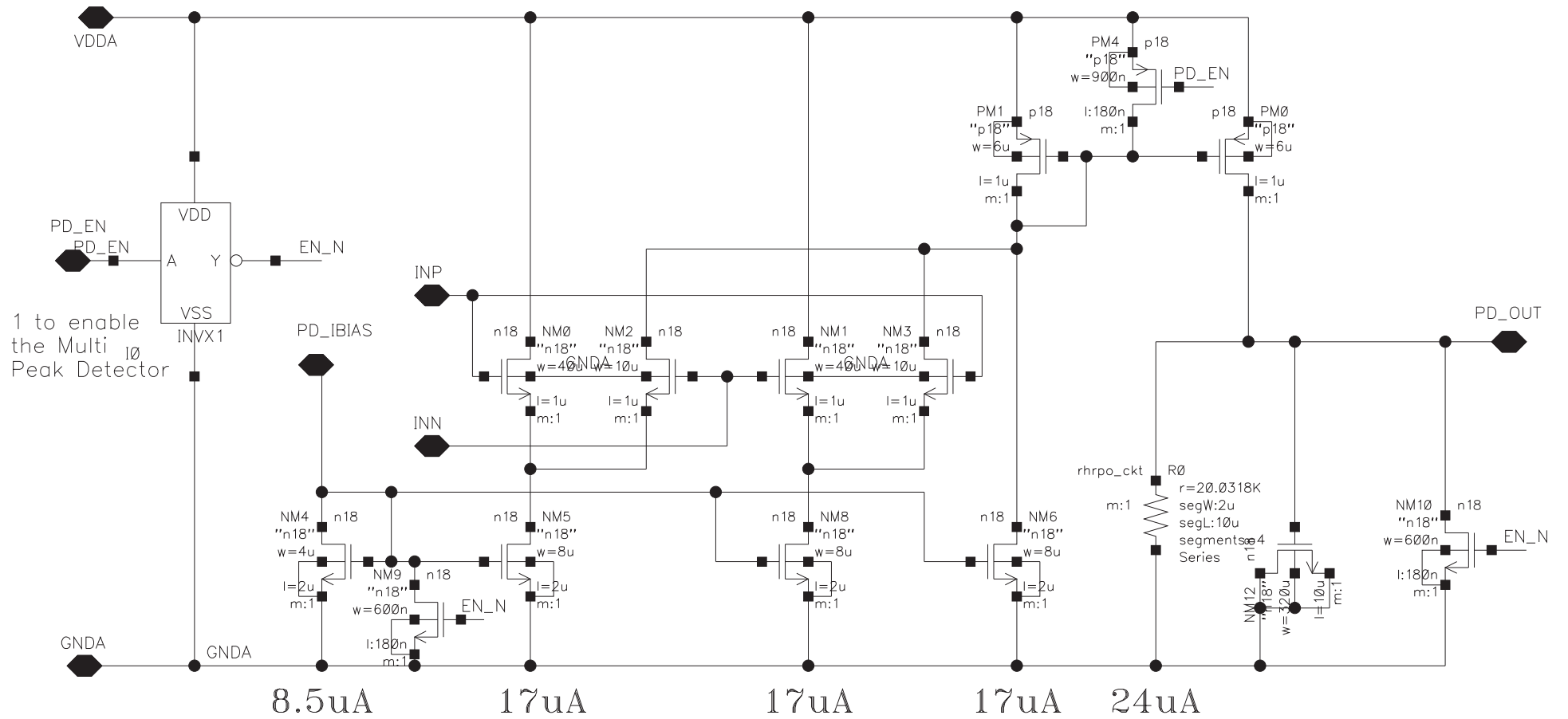


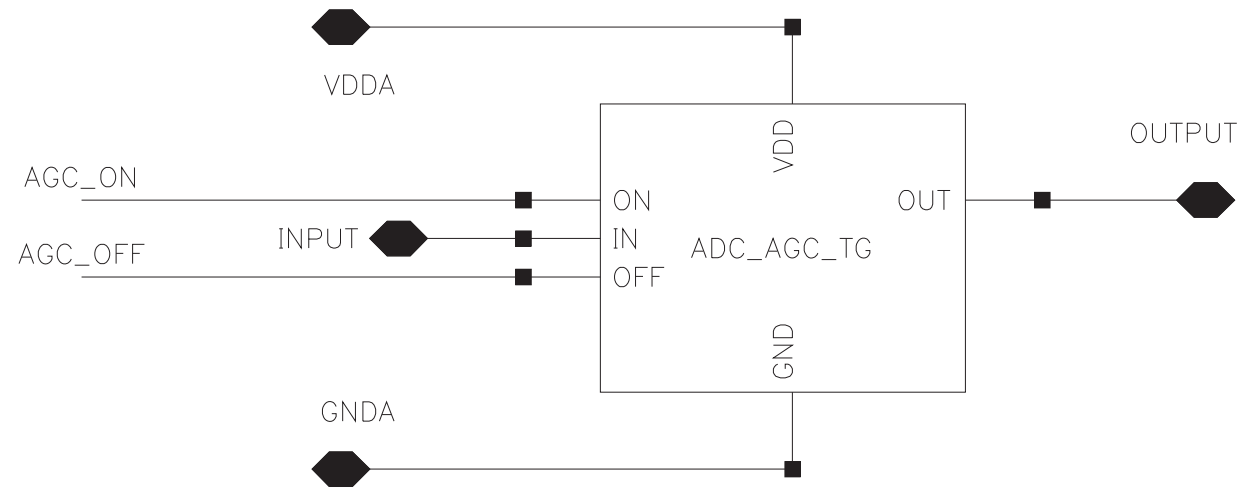
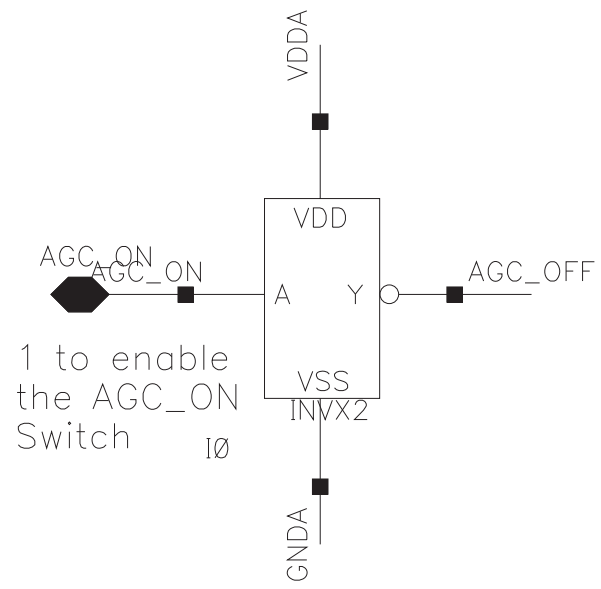


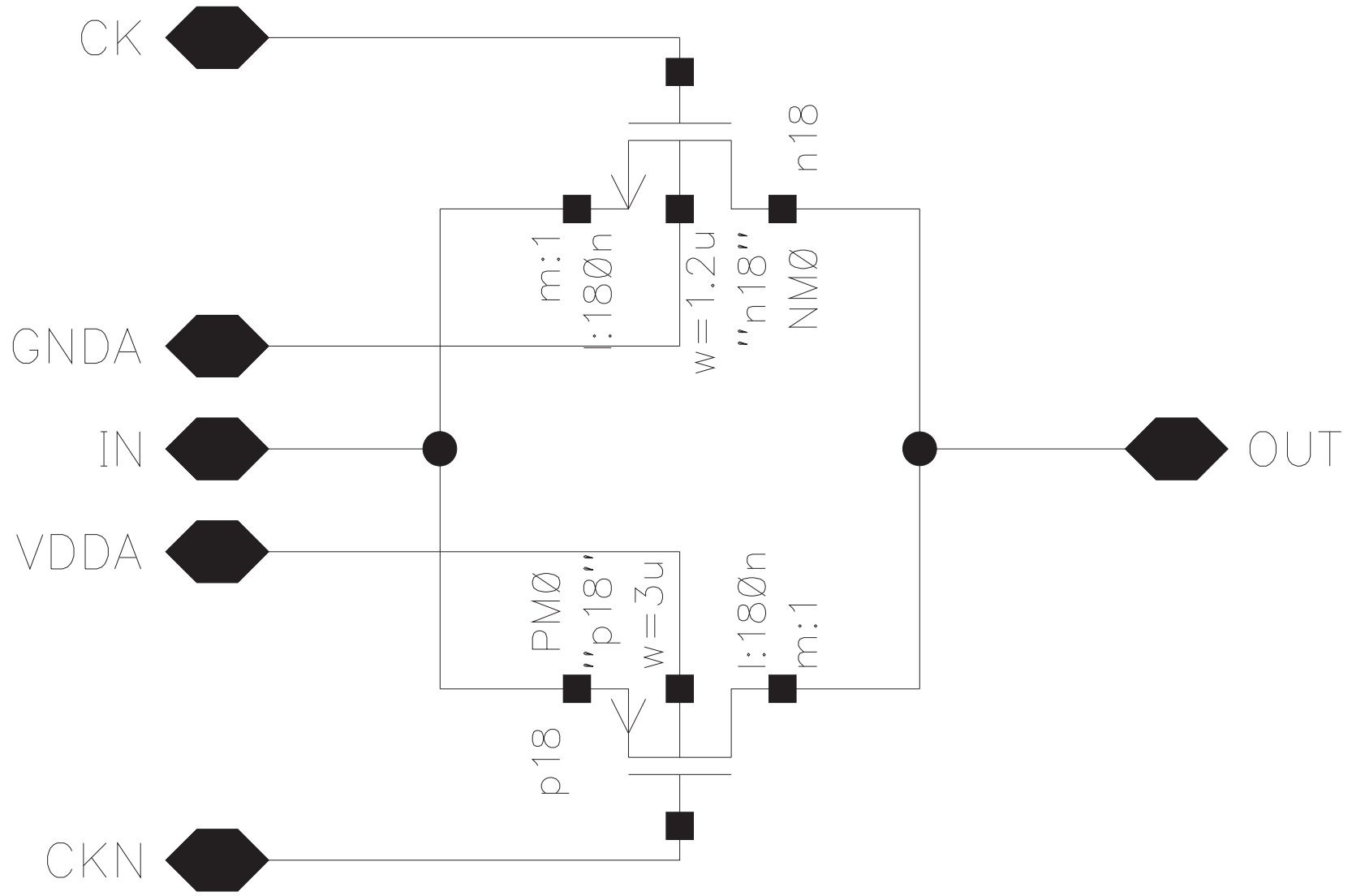


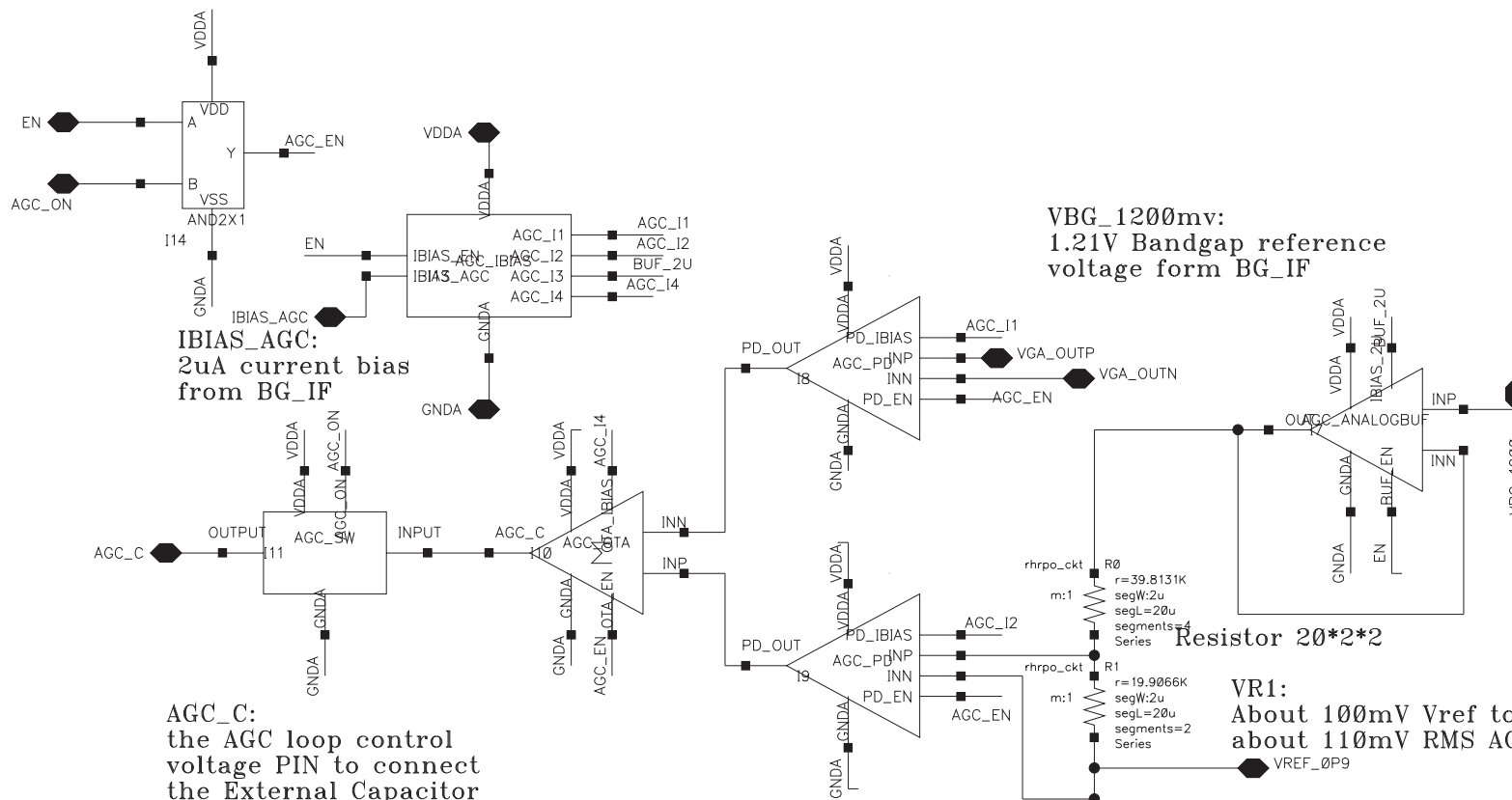


1 to enable the AGC loop Integrator OTA









**IBIAS\_AGC:**  
2uA current bias  
from BG\_IF

**AGC\_C:**  
the AGC loop control  
voltage PIN to connect  
the External Capacitor  
and supply a control Voltage  
to 3 stages VGA.

**VBG\_1200mv:**  
1.21V Bandgap reference  
voltage form BG\_IF

**Resistor 20\*2\*2**

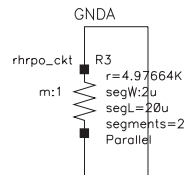
**VR1:**  
About 100mV Vref to define  
about 110mV RMS AGWN.

**VREF\_0P9:**  
0.9V Voltage Bias  
for VCM.

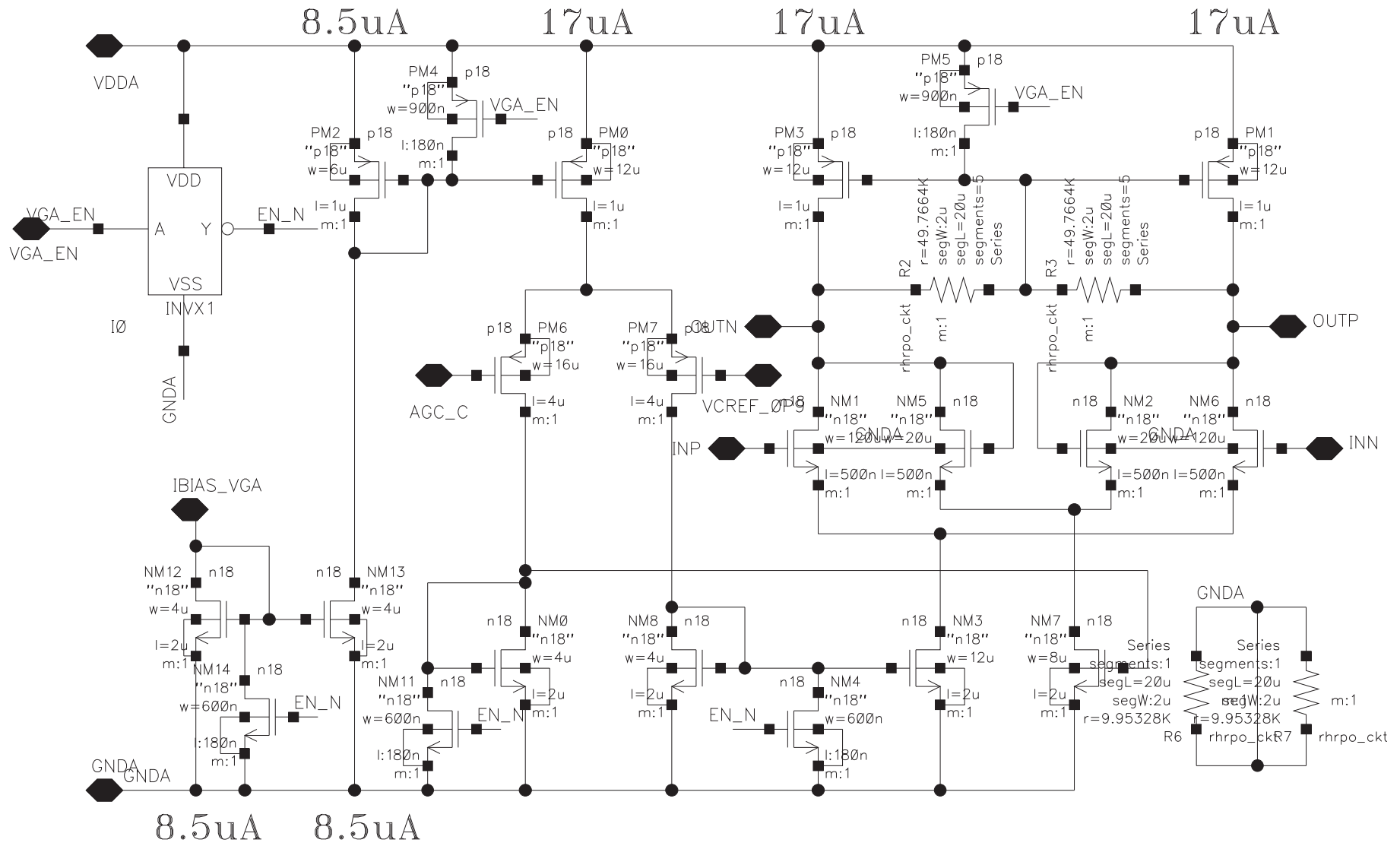
**VCREf\_0P75:**  
0.75V Voltage Bias  
for VCREf.

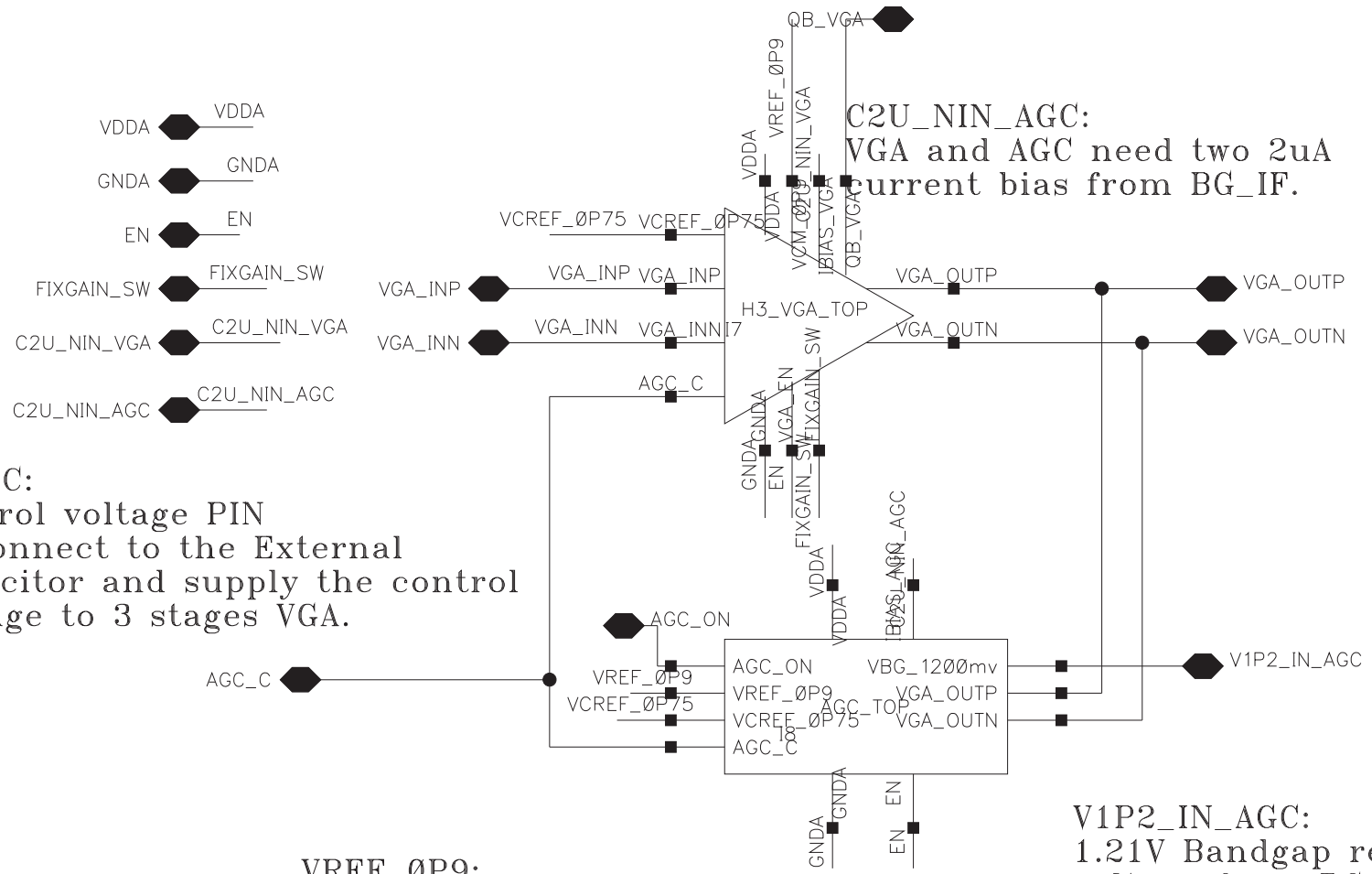
Be Careful !!!

Here we use the EN signal,  
to enable to supply VREF\_0P9  
when AGC disable but control by  
ADC !!!!!!!







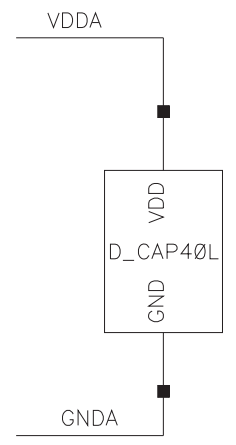


C2U\_NIN\_AGC:  
VGA and AGC need two 2uA  
current bias from BG\_IF.

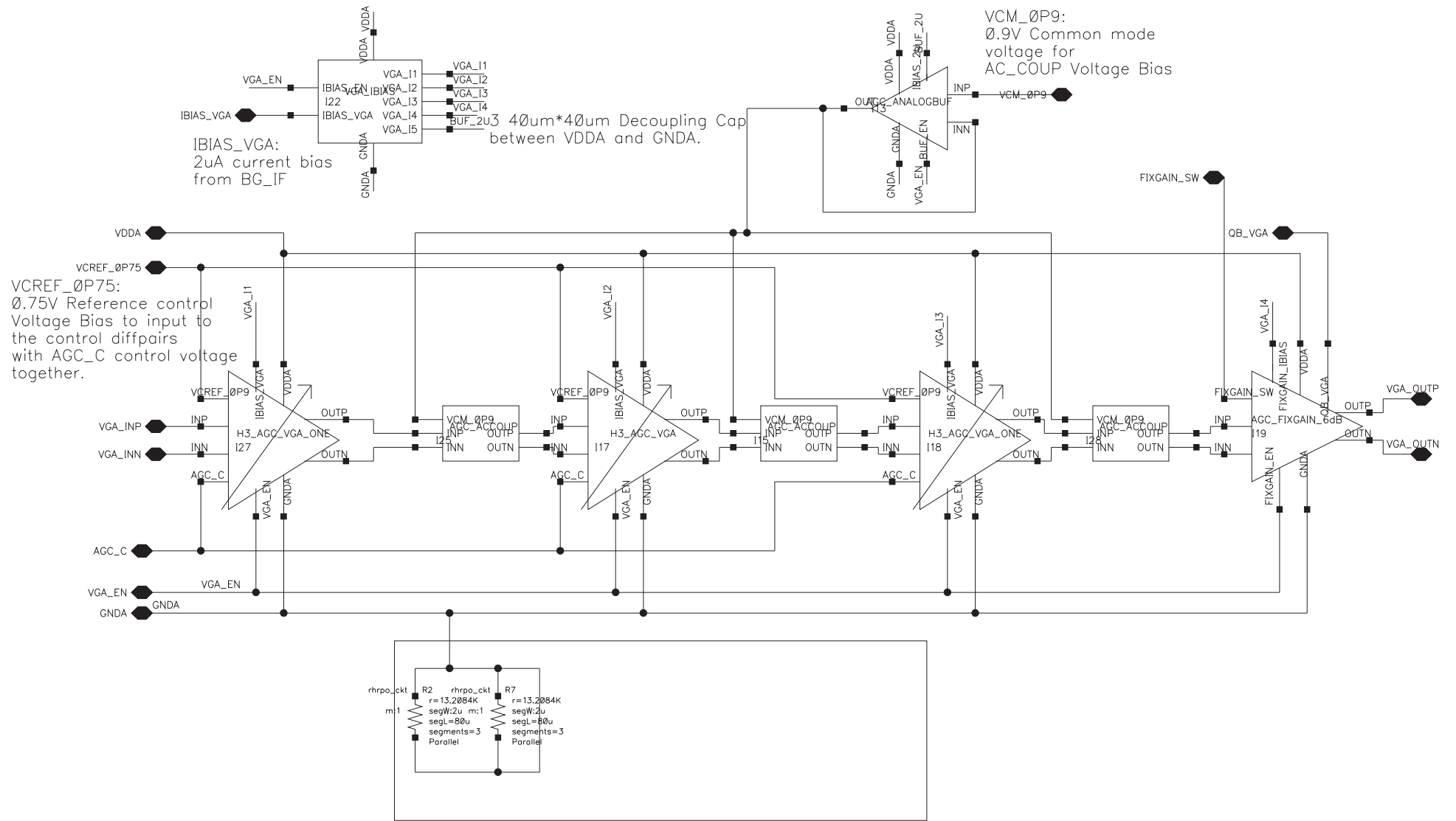
AGC\_C:  
Control voltage PIN  
to connect to the External  
Capacitor and supply the control  
Voltage to 3 stages VGA.

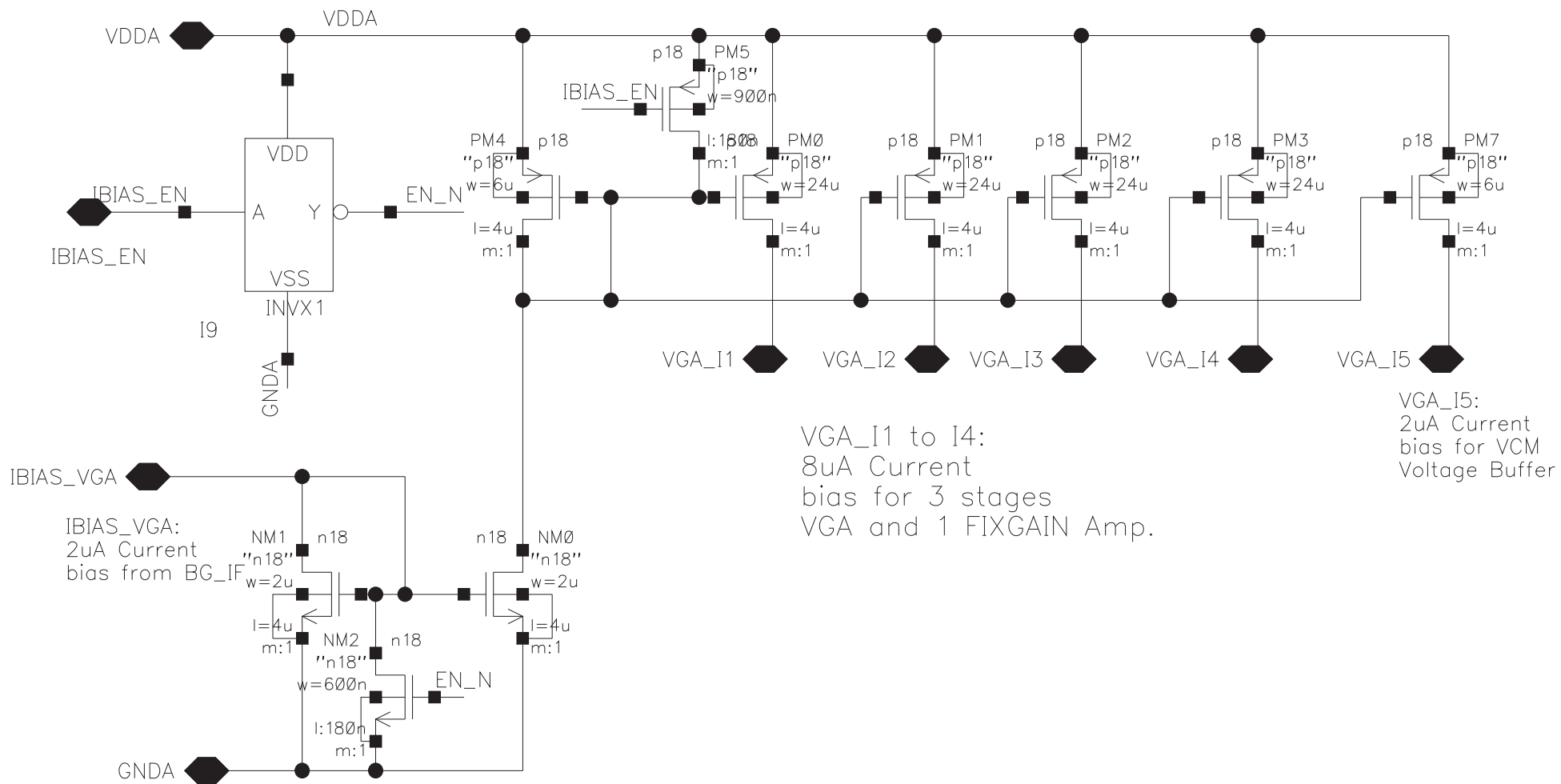
VREF\_0P9:  
0.9V Voltage Bias from  
VBG\_1P21 divide with Resistor  
Array, and supply to VCM and  
VCMREF (Control Reference Voltage).

V1P2\_IN\_AGC:  
1.21V Bandgap reference  
voltage from BG\_IF.



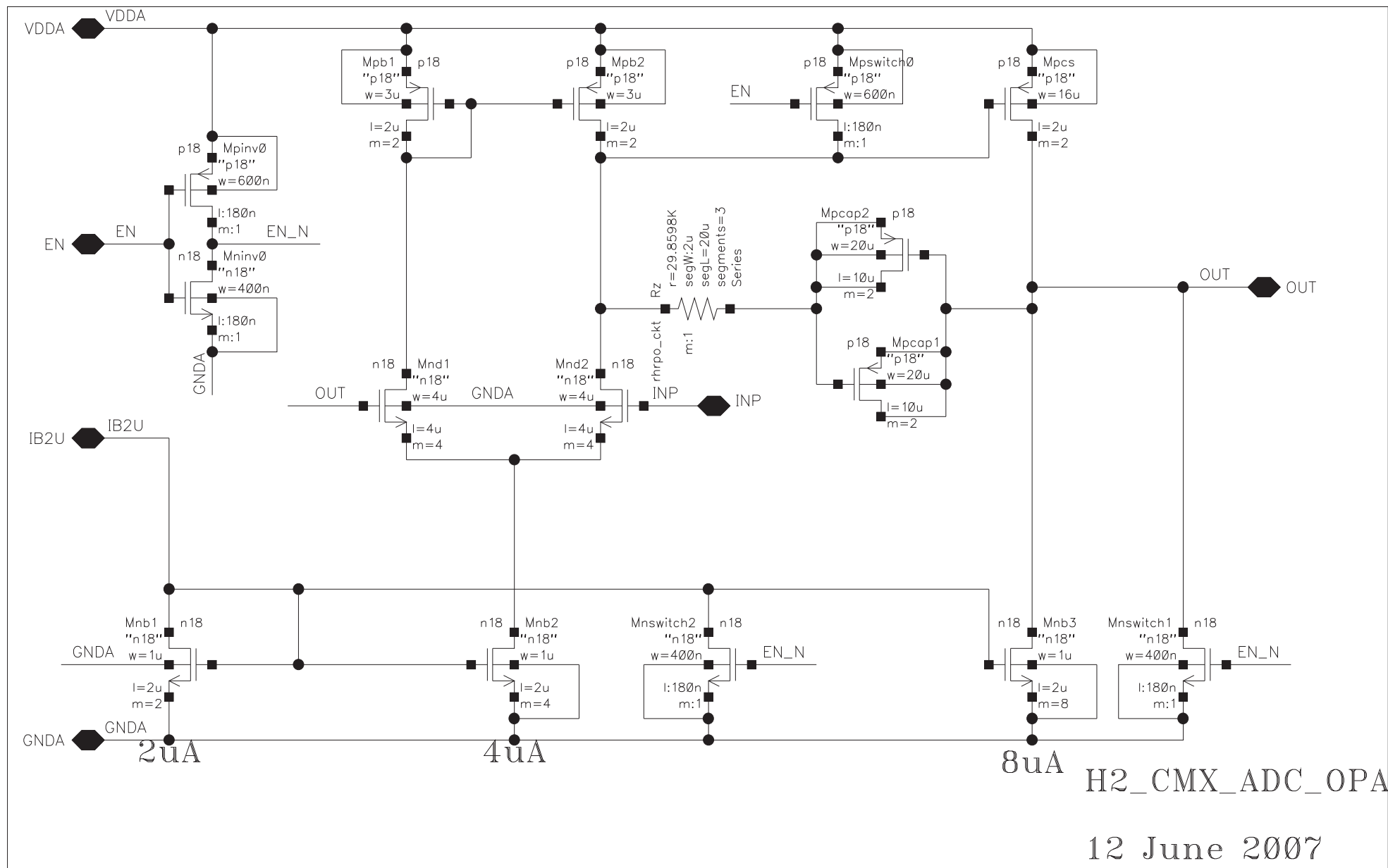


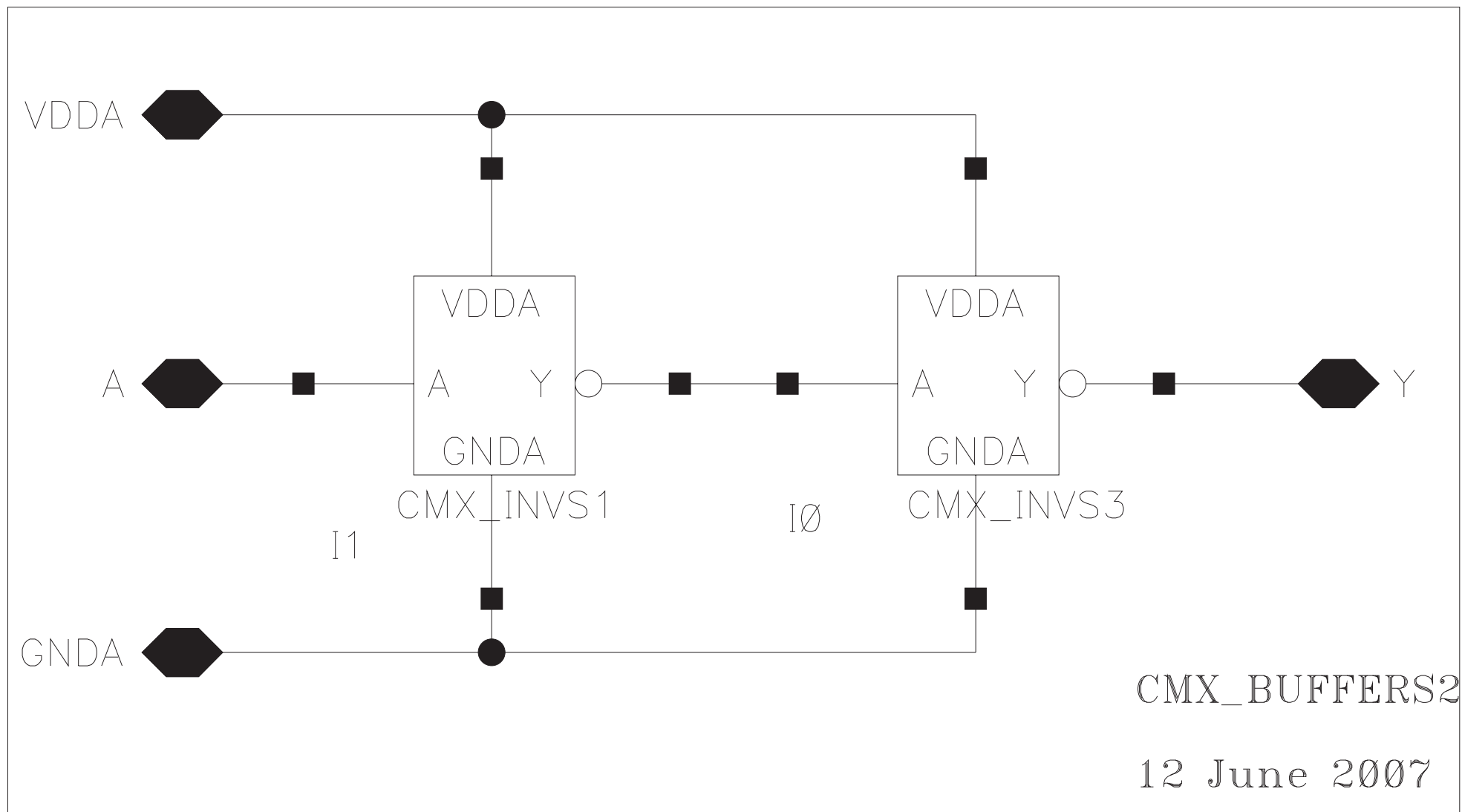


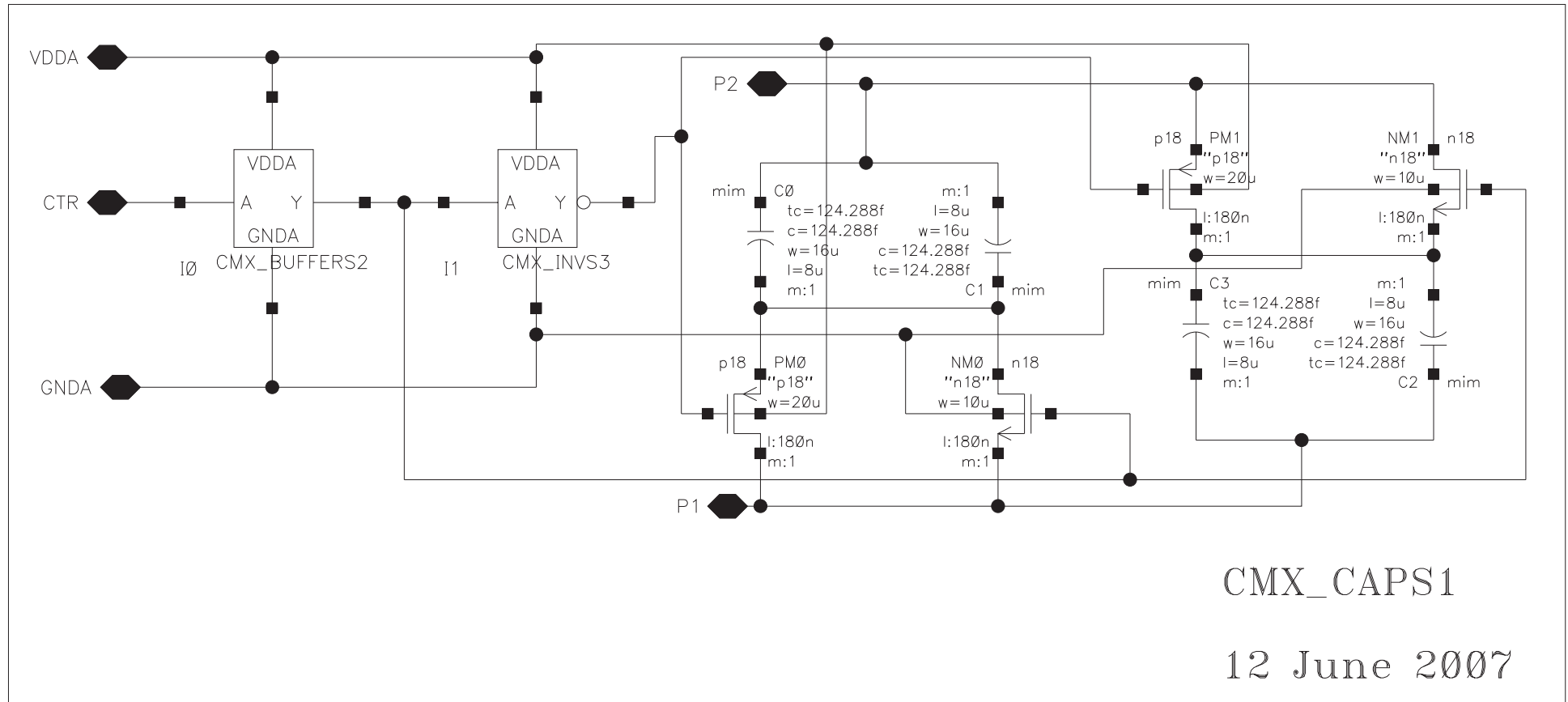


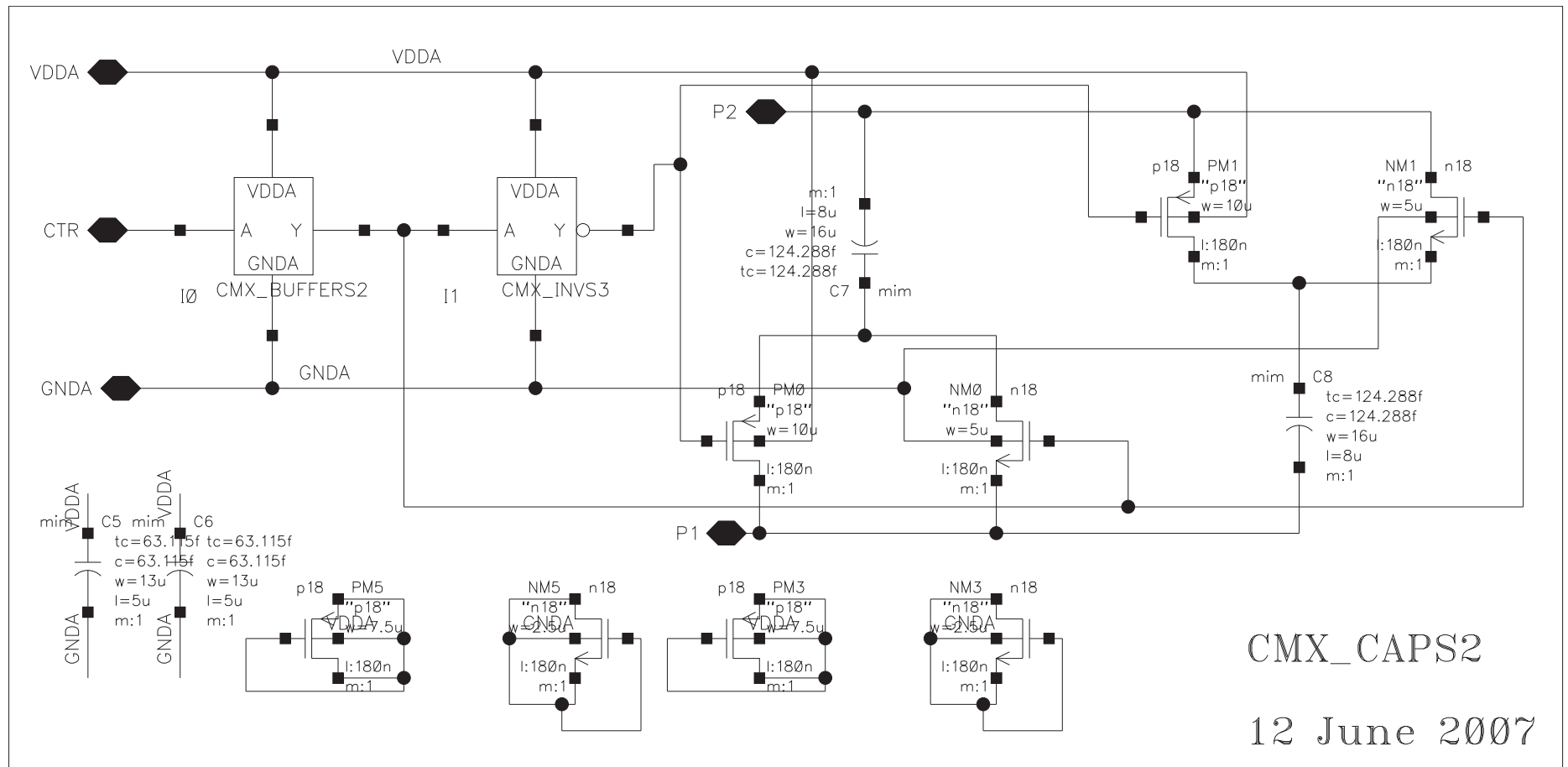
VGA\_I1 to I4:  
 8uA Current  
 bias for 3 stages  
 VGA and 1 FIXGAIN Amp.

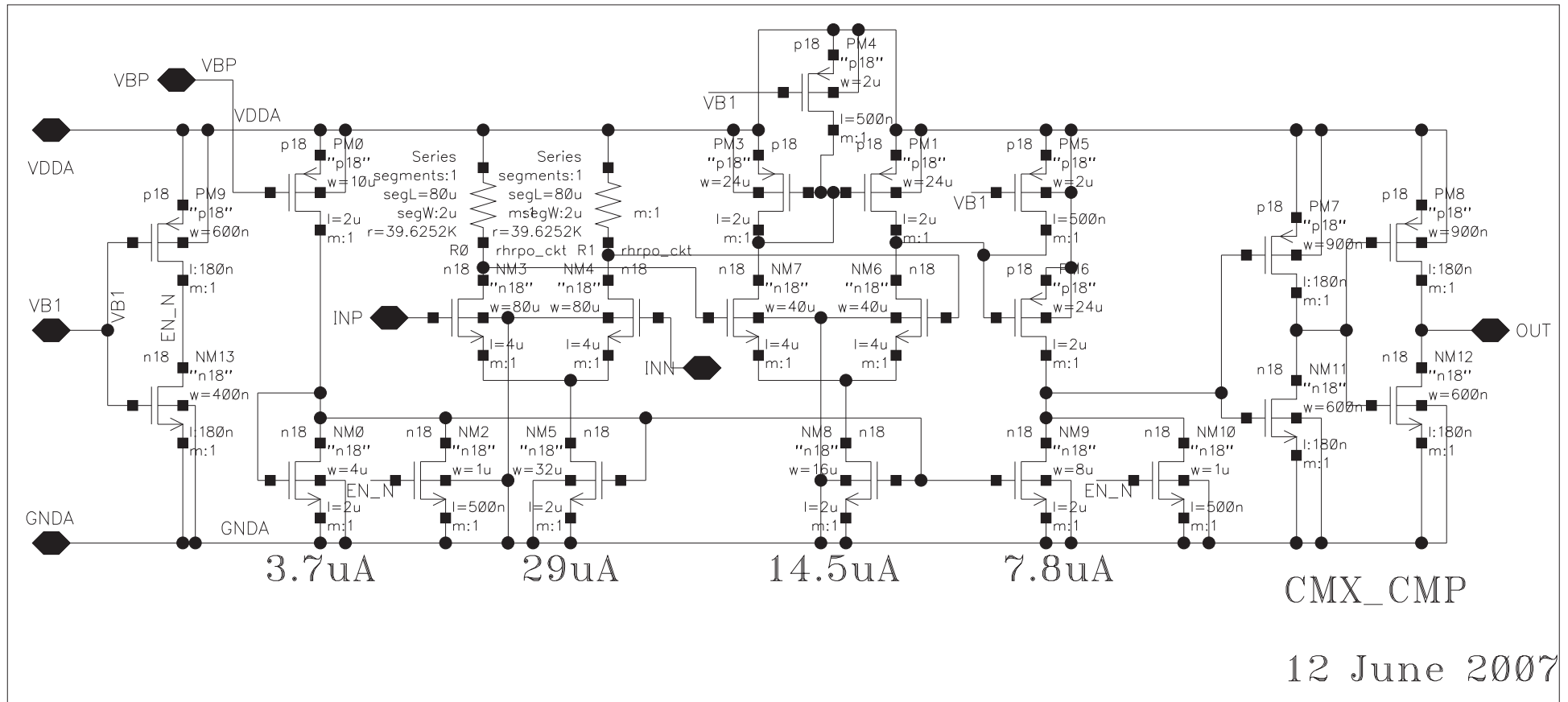
VGA\_I5:  
 2uA Current  
 bias for VCM  
 Voltage Buffer

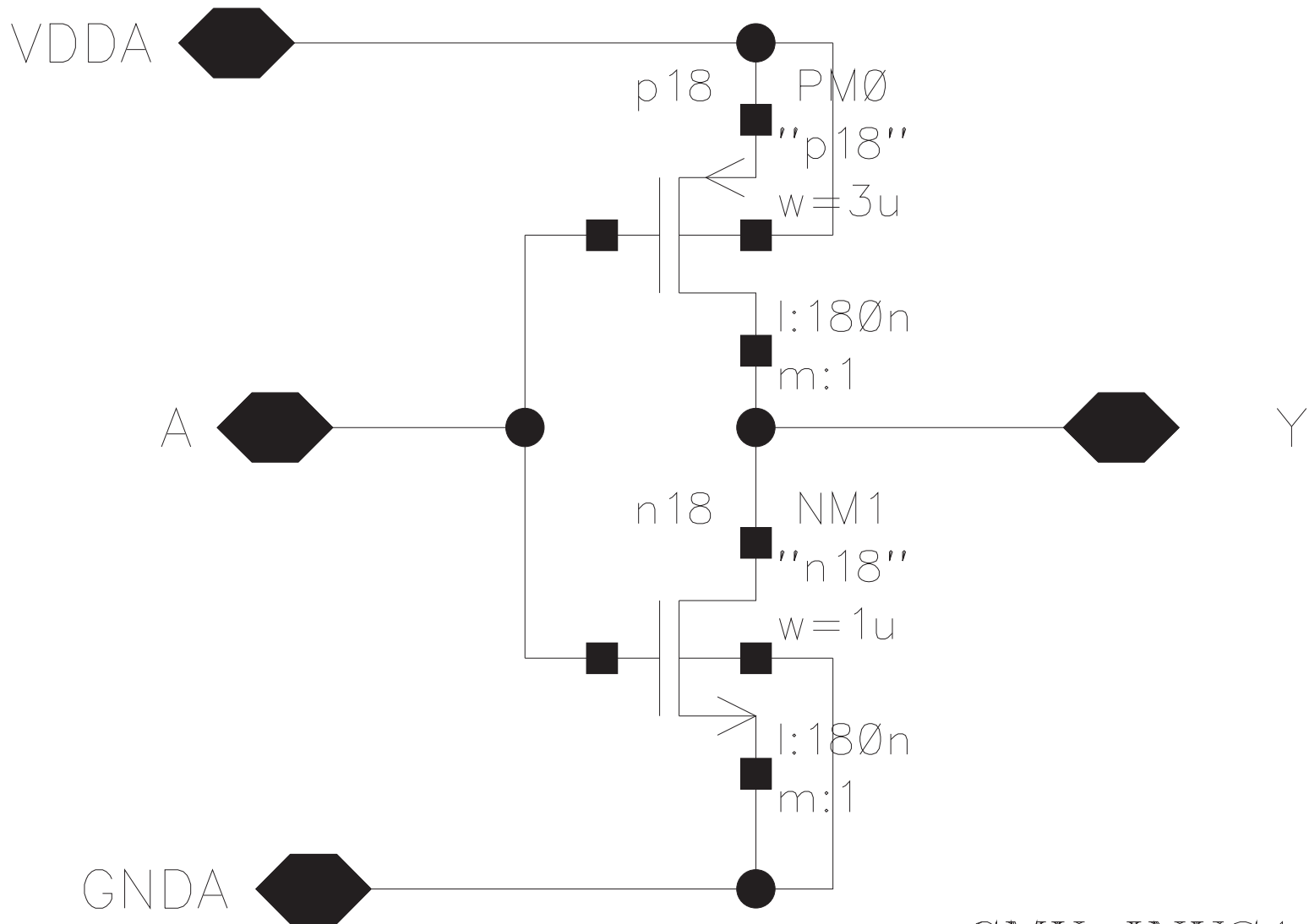








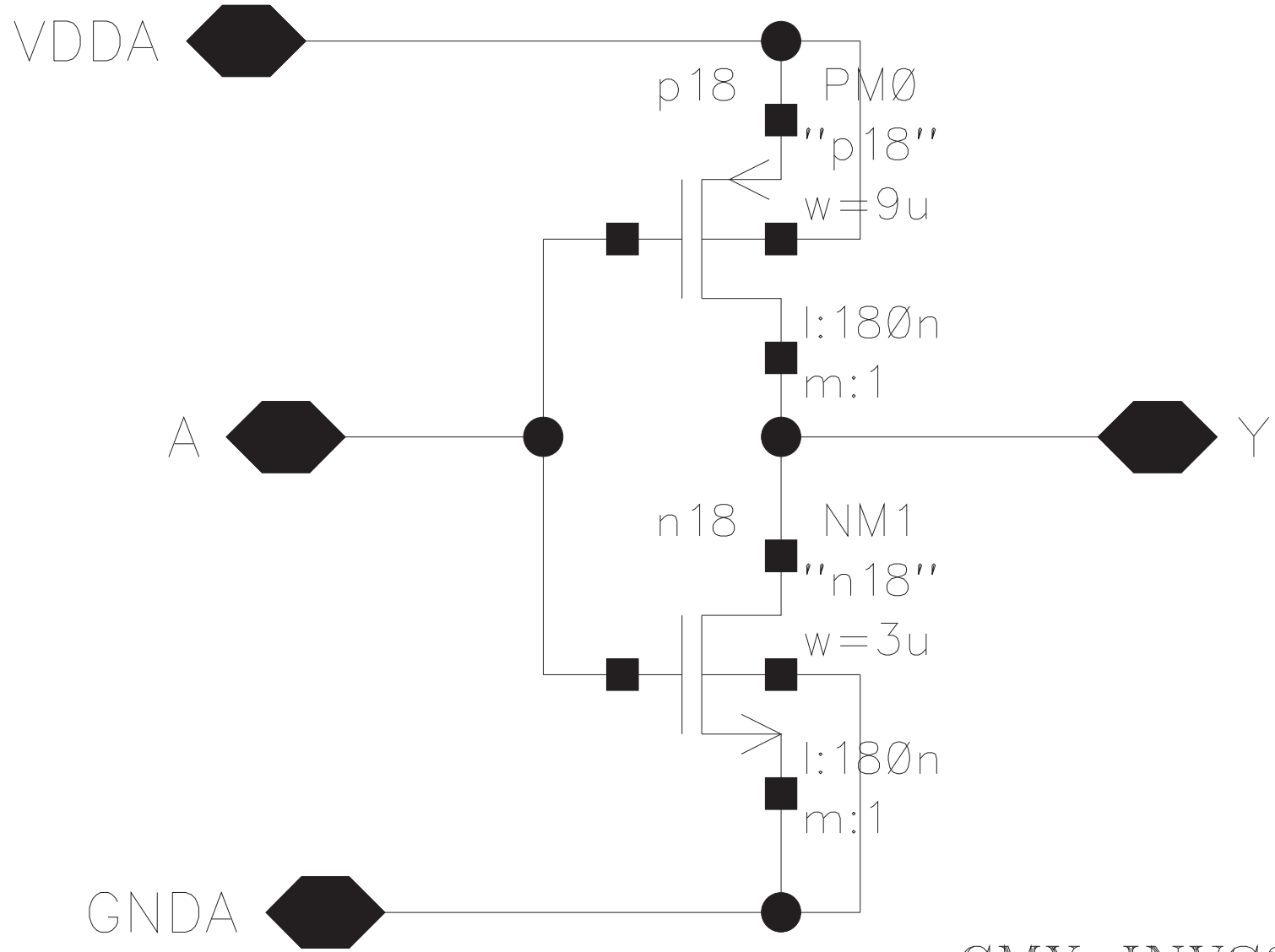




CMX\_INVS1

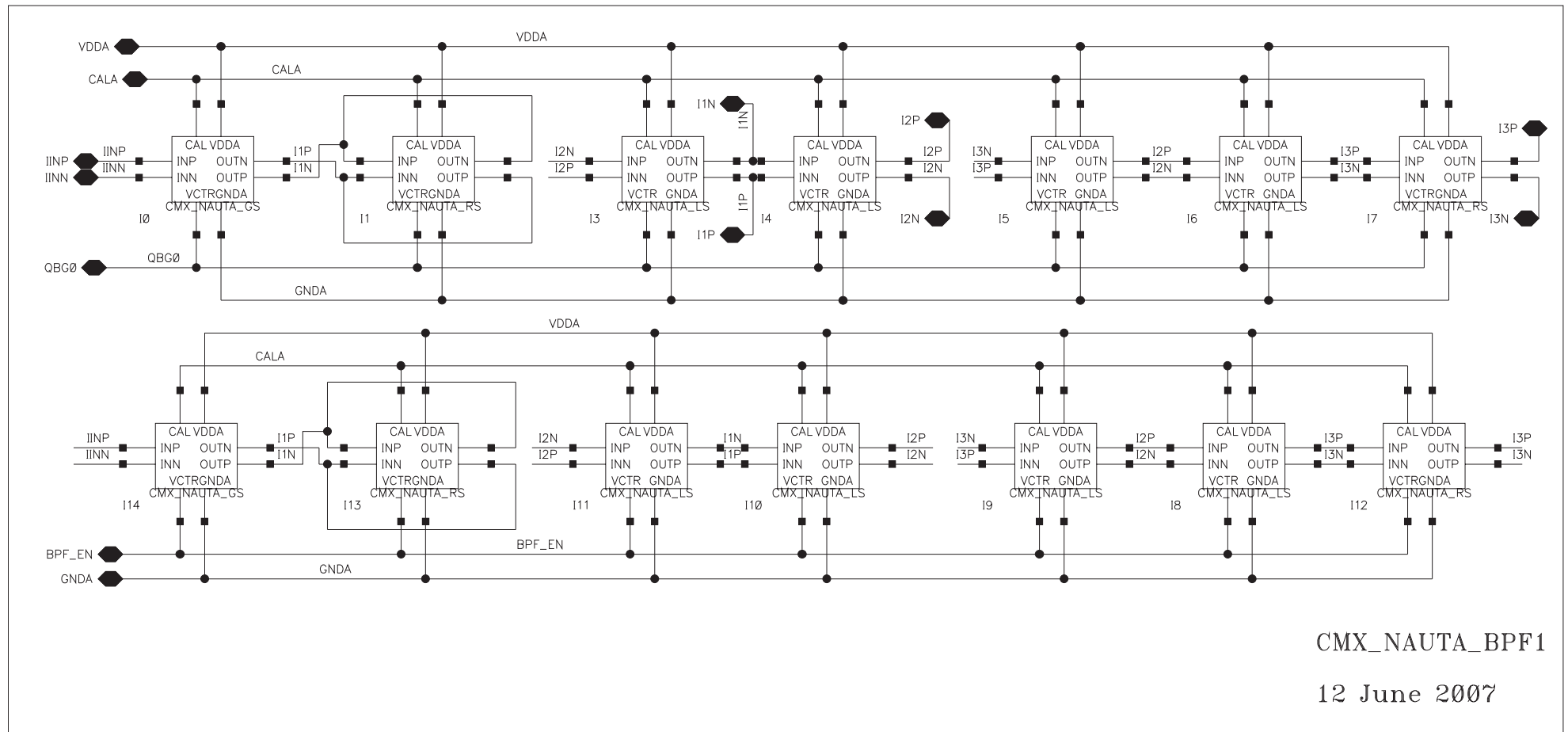
12 June 2007





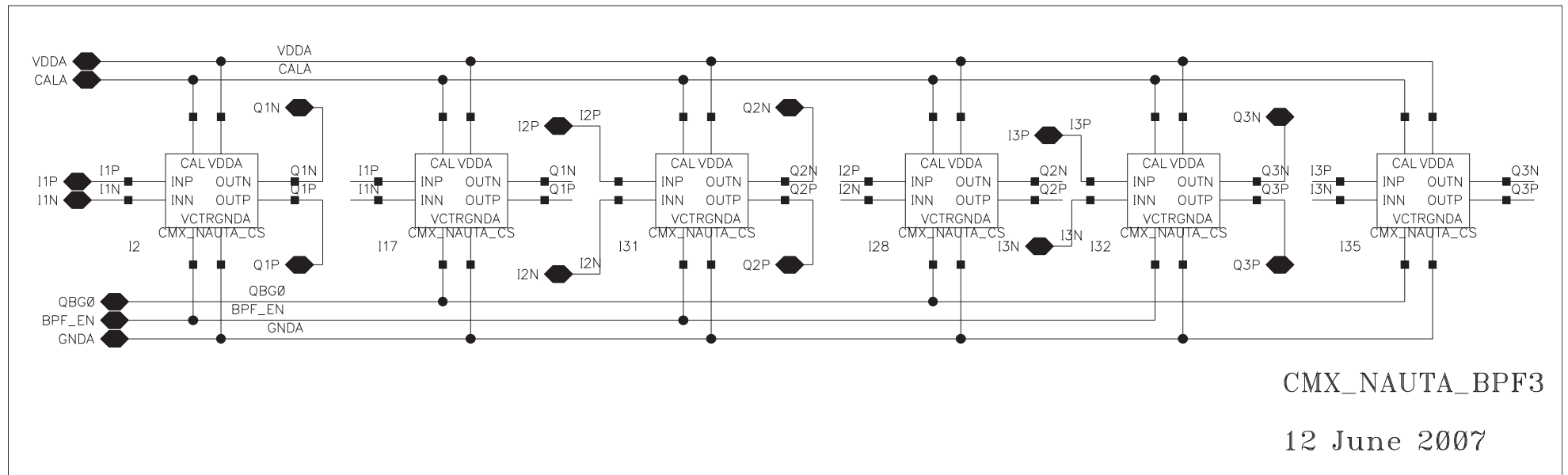
CMX\_INVS3

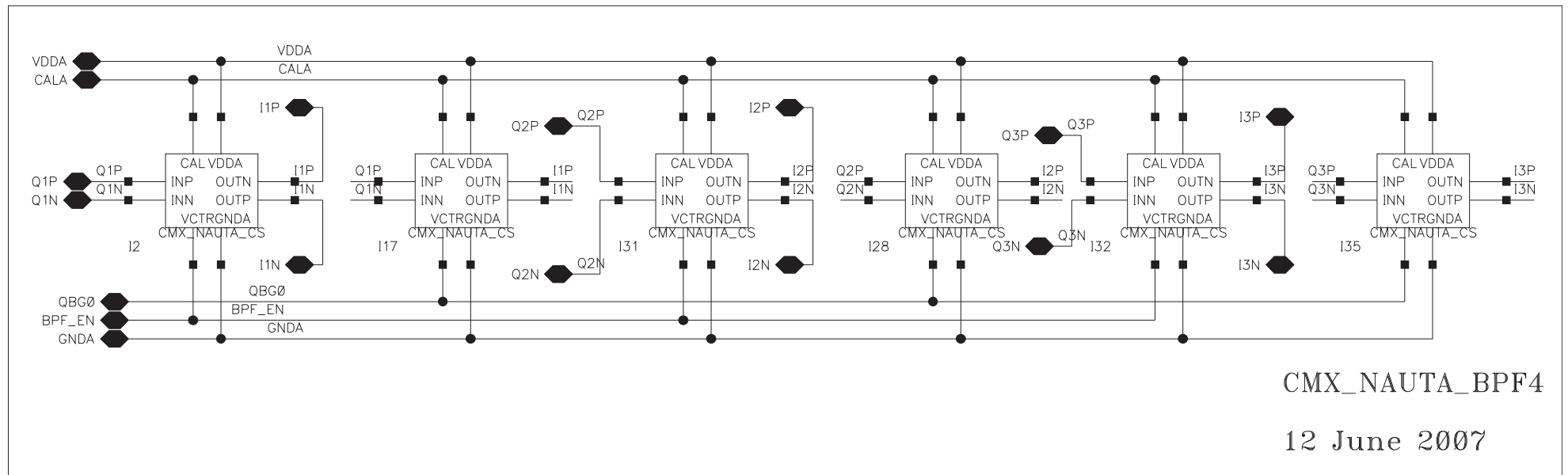
12 June 2007

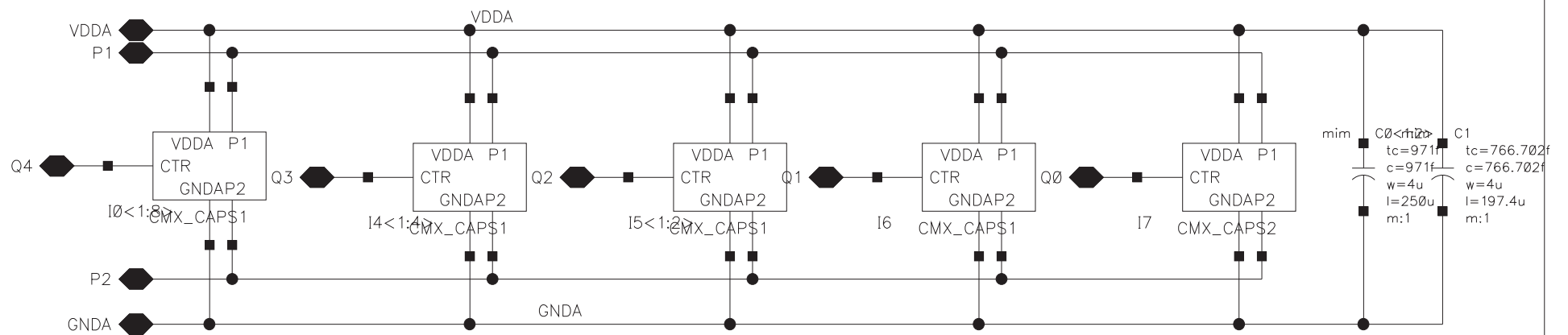


CMX\_NAUTA\_BPF1

12 June 2007

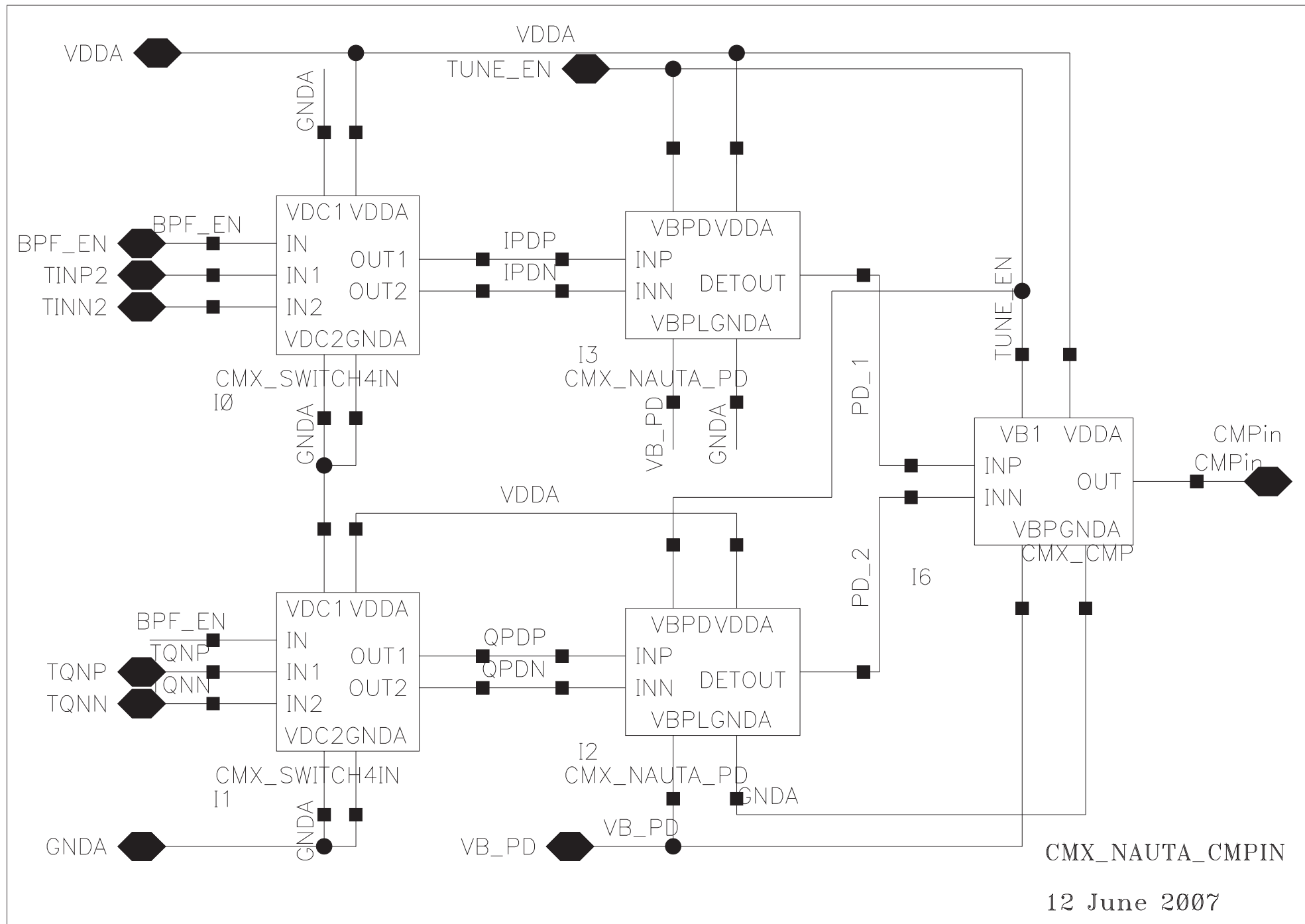


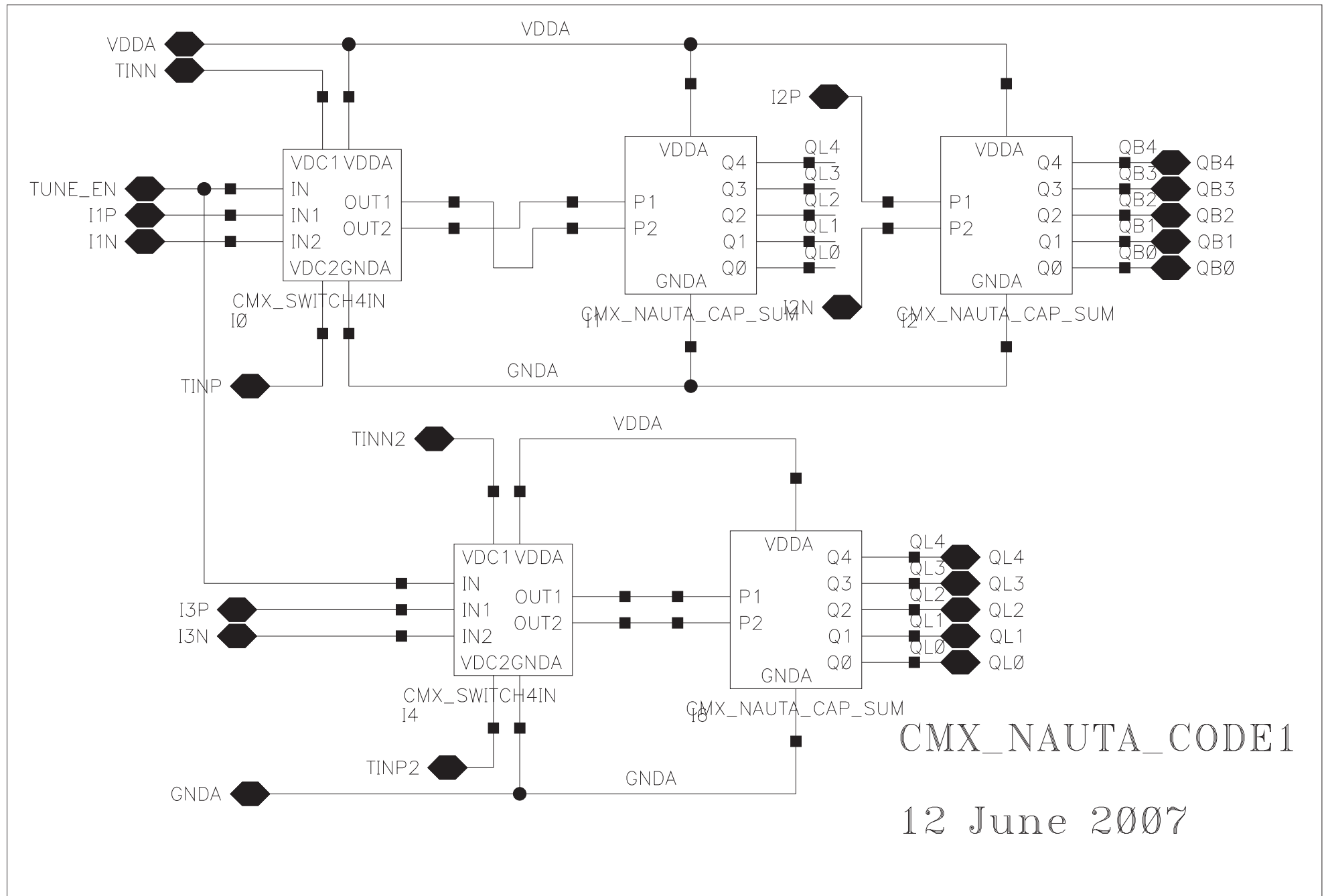


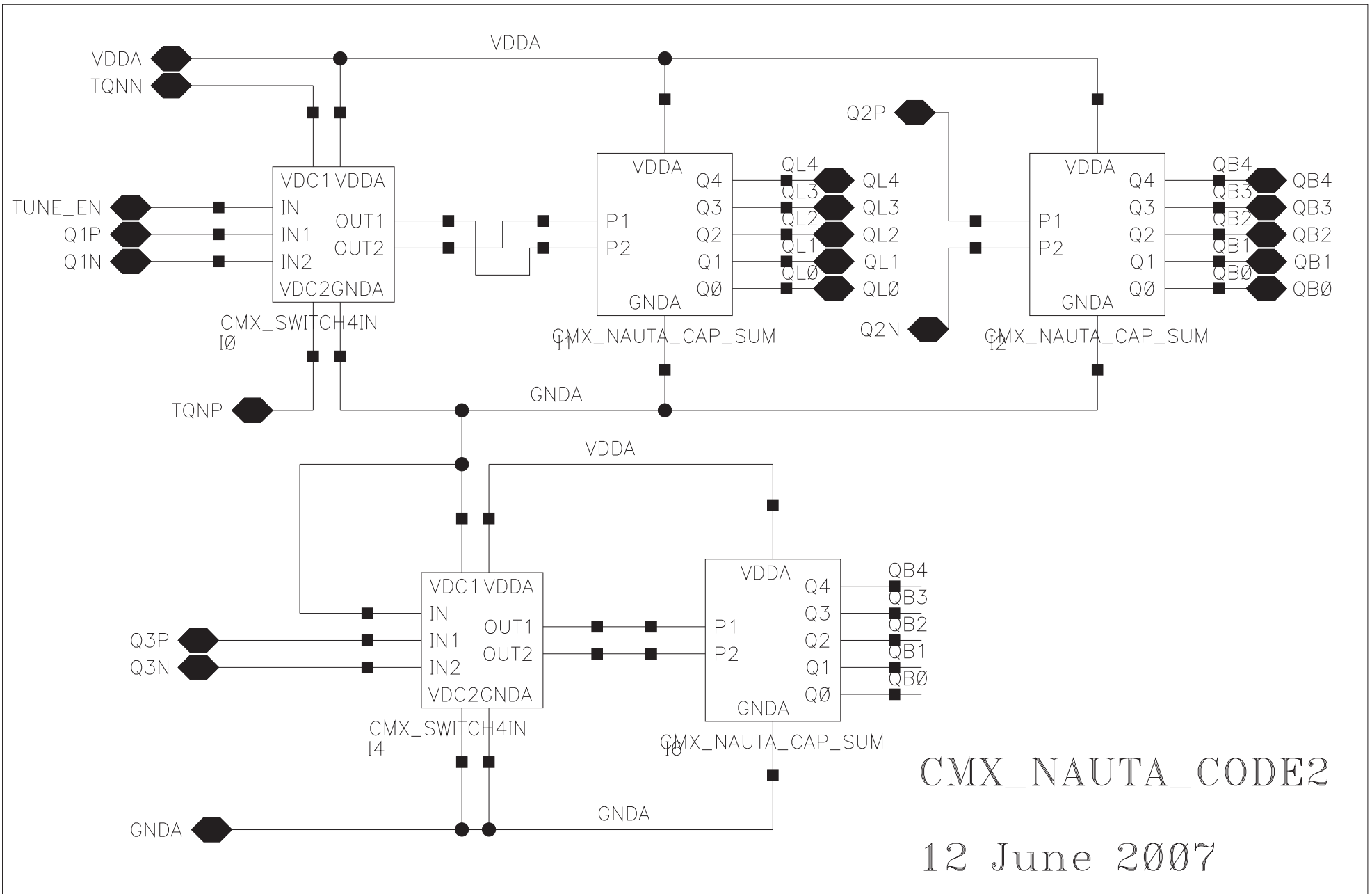


CMX\_NAUTA\_CAP\_SUM

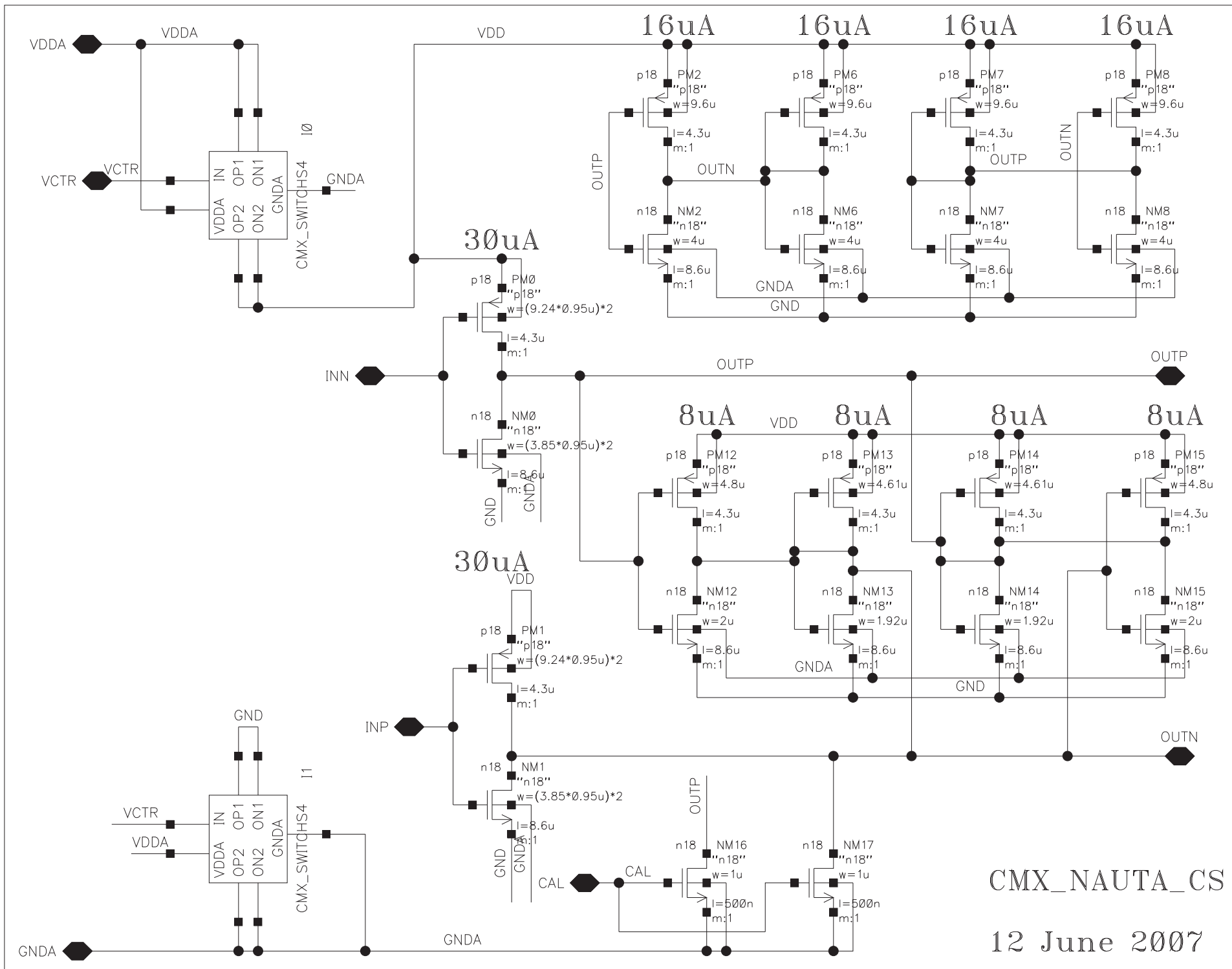
12 June 2007

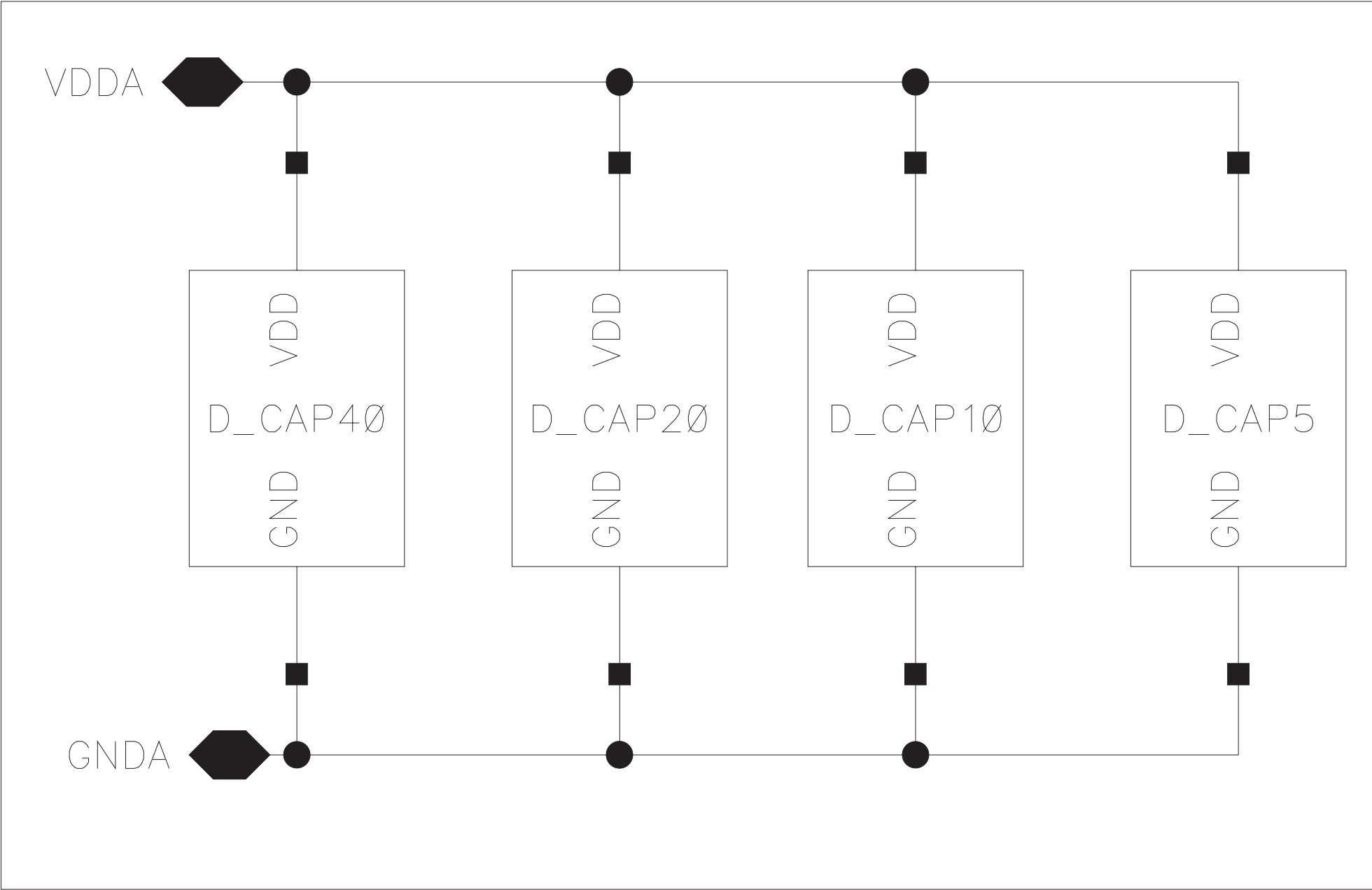


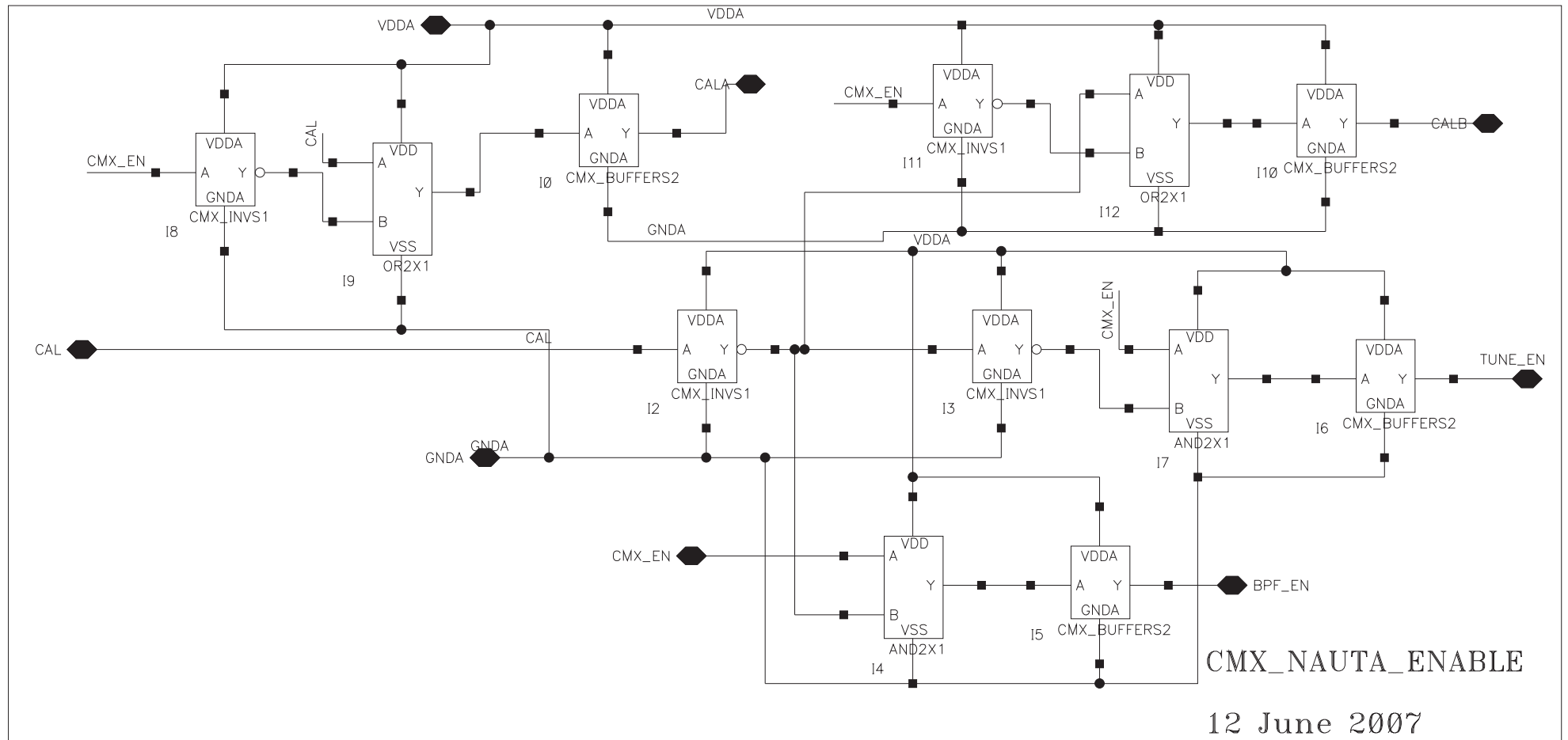


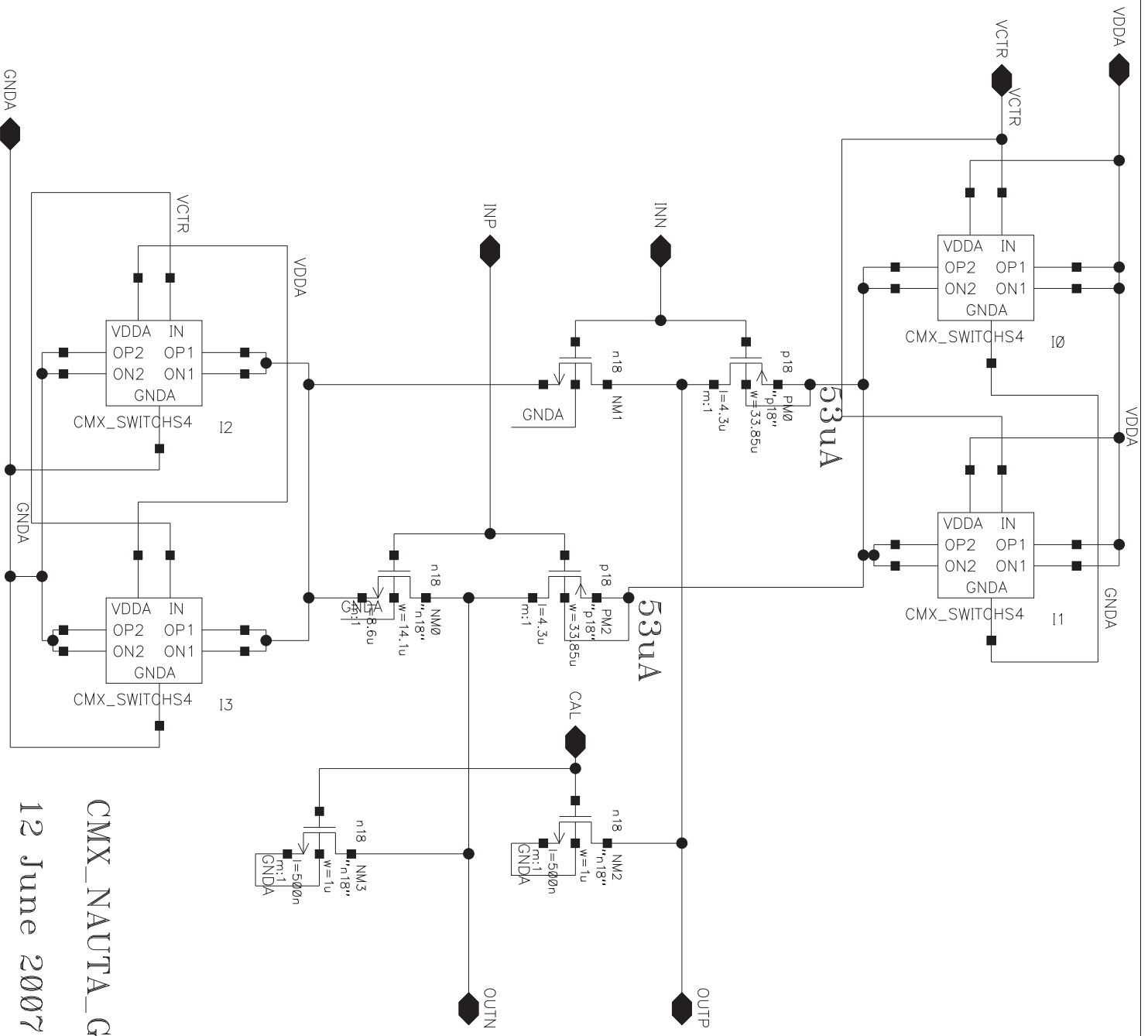






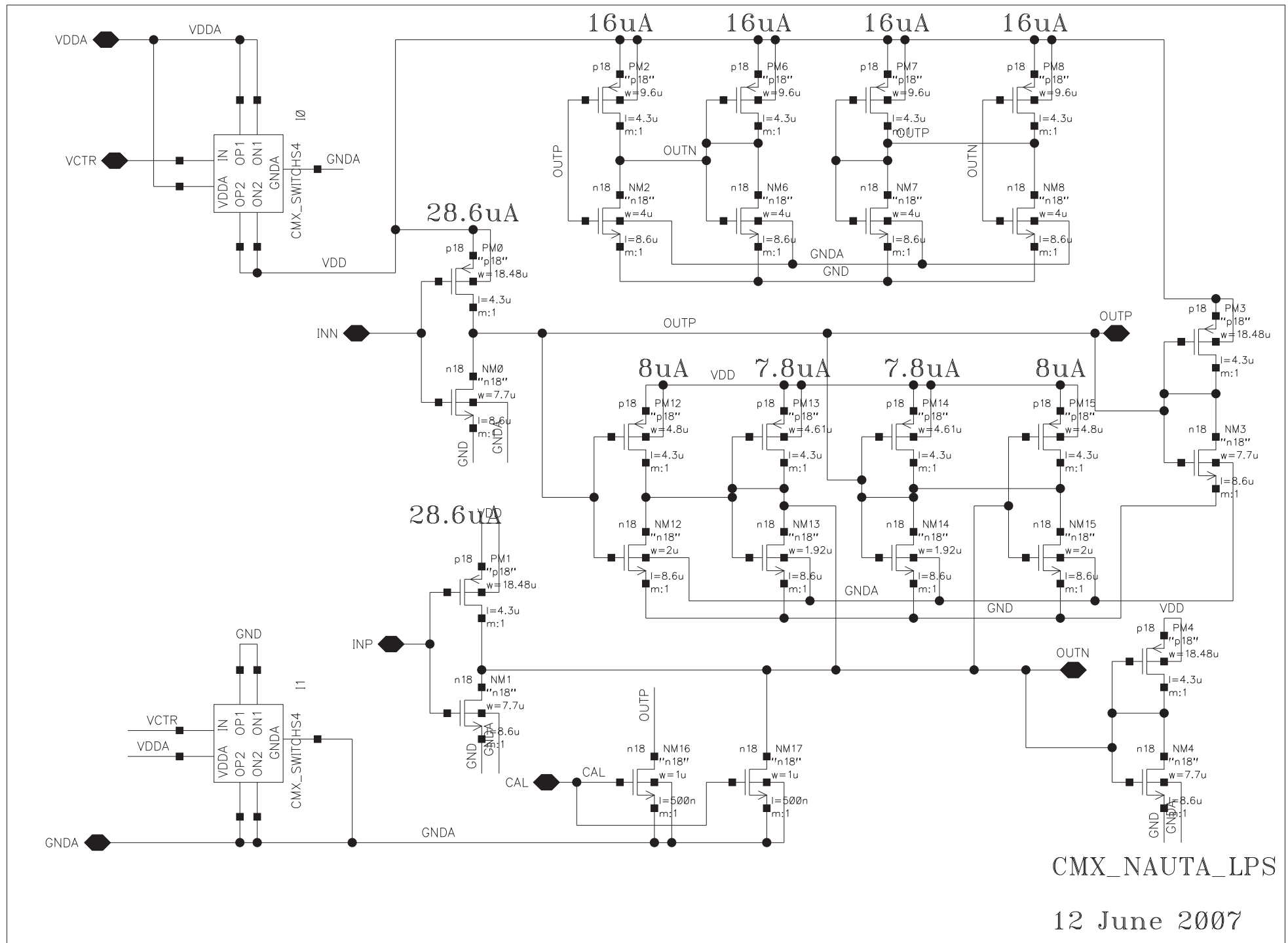


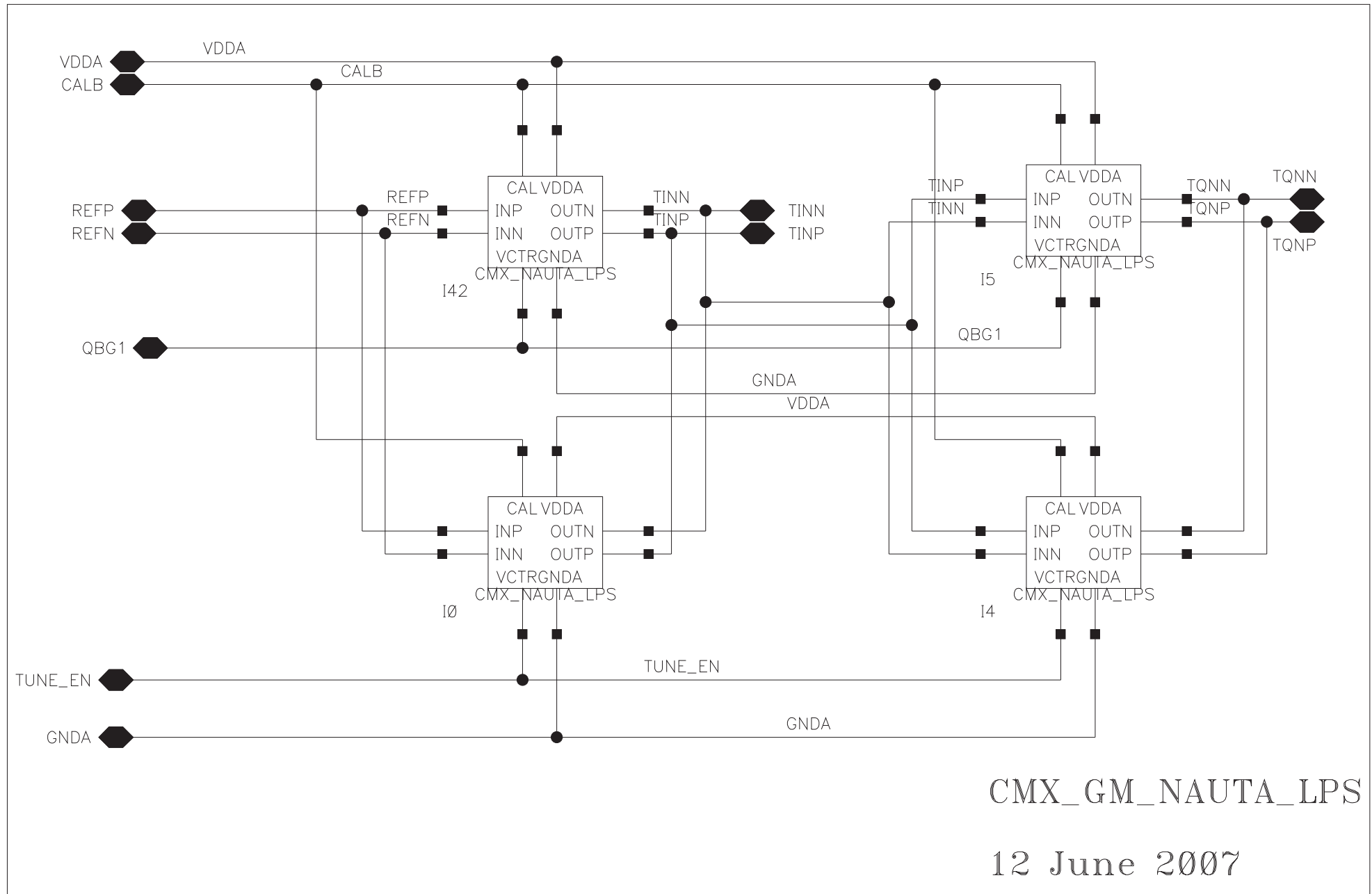




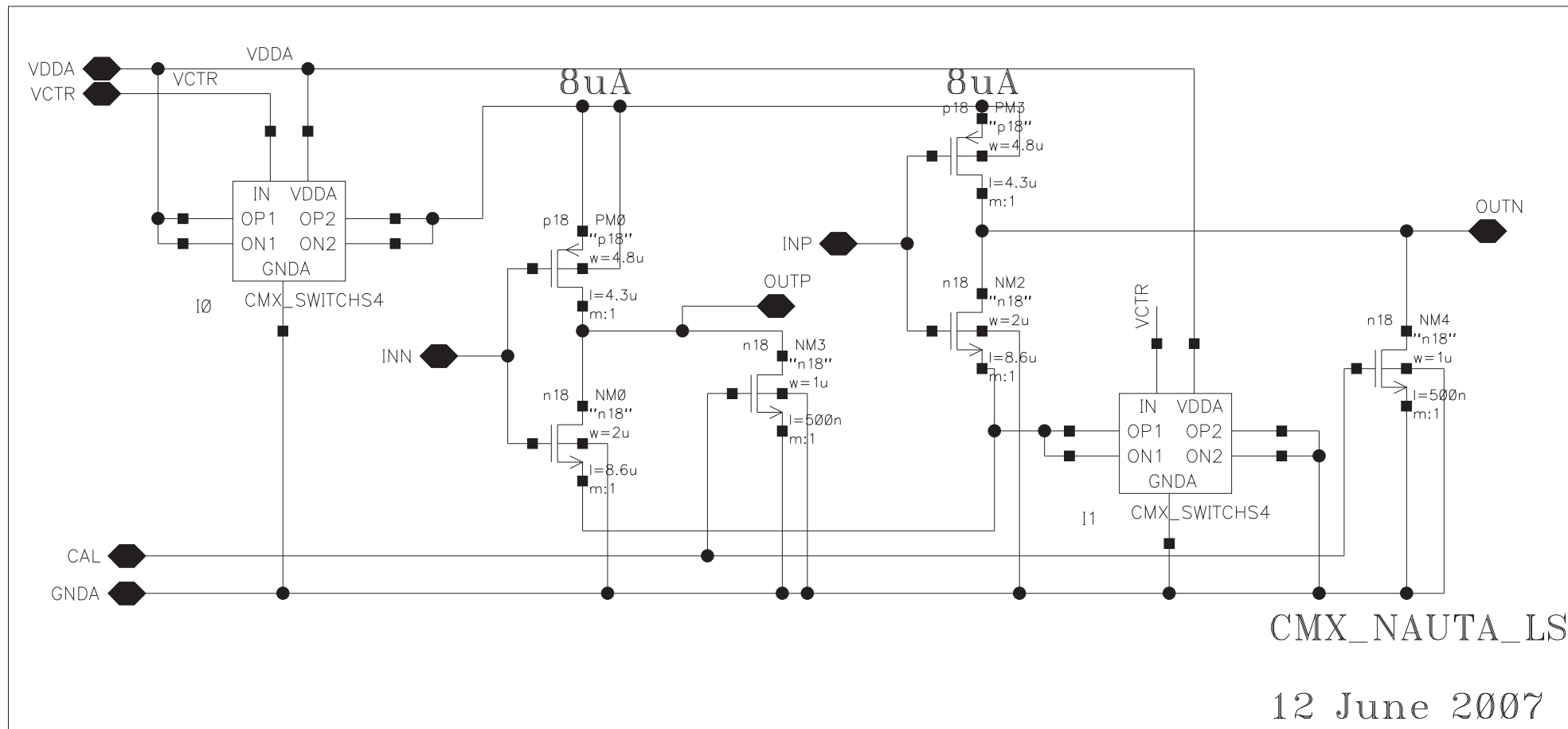
CMX\_NAUTA\_GS

12 June 2007



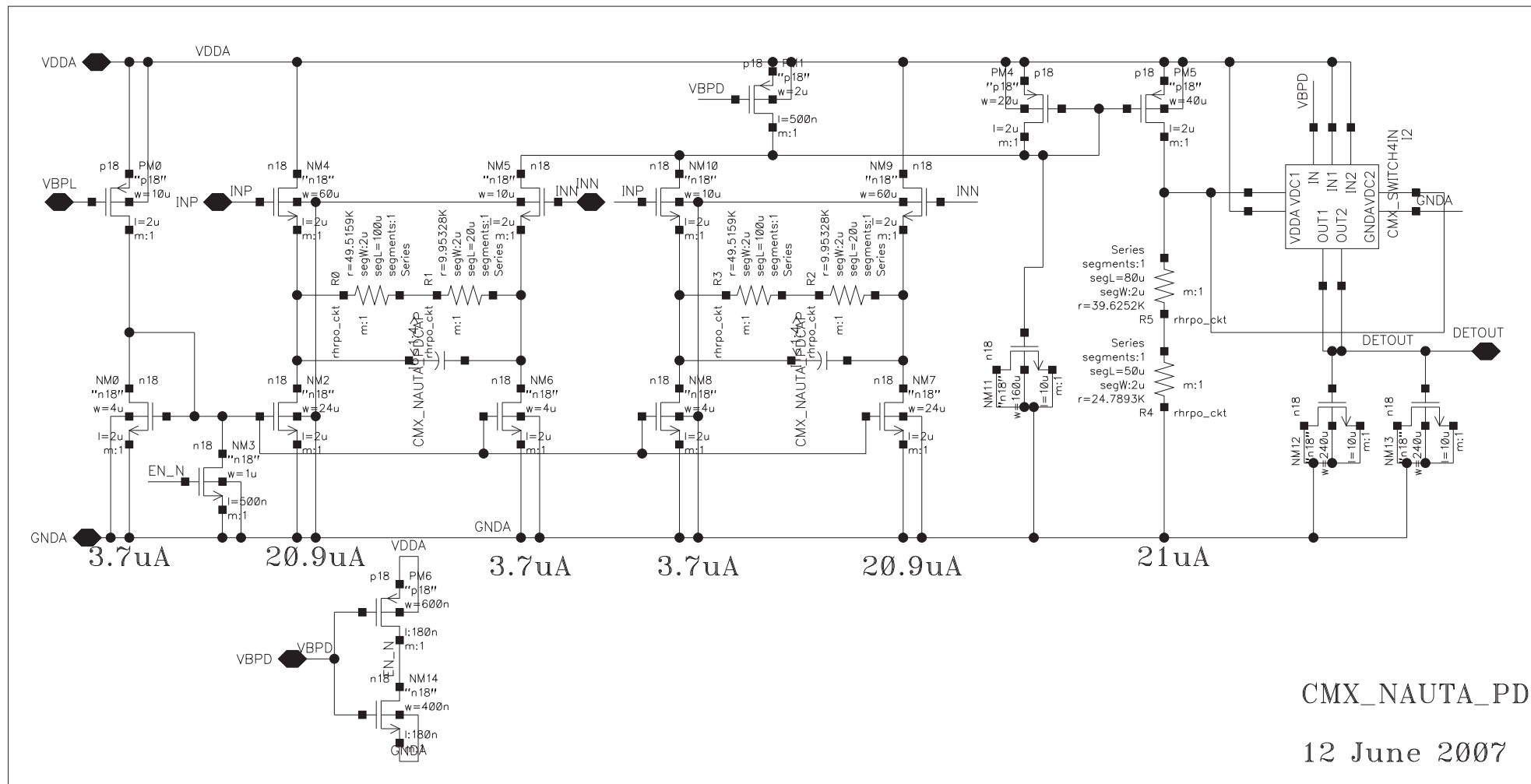












CMX\_NAUTA\_PD

12 June 2007

P1



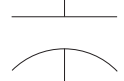
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w=30u  
c=873.9f  
tc=873.9f



C1

mim

mim



C0

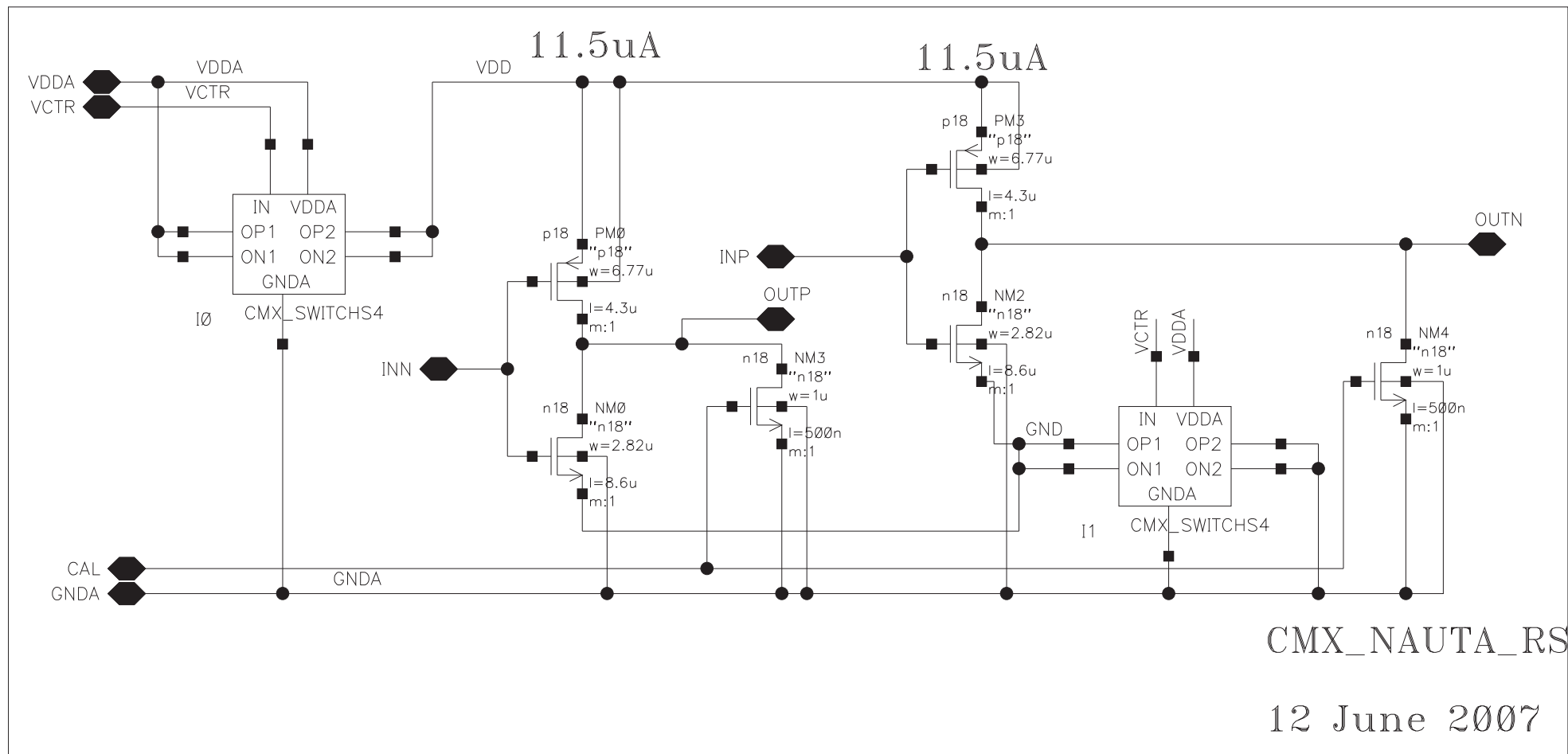
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l=30u  
m:1

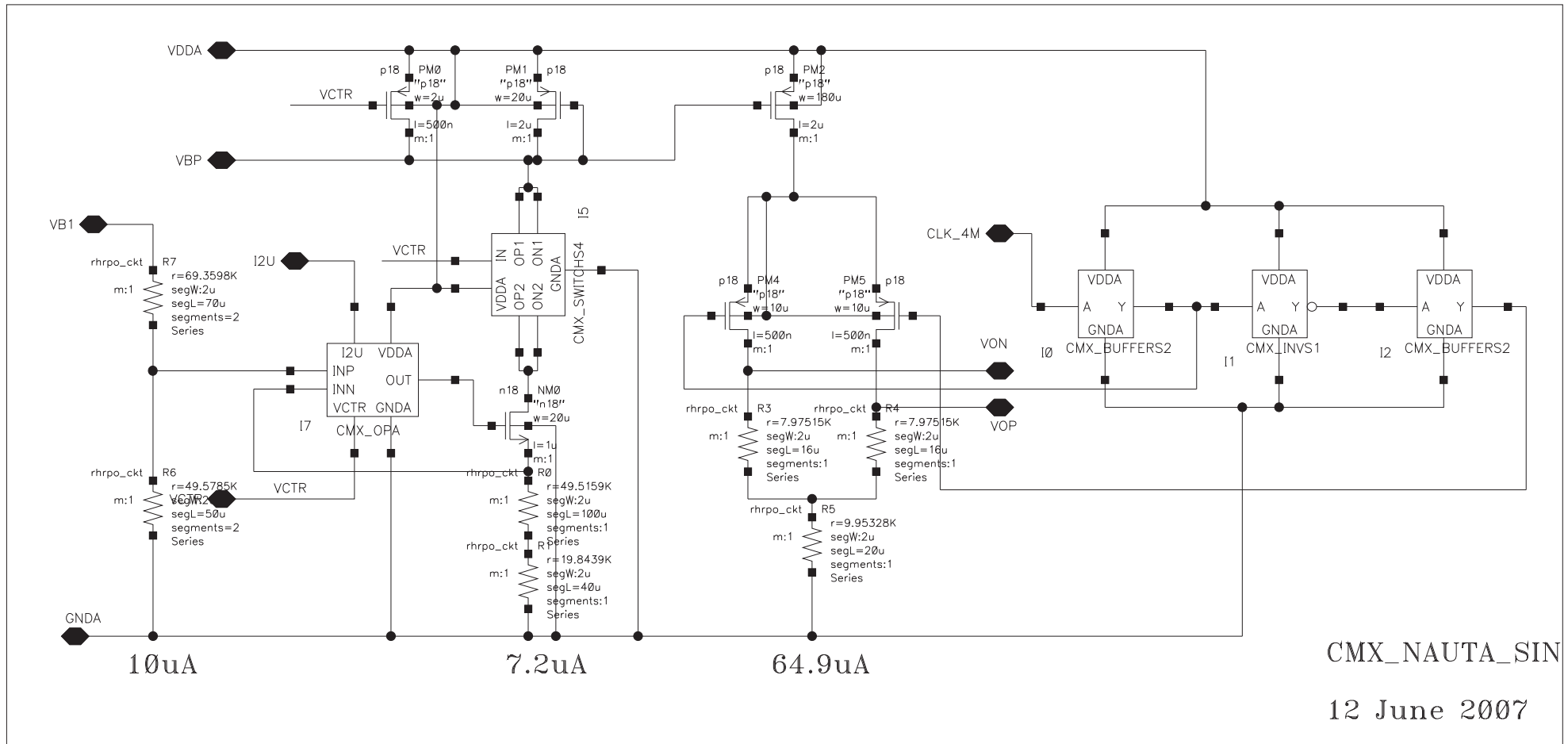
P2



CMX\_NAUTA\_PDCCAP

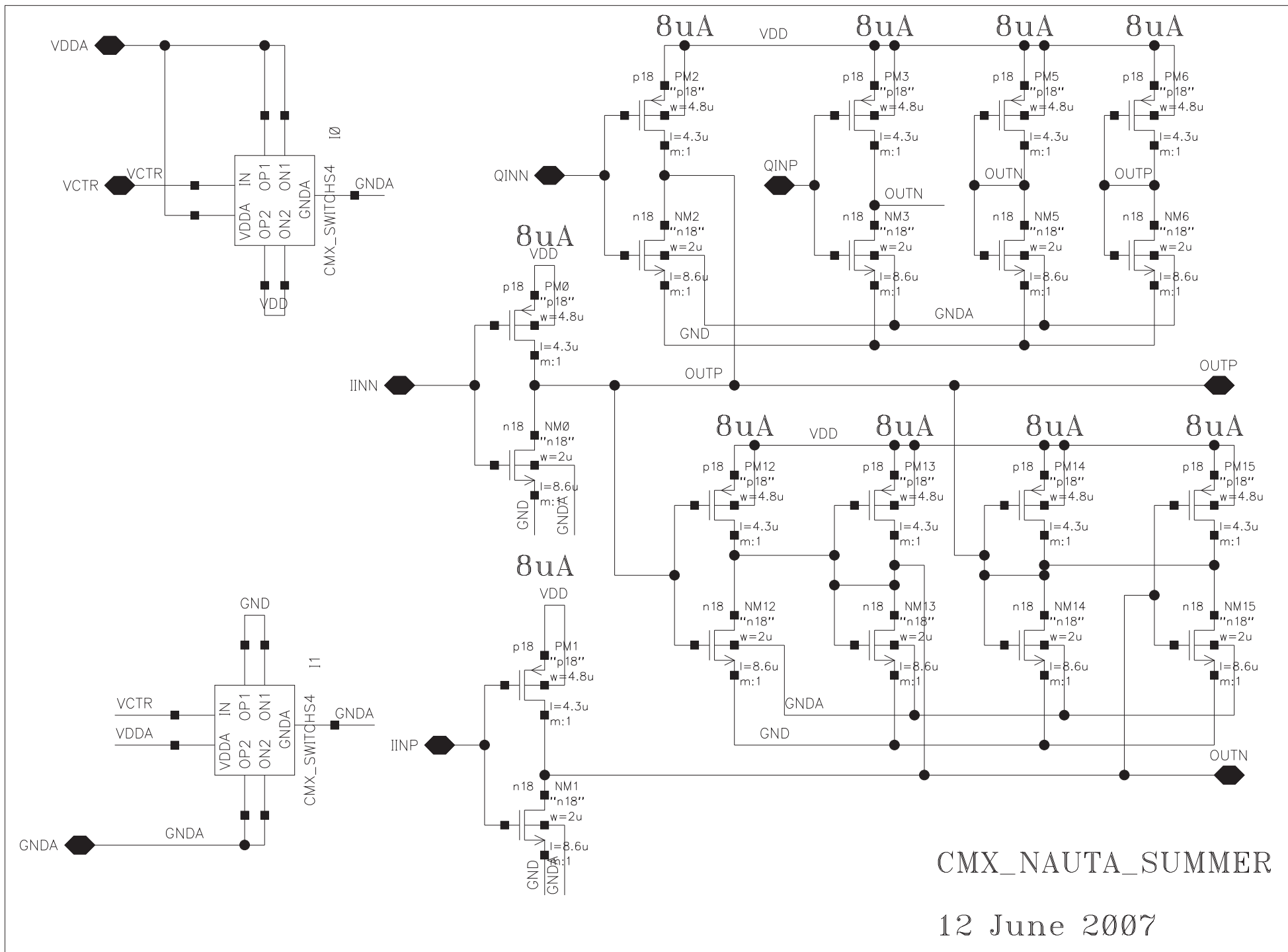
2 May 2006

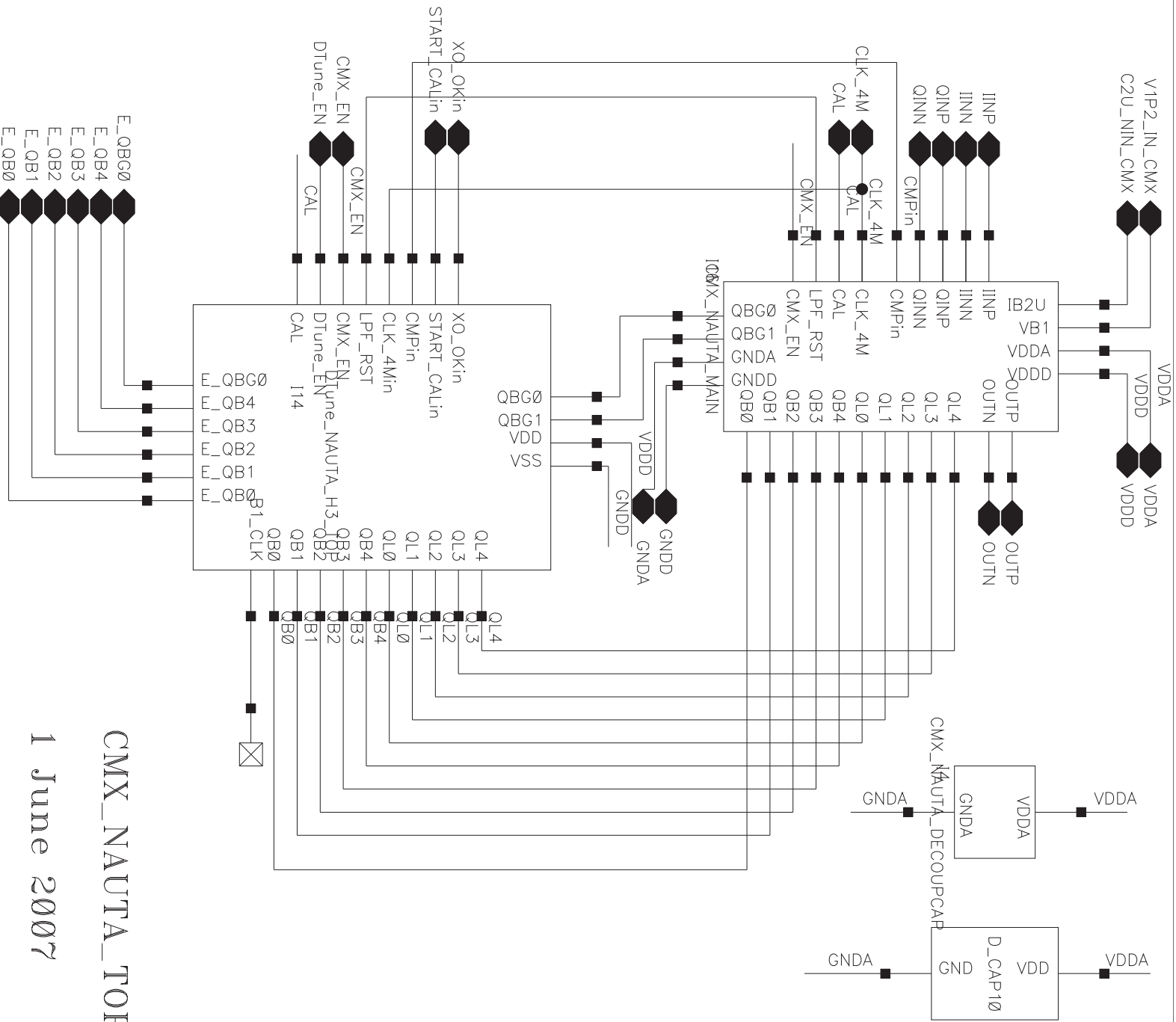




CMX\_NAUTA\_SIN

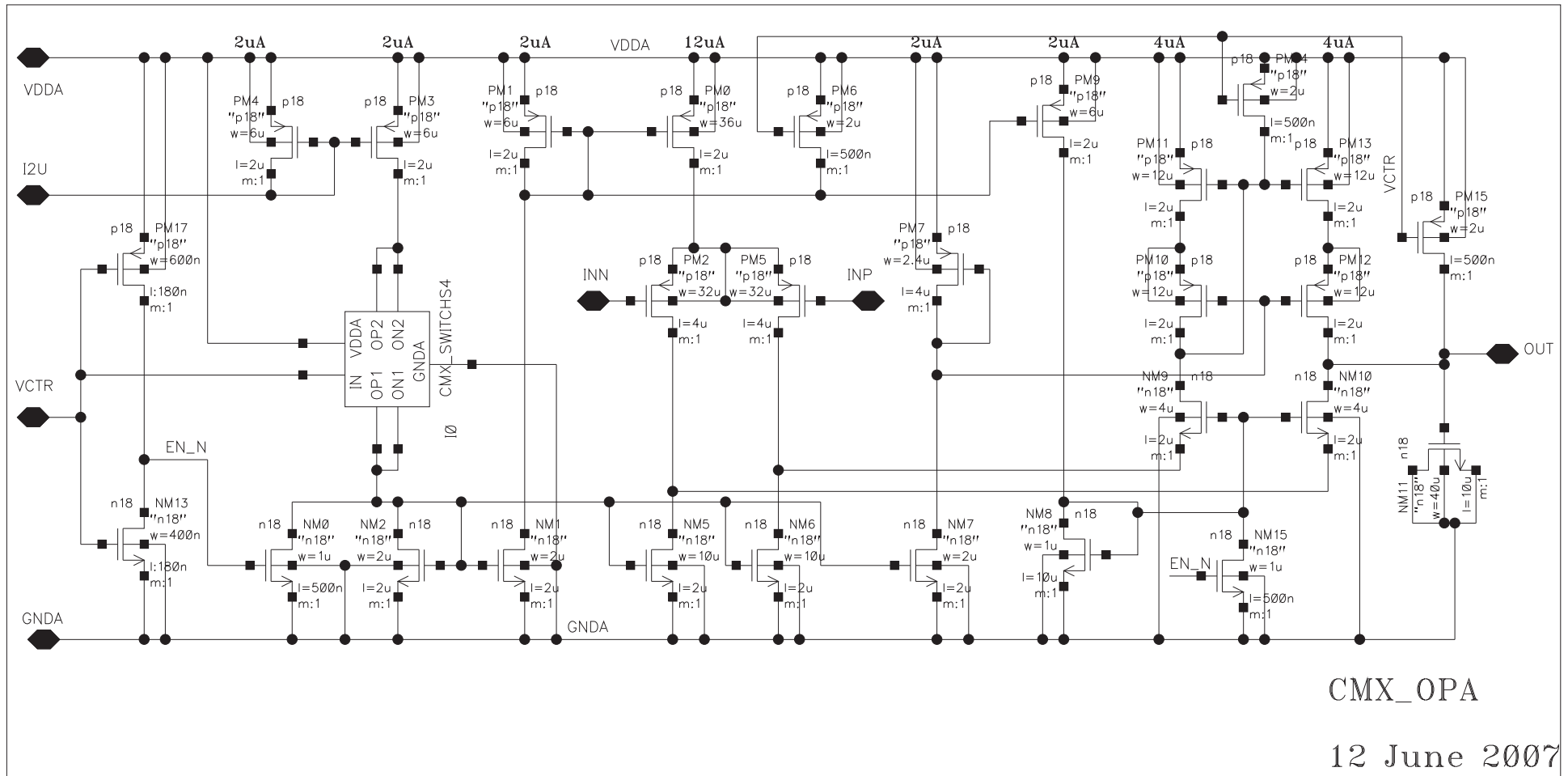
12 June 2007



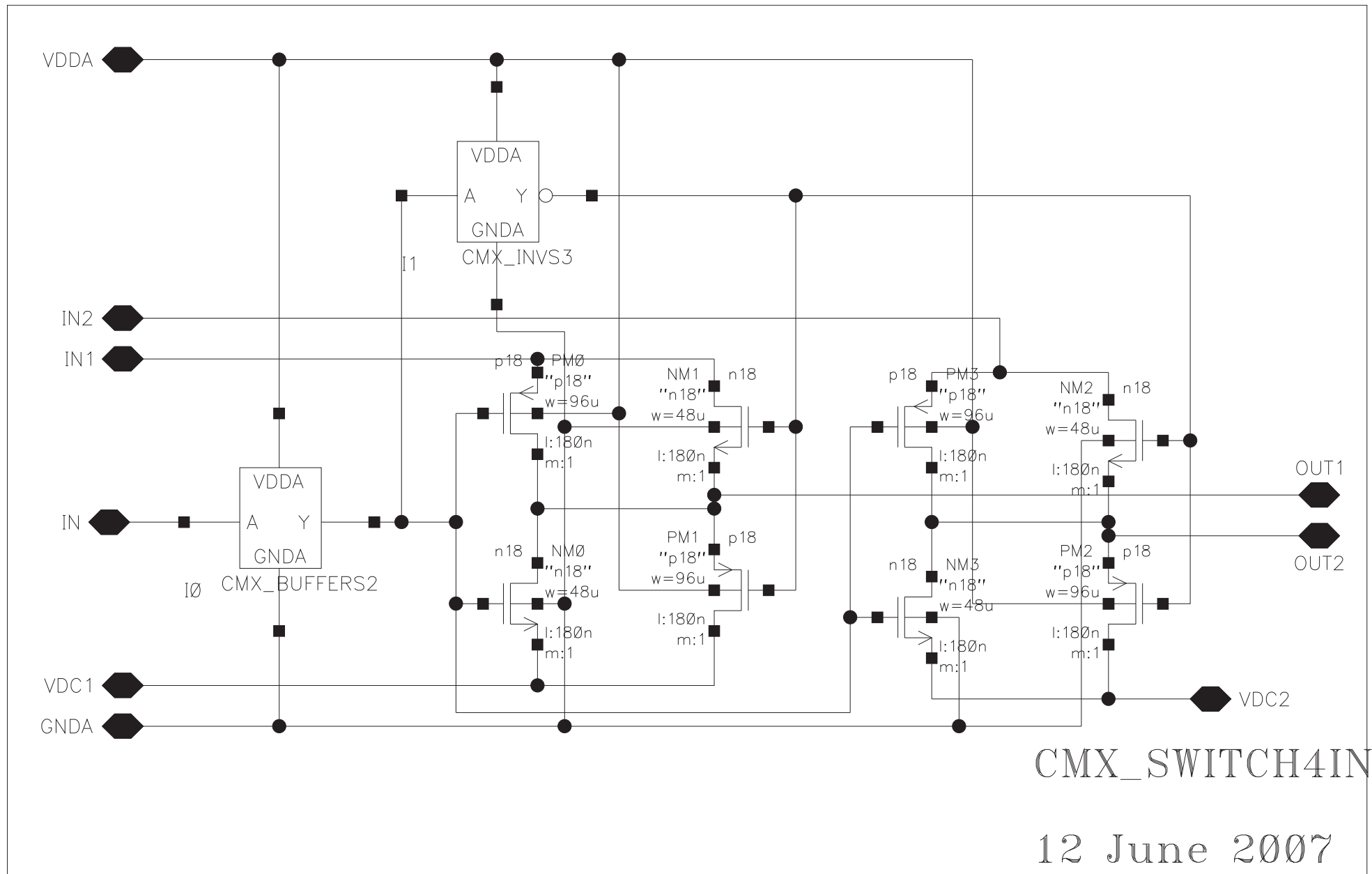


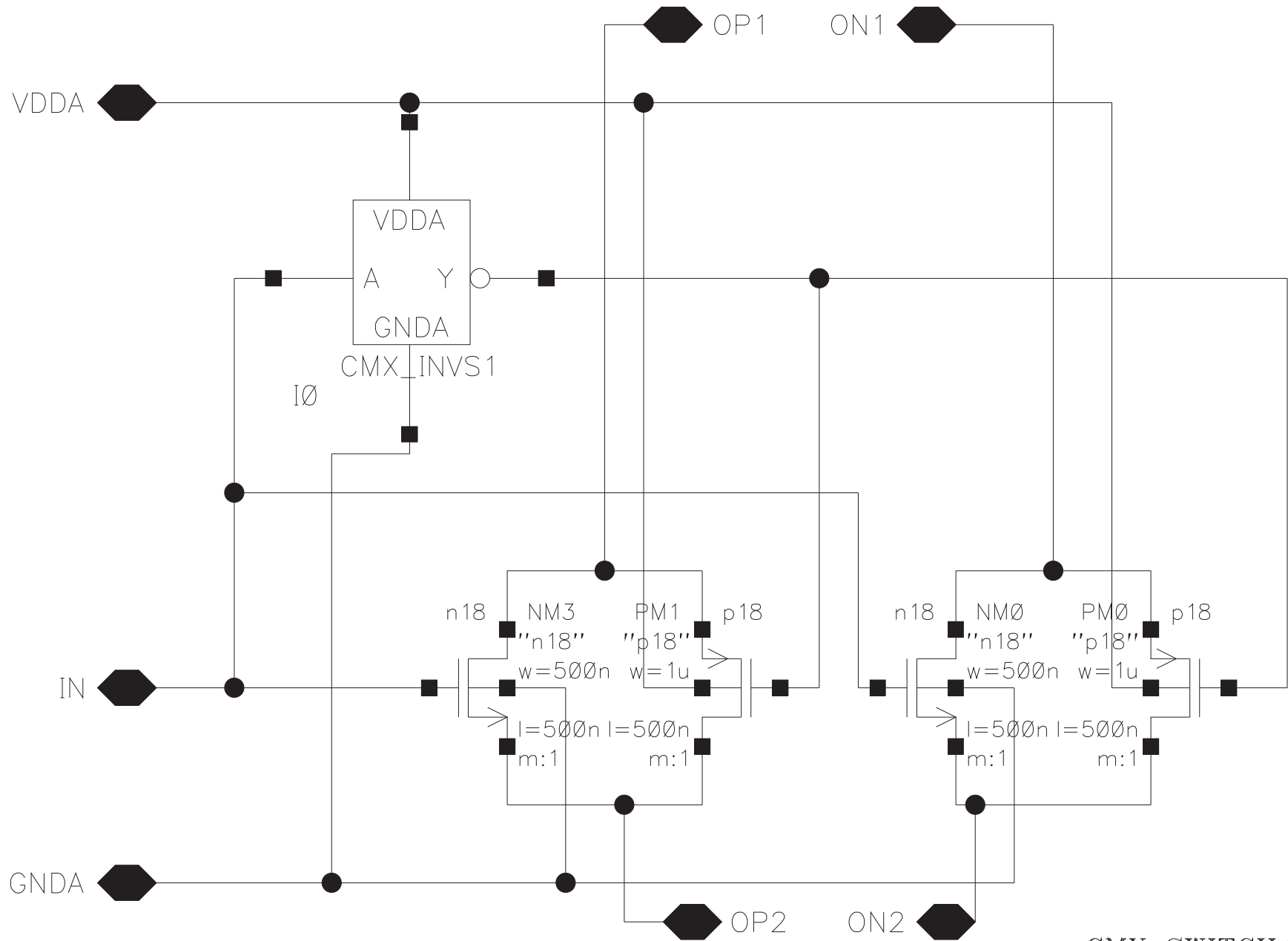
CMX\_NAUTA\_TOP

1 June 2007



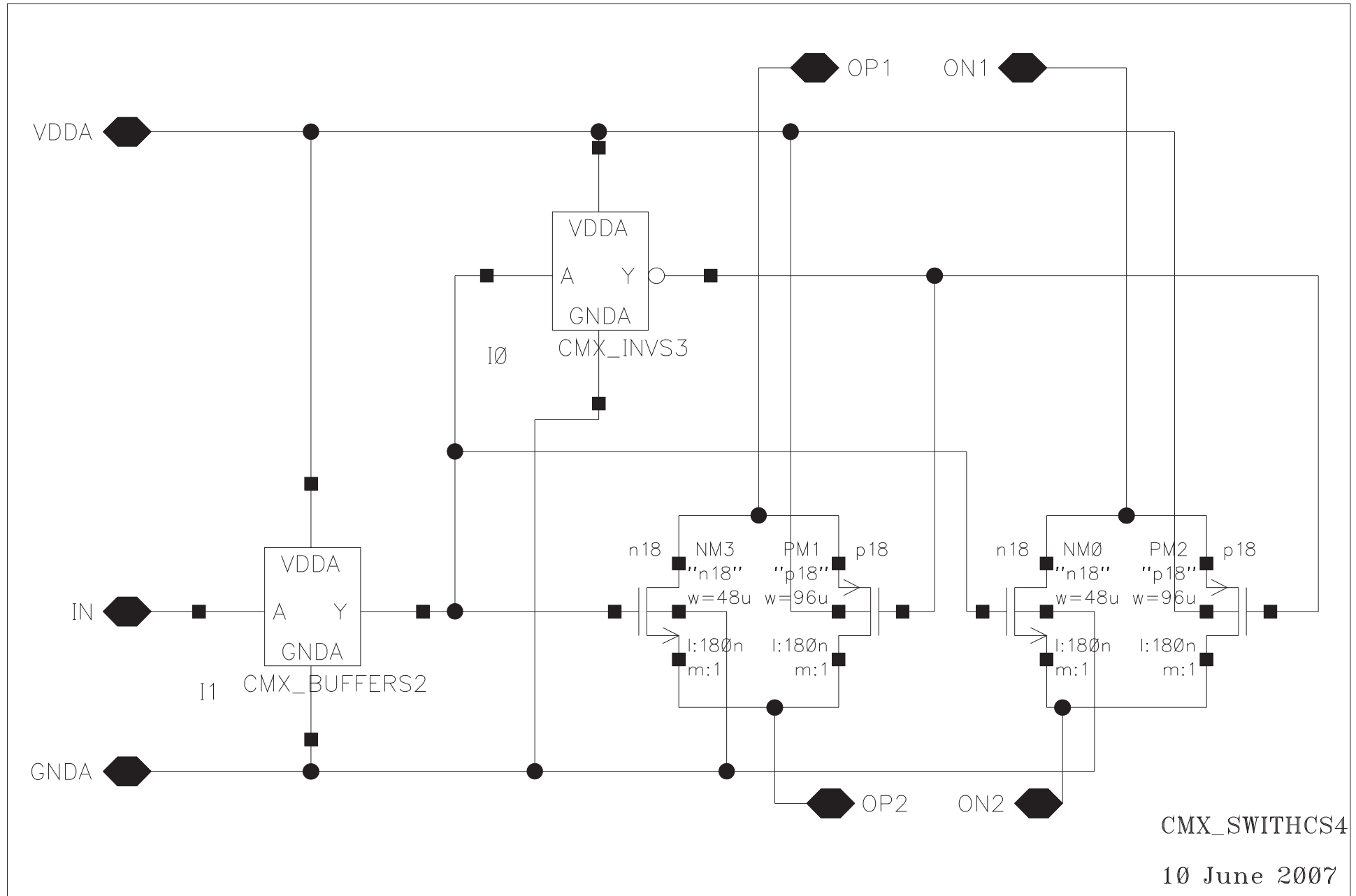


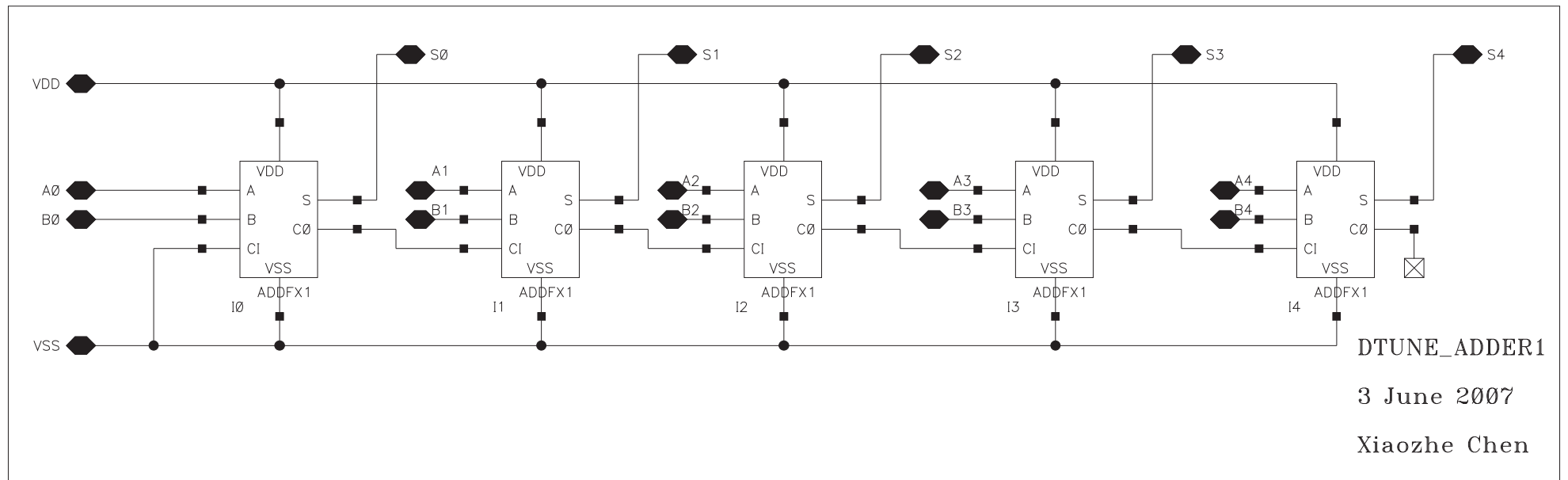


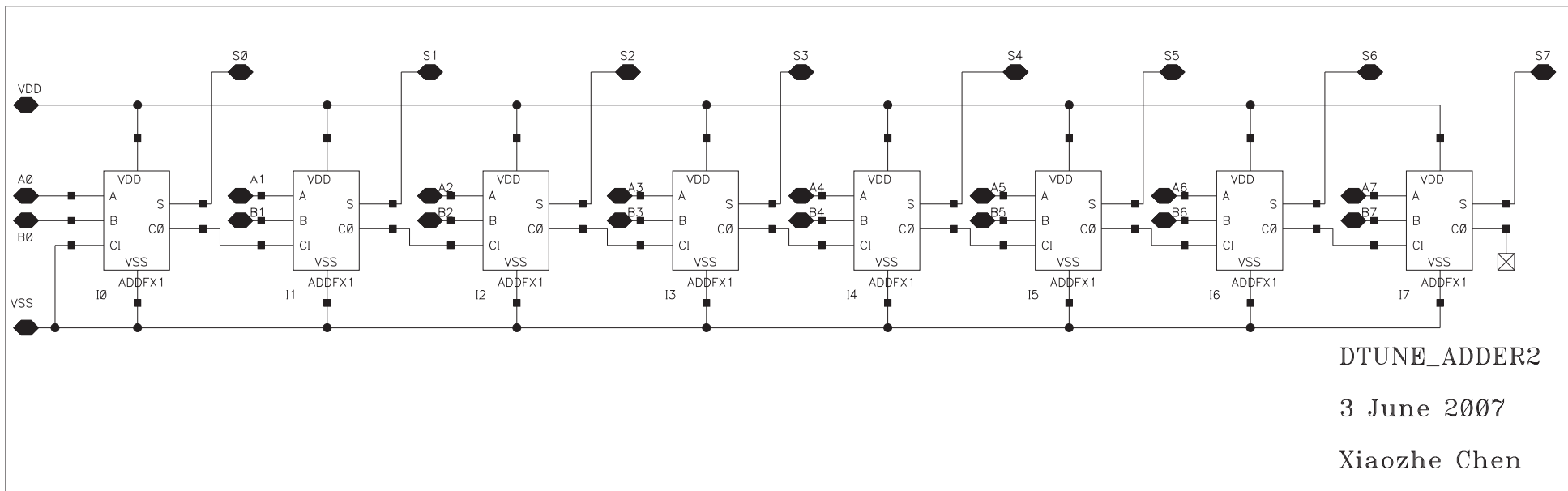


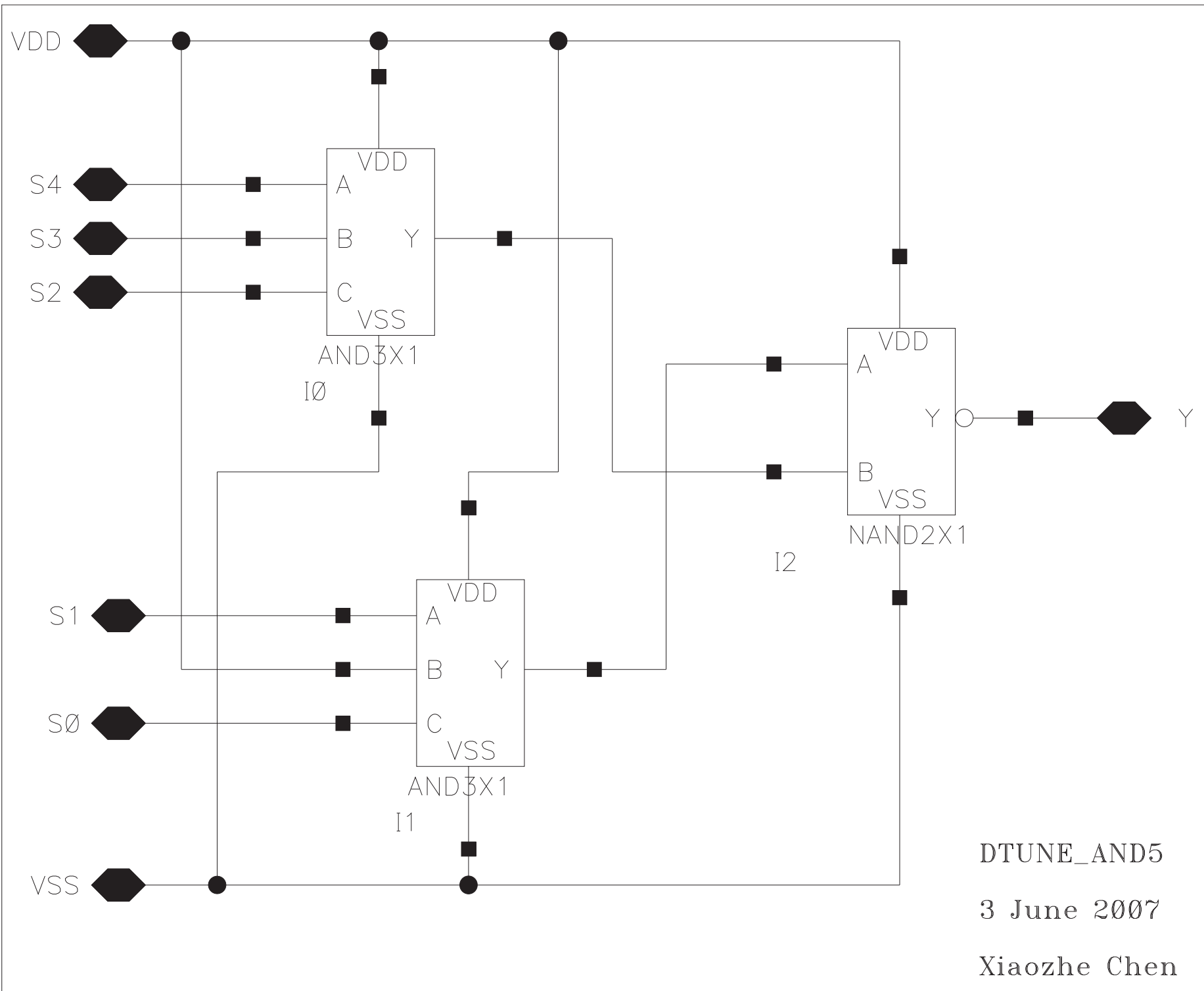
CMX\_SWITCH4LP

12 June 2007





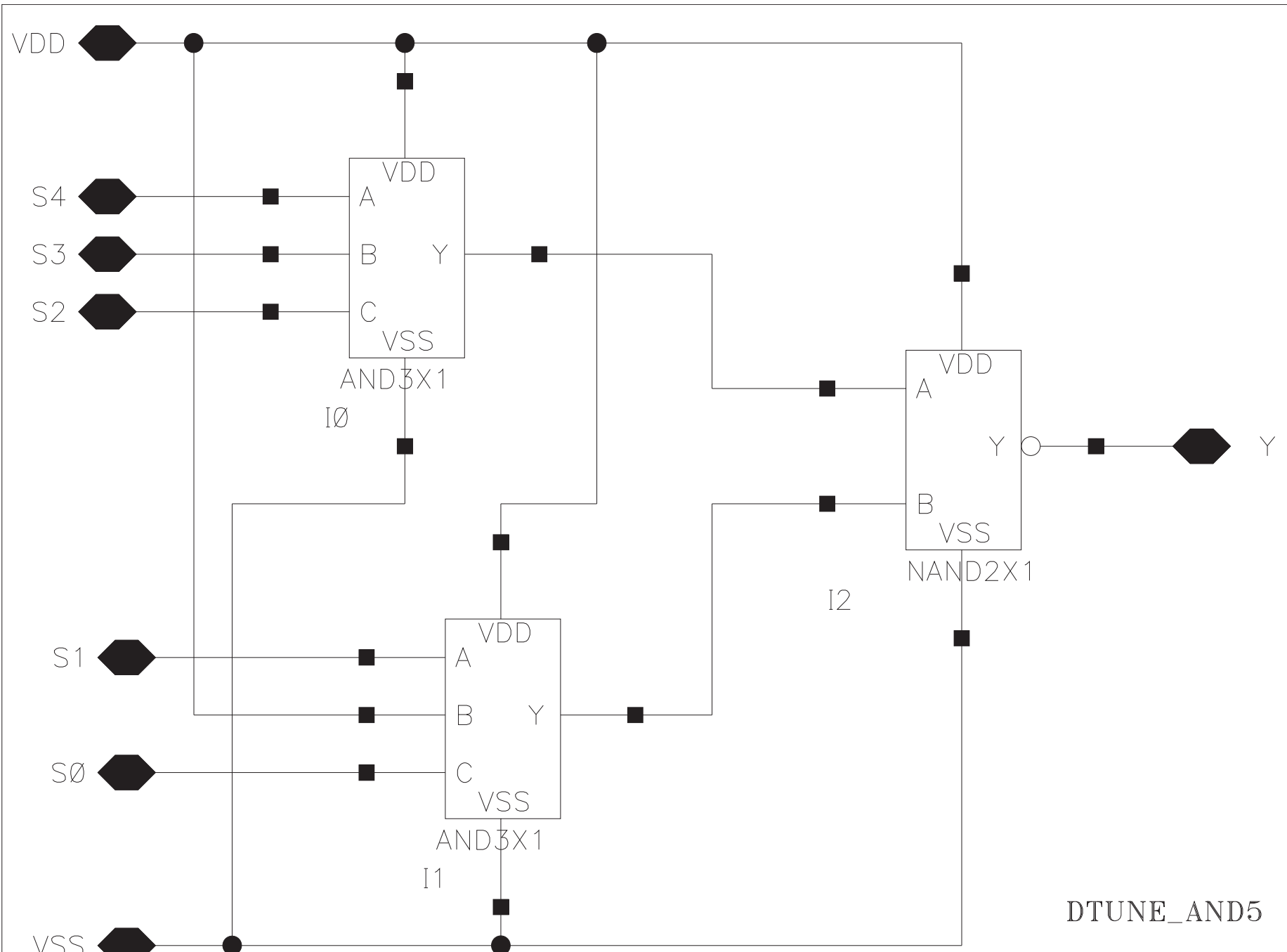




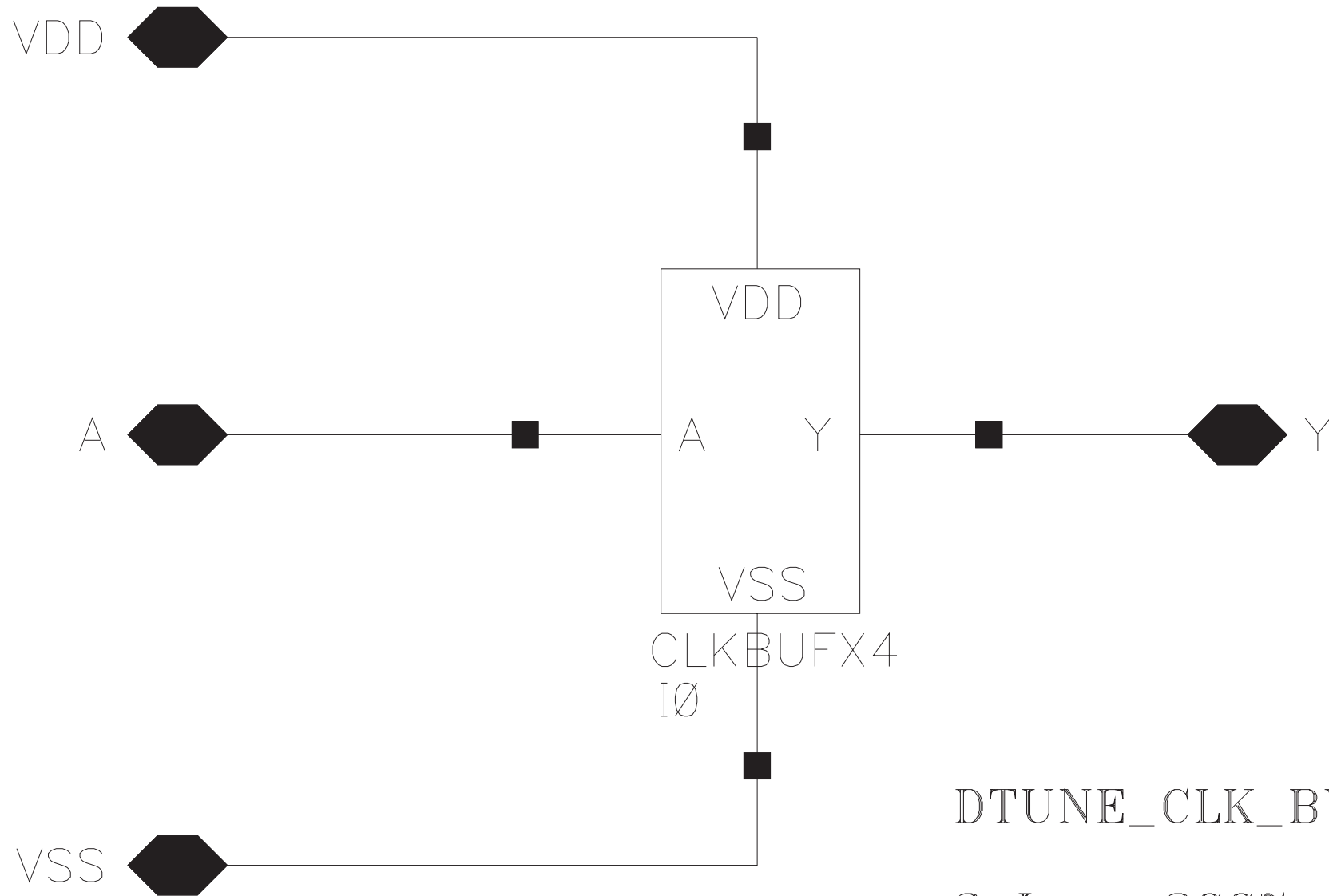
DTUNE\_AND5

3 June 2007

Xiaozhe Chen



DTUNE\_AND5  
 3 June 2007  
 Xiaozhe Chen

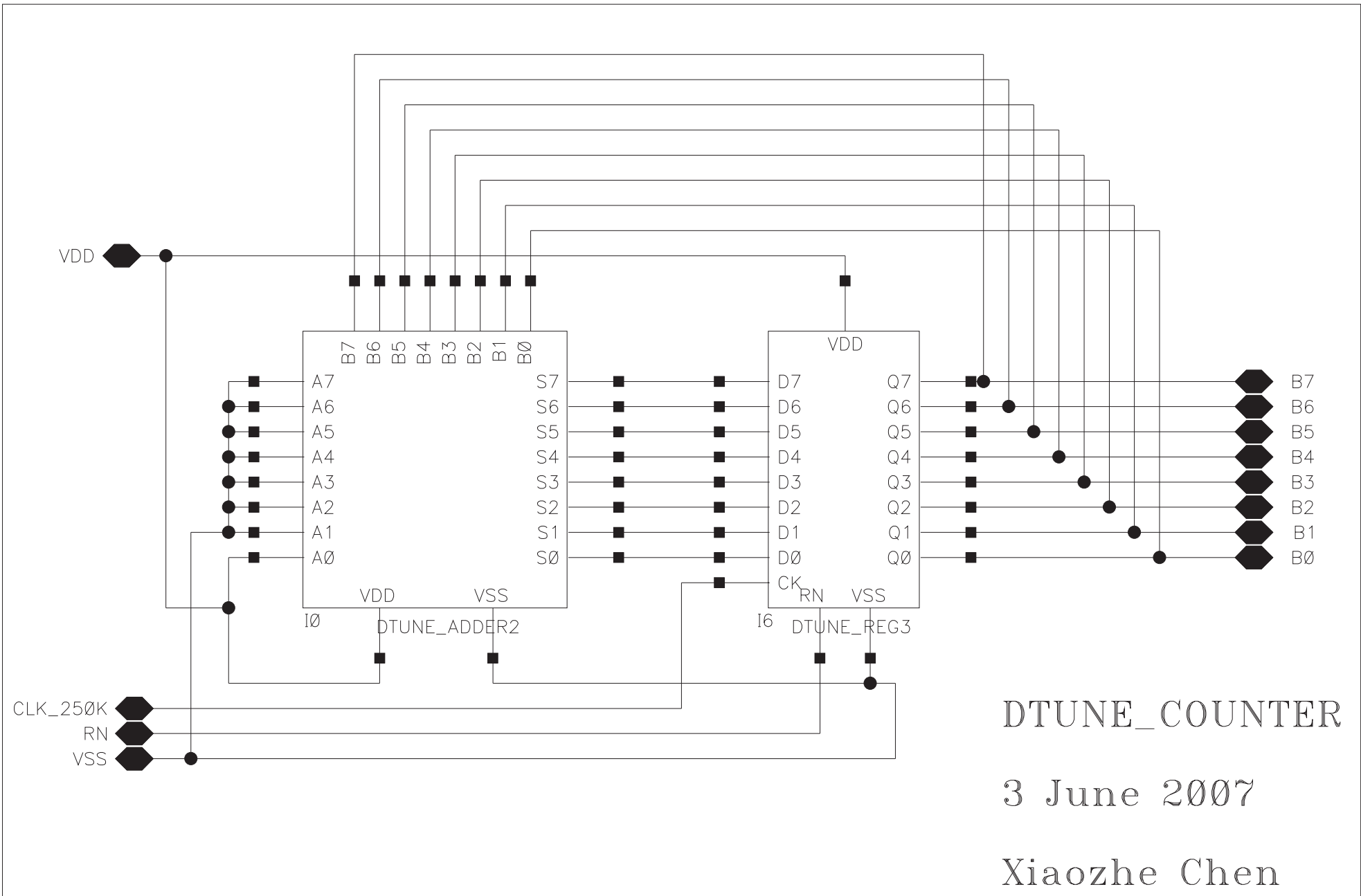


DTUNE\_CLK\_BUFFER

3 June 2007

Xiaozhe Chen

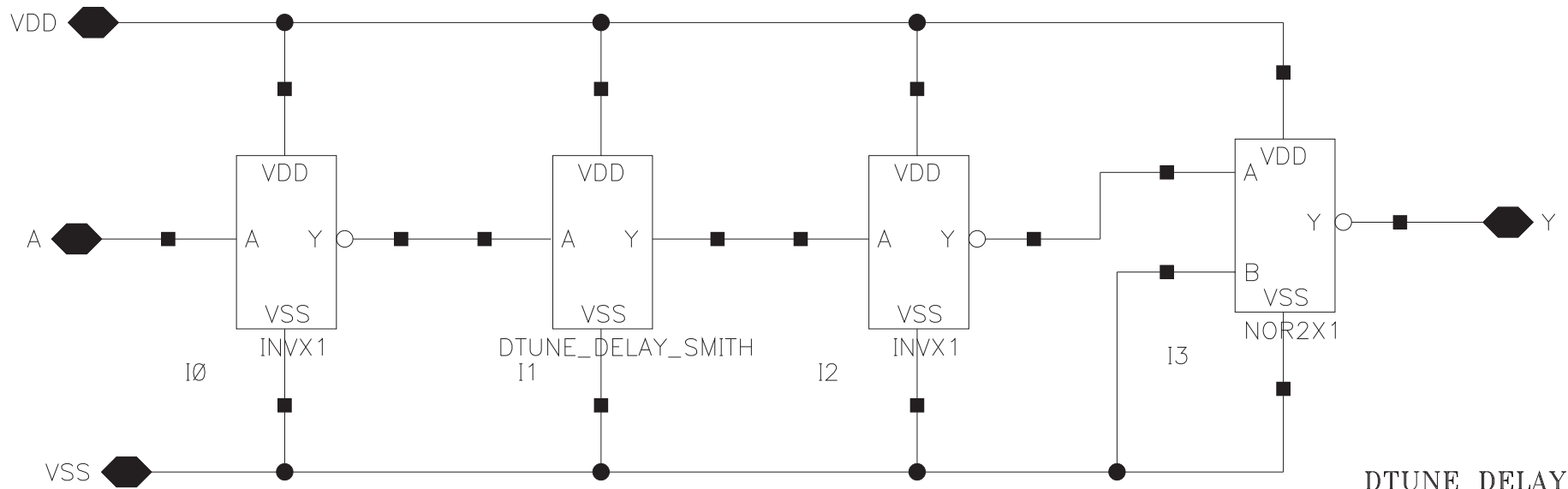




DTUNE\_COUNTER

3 June 2007

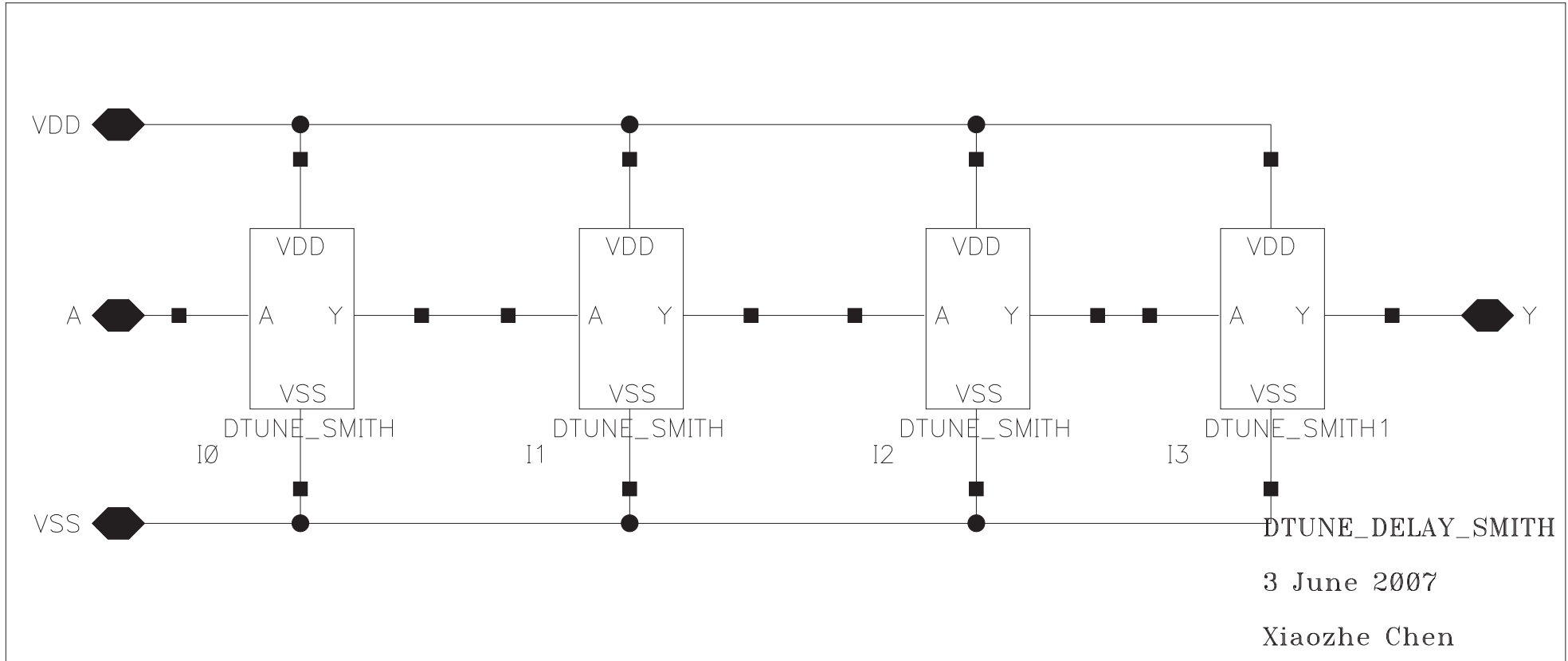
Xiaozhe Chen

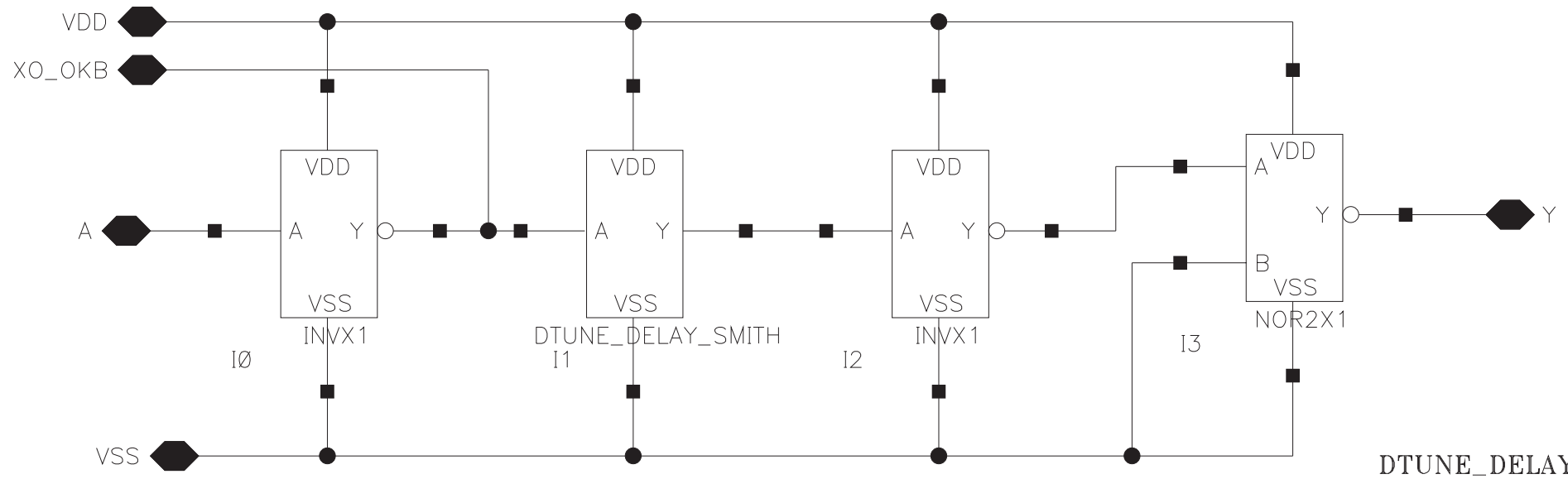


DTUNE\_DELAY

3 June 2007

Xiaozhe Chen

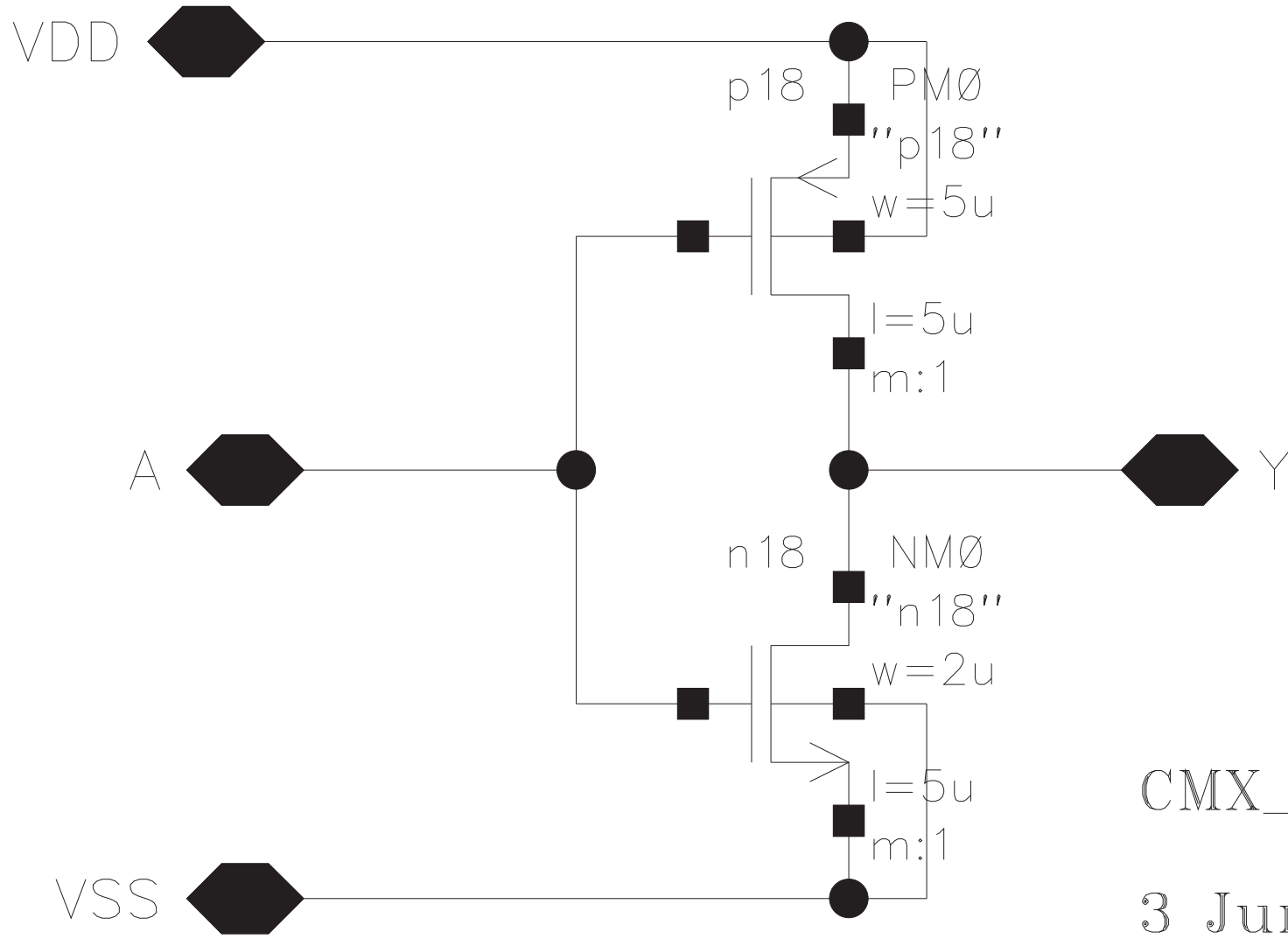




DTUNE\_DELAY1

3 June 2007

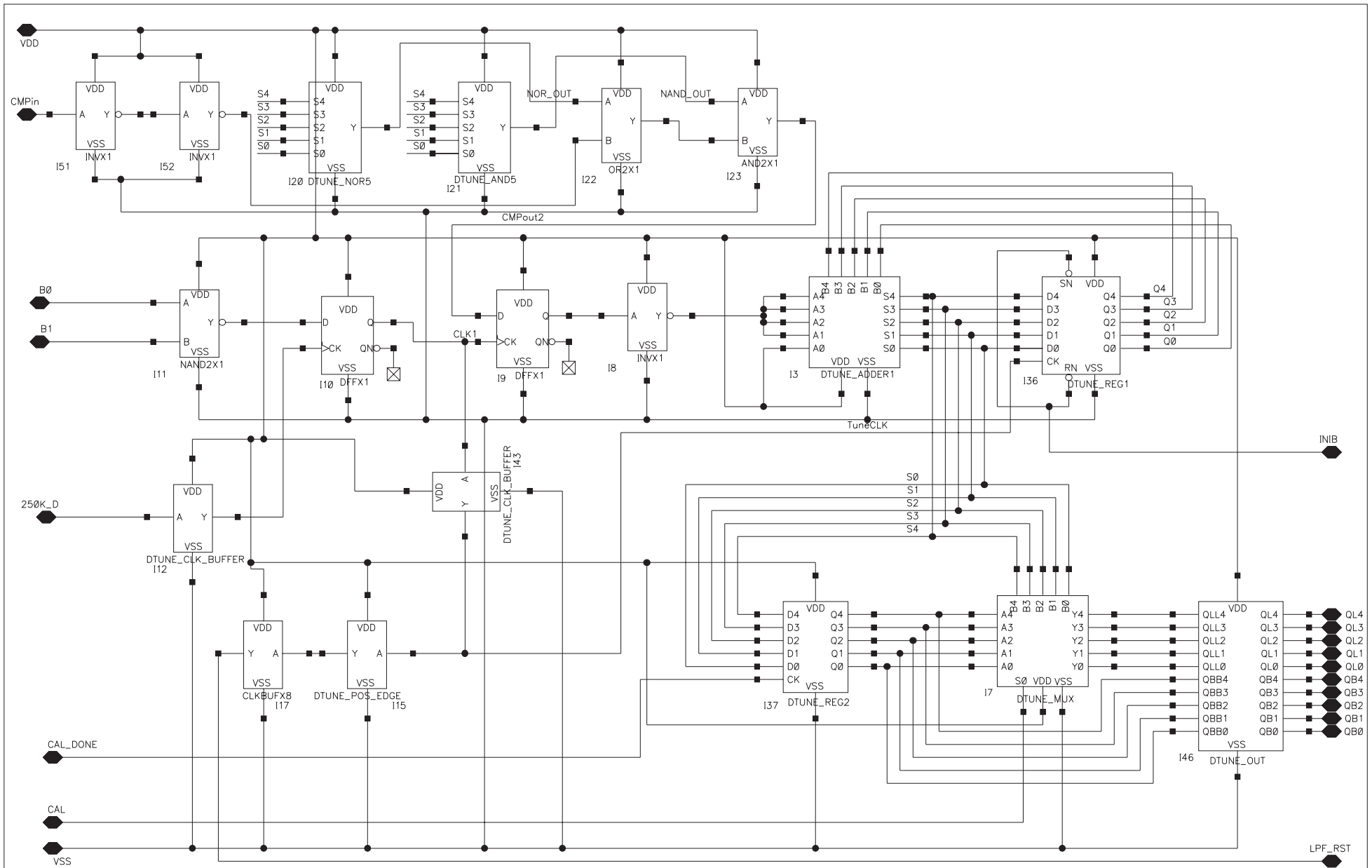
Xiaozhe Chen



CMX\_INVS12

3 June 2007

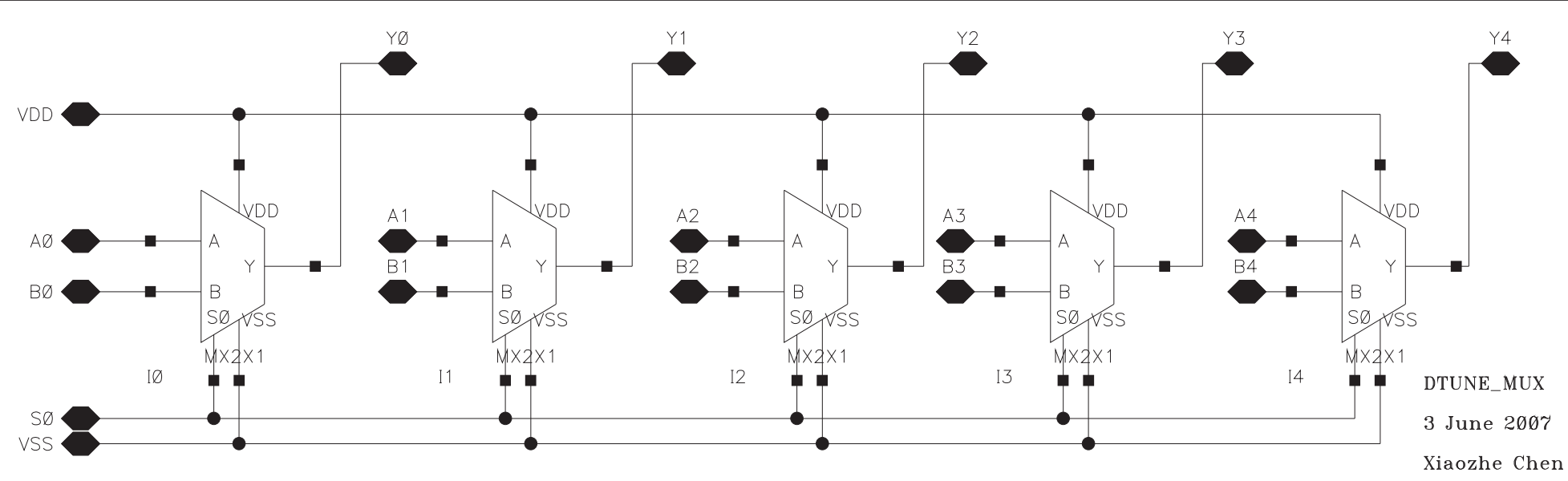
Xiaozhe Chen

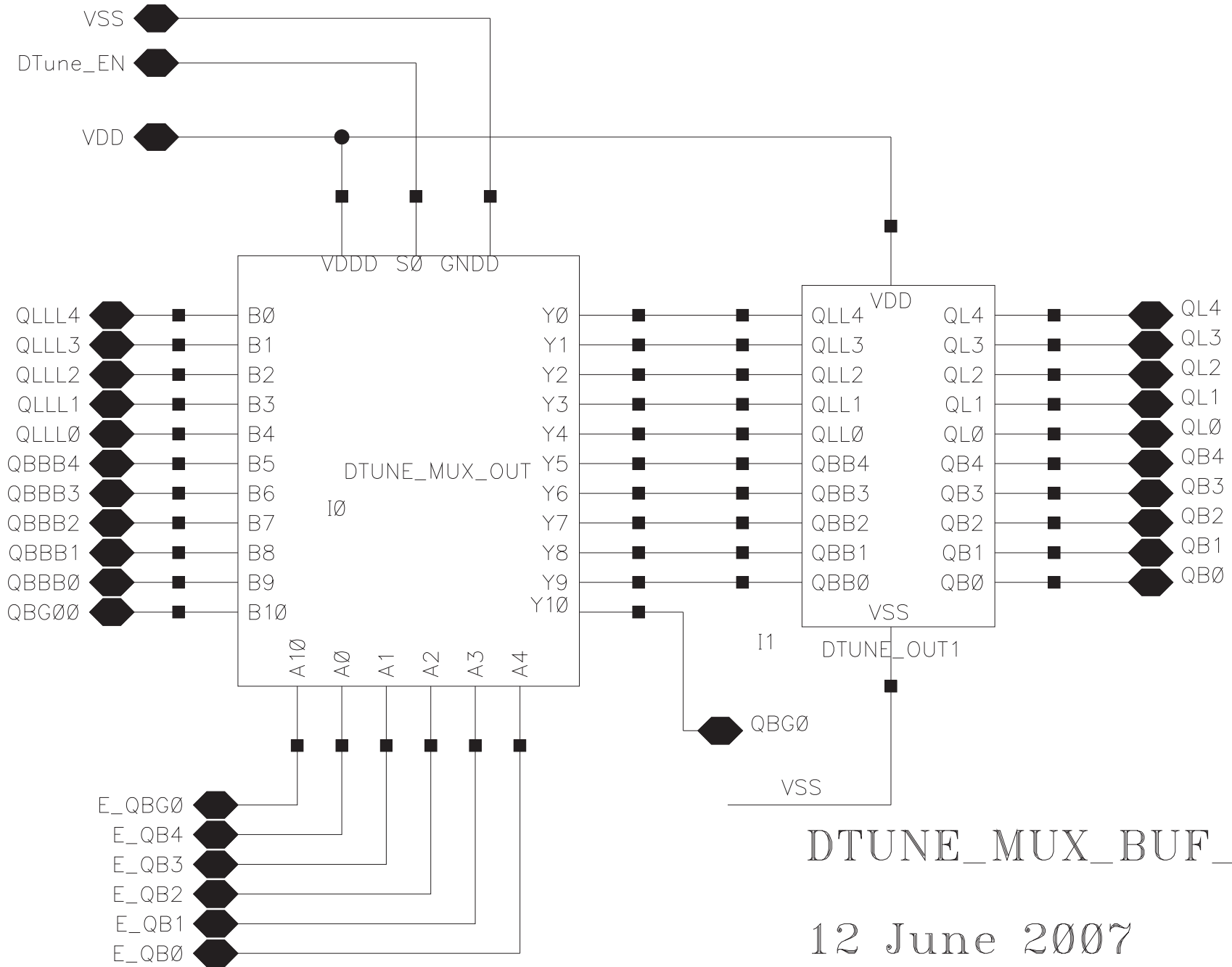


DTUNE\_LOOP

3 June 2007

Xiaozhe Chen

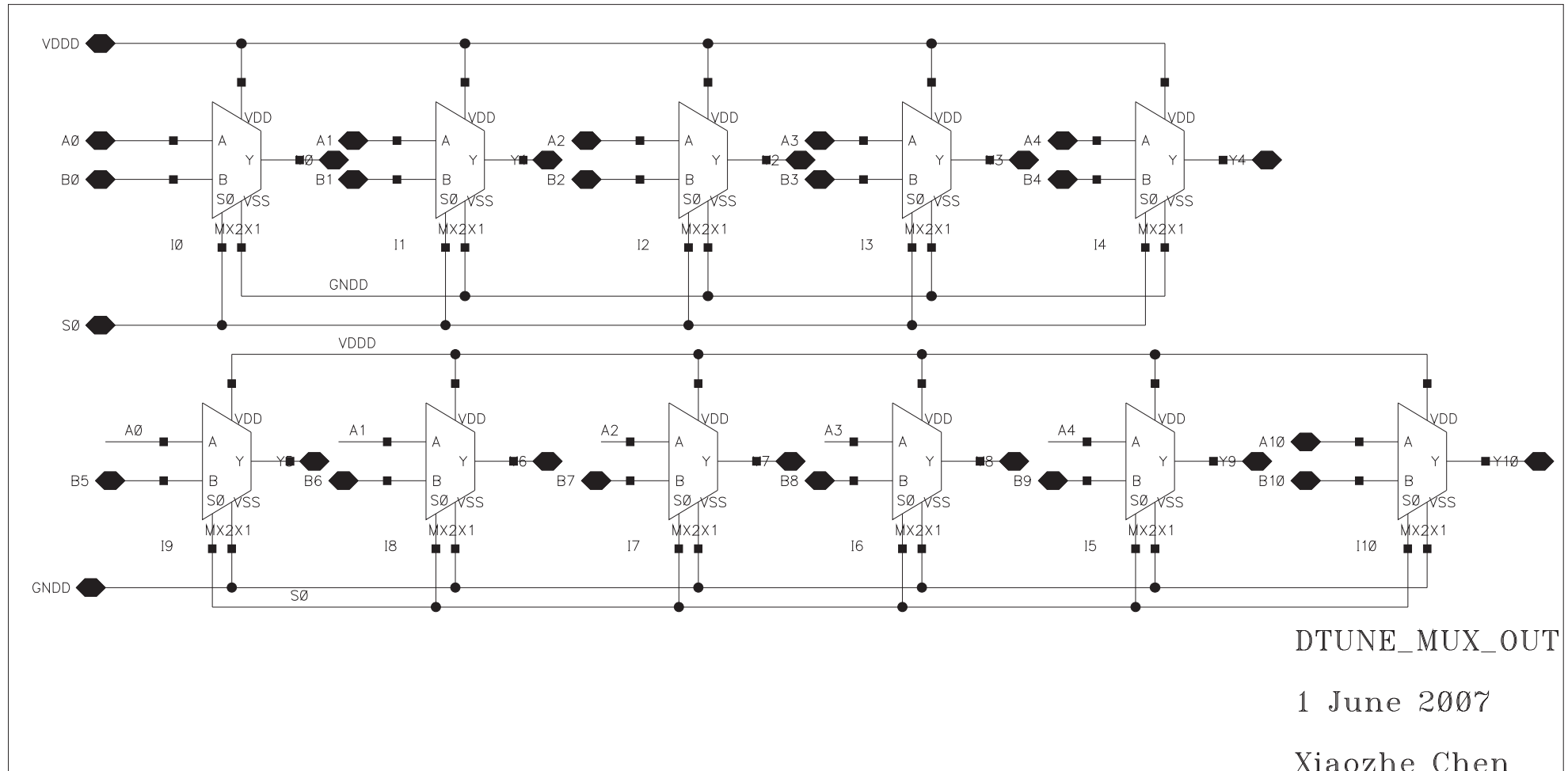




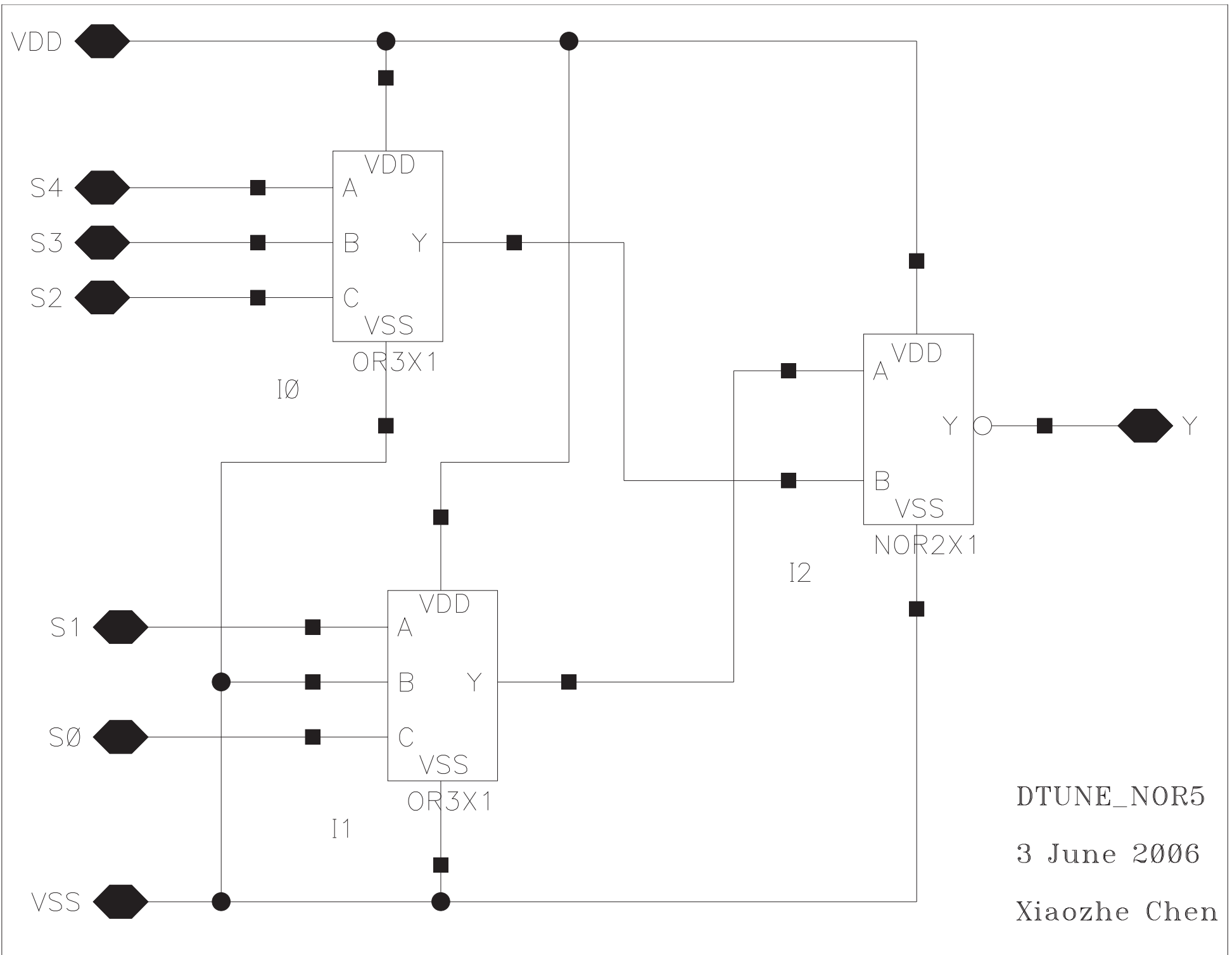
DTUNE\_MUX\_BUF\_OUT

12 June 2007





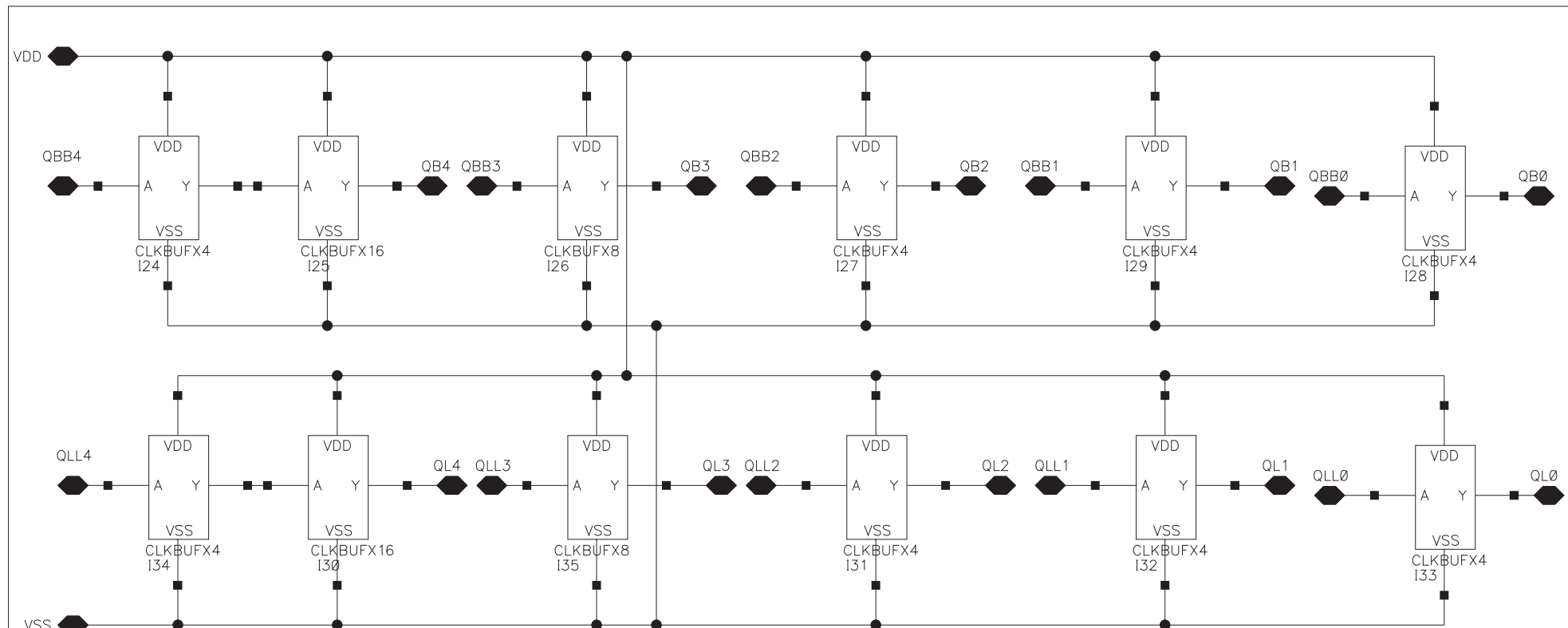




DTUNE\_NOR5

3 June 2006

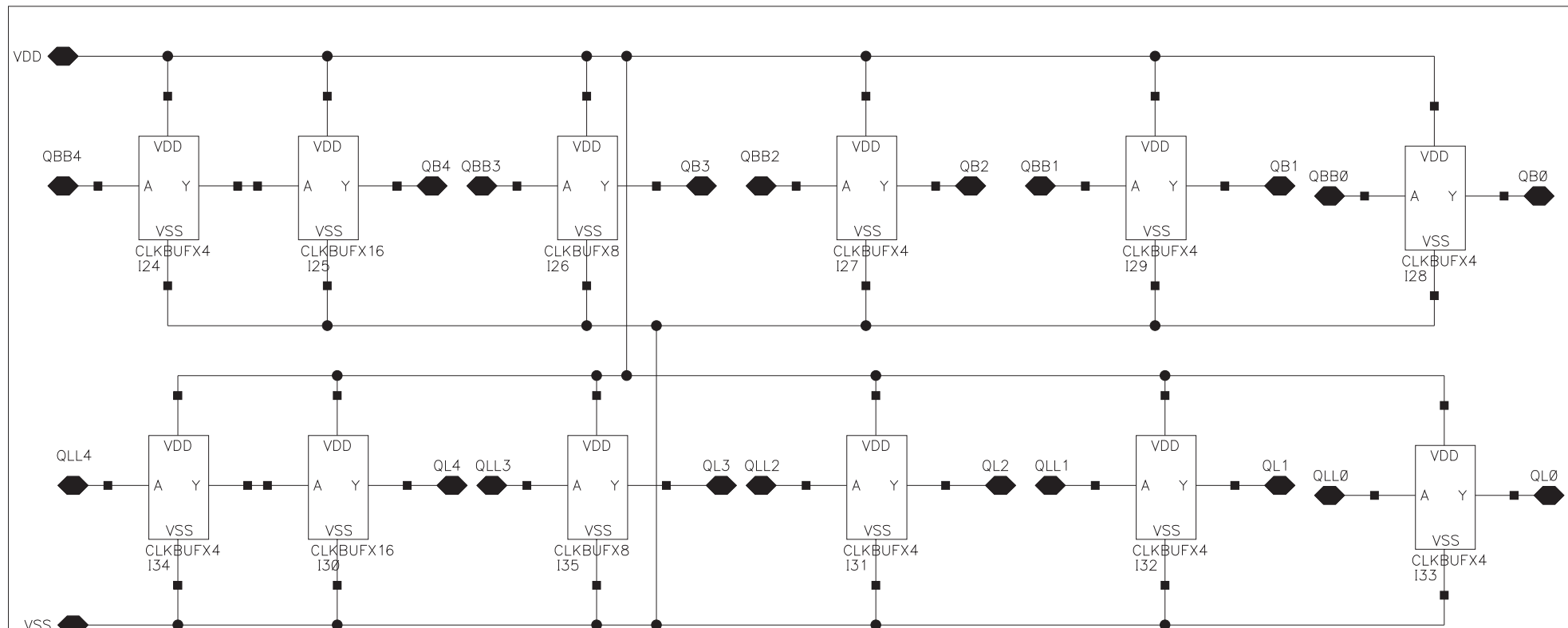
Xiaozhe Chen



DTUNE\_OUT

3 June 2007

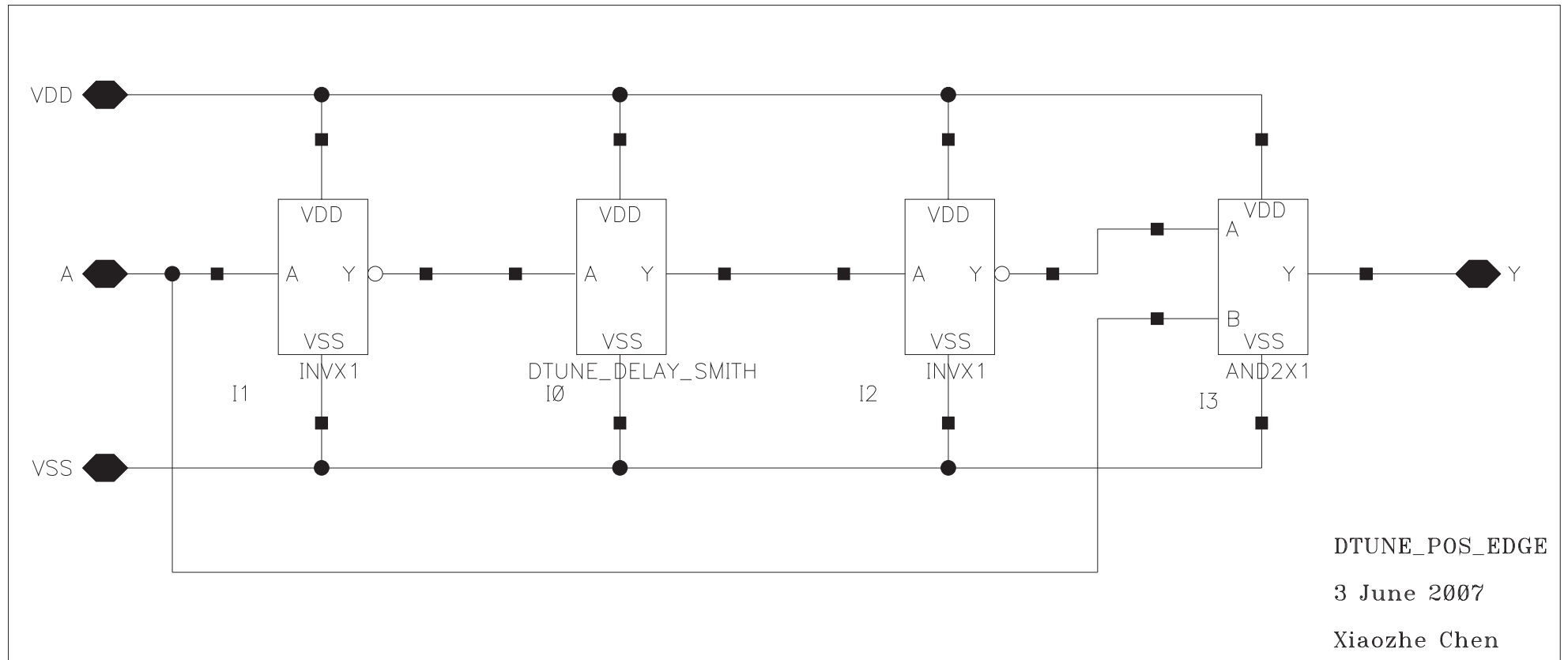
Xiaozhe Chen

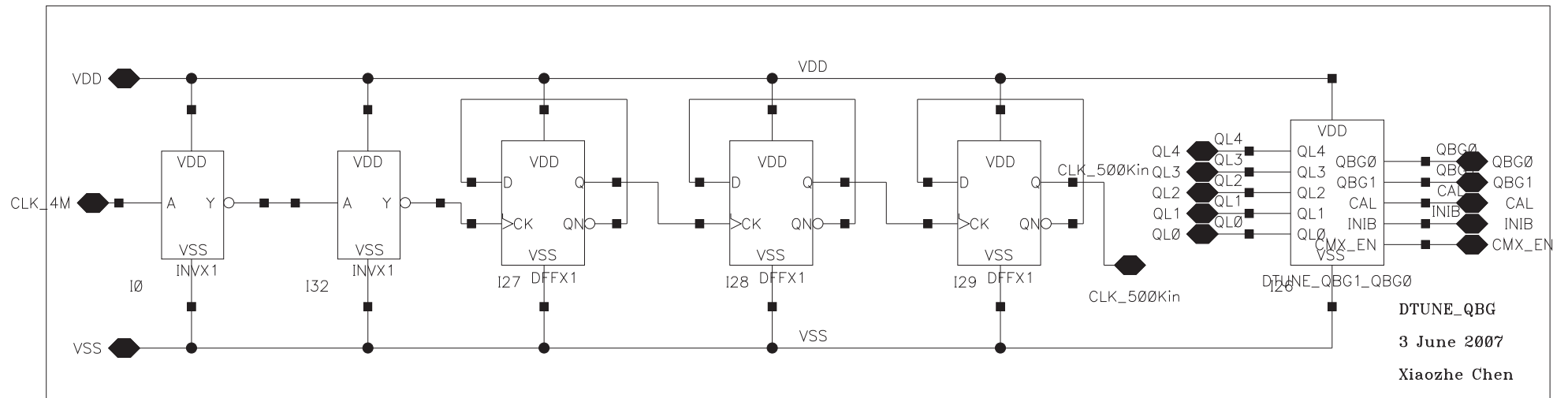


DTUNE\_OUT

3 June 2007

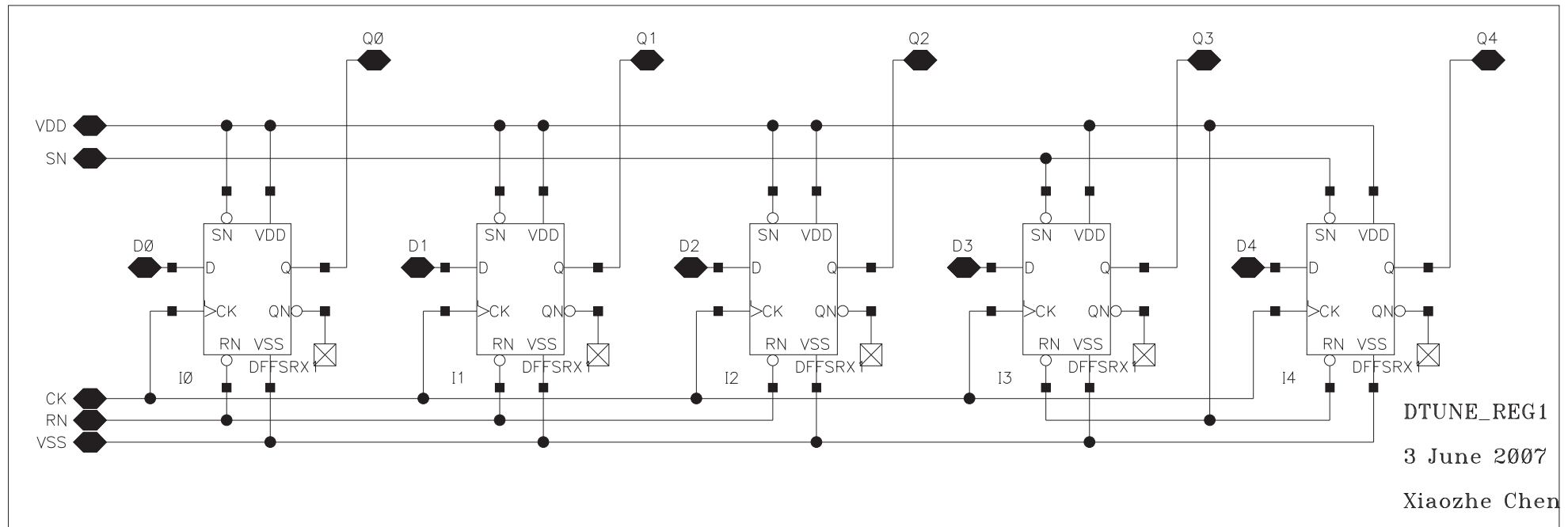
Xiaozhe Chen

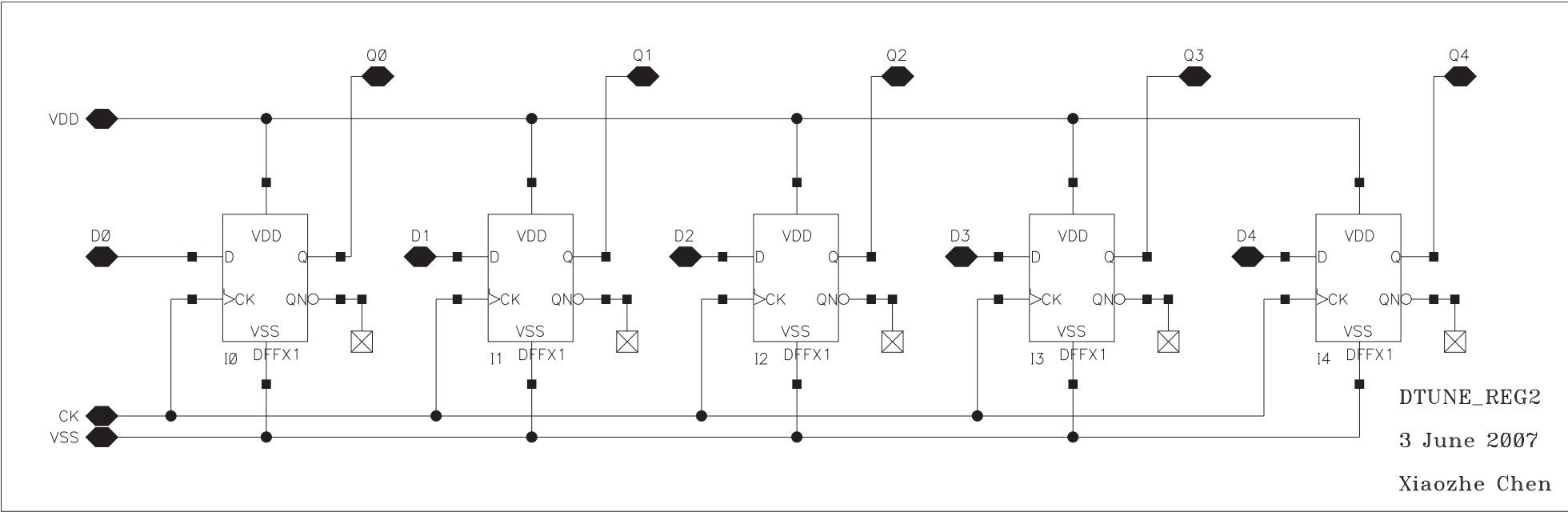


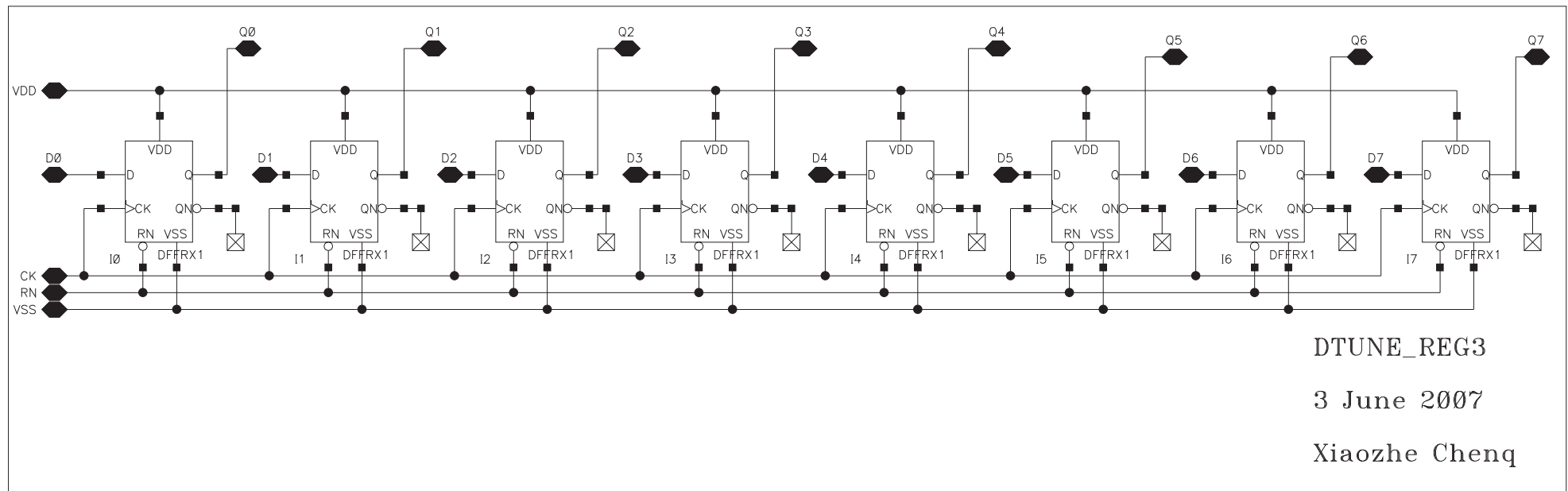








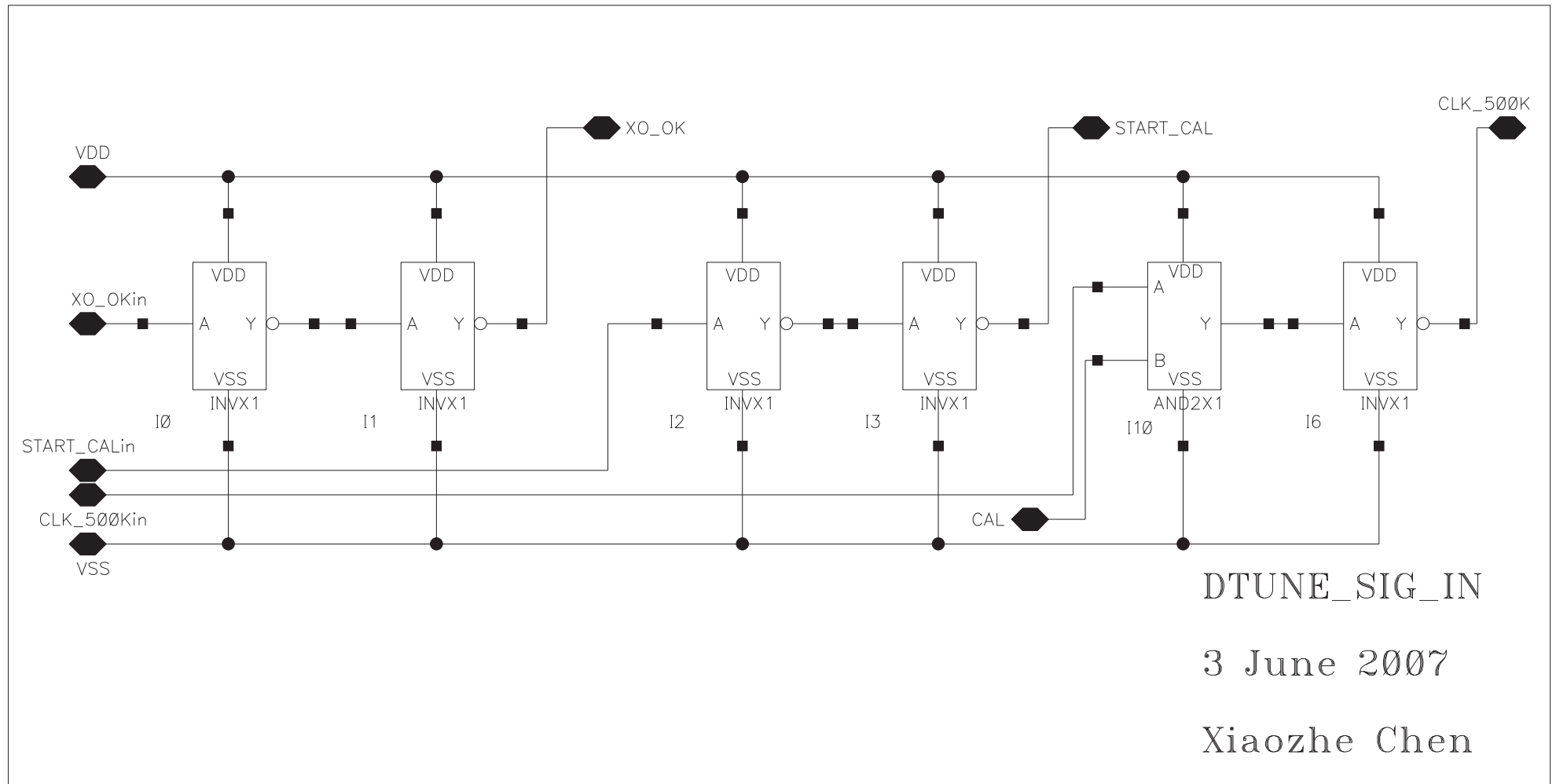


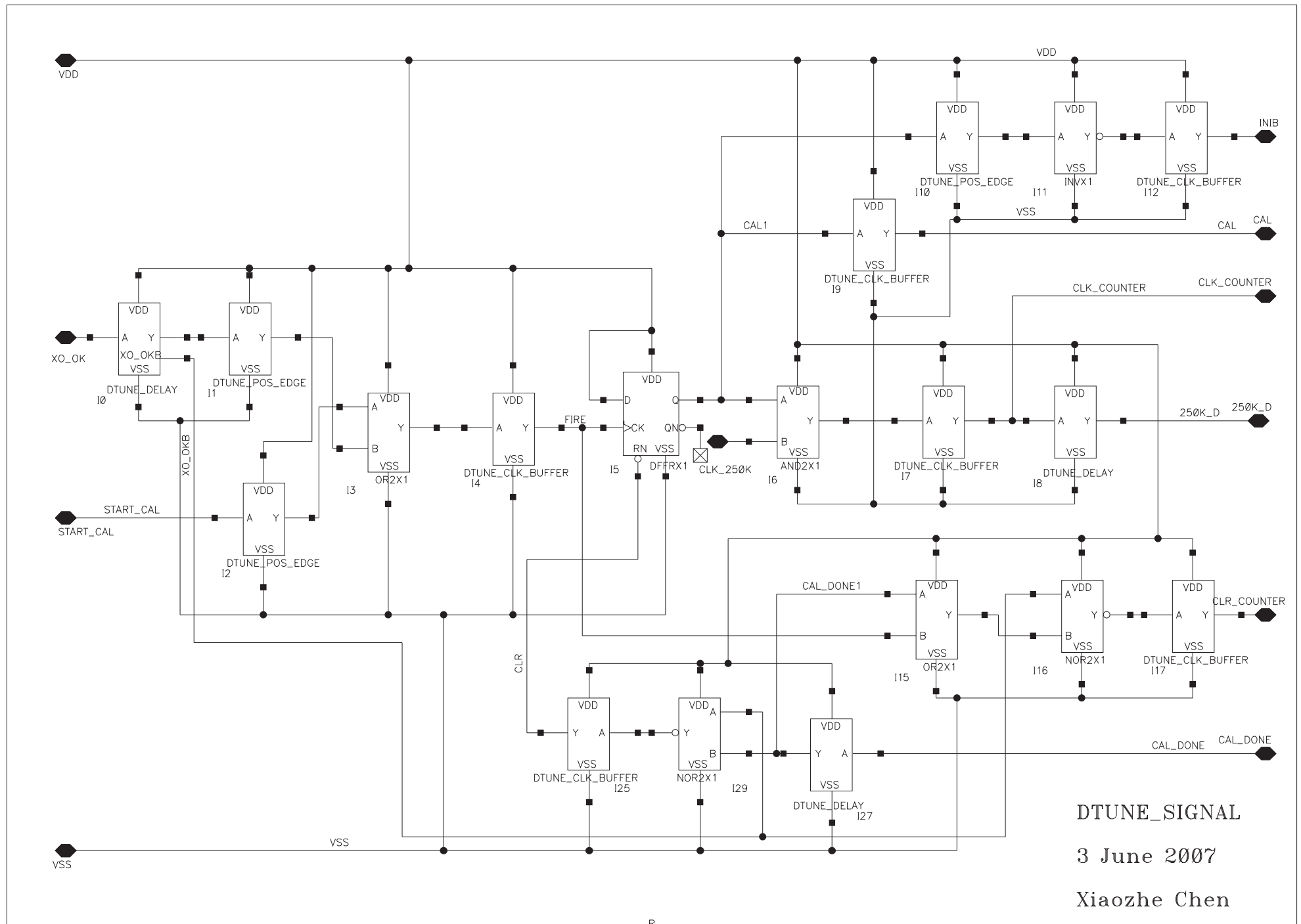


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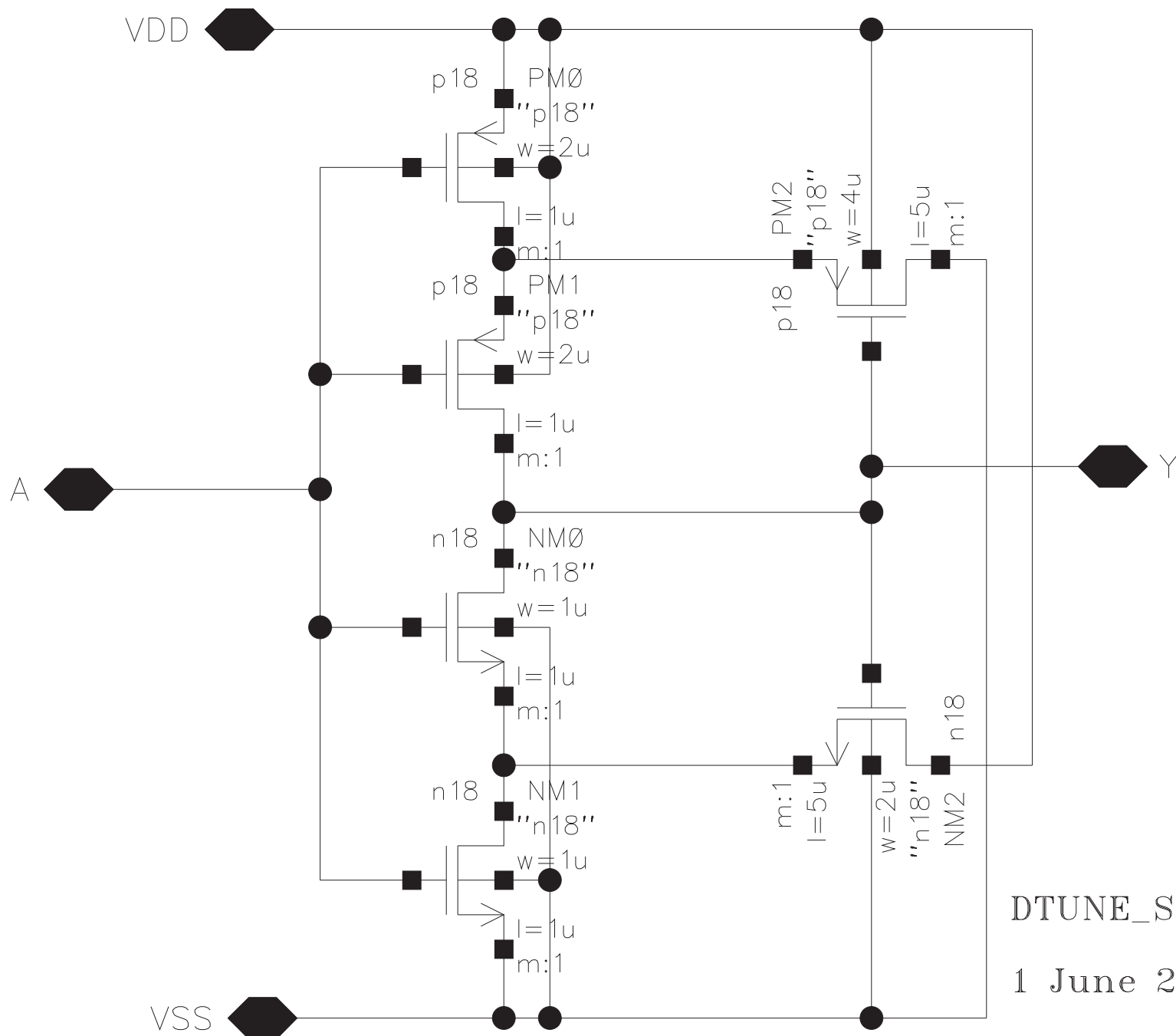
3 June 2007

Xiaozhe Chenq









DTUNE\_SMITH1

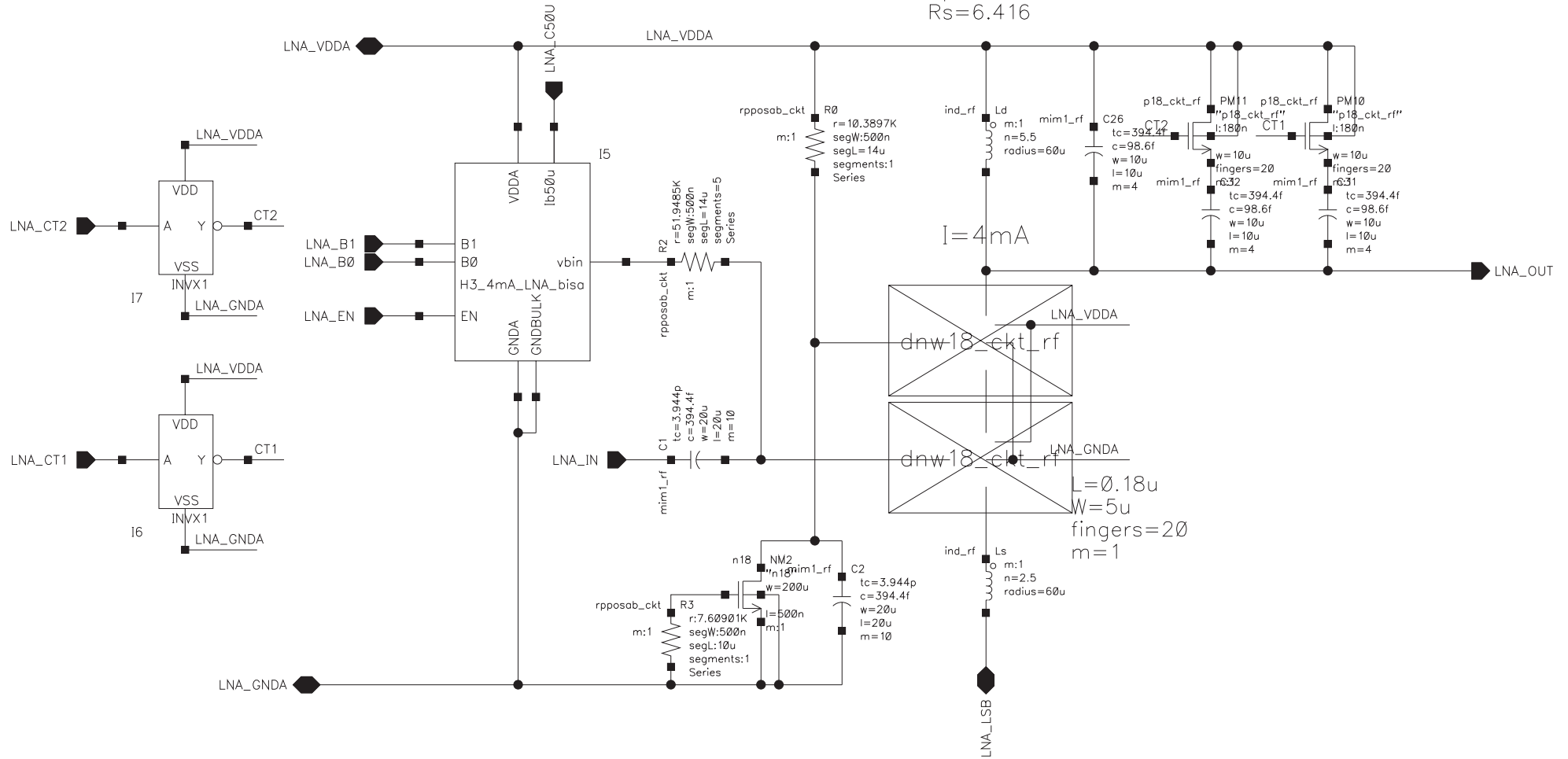
1 June 2007

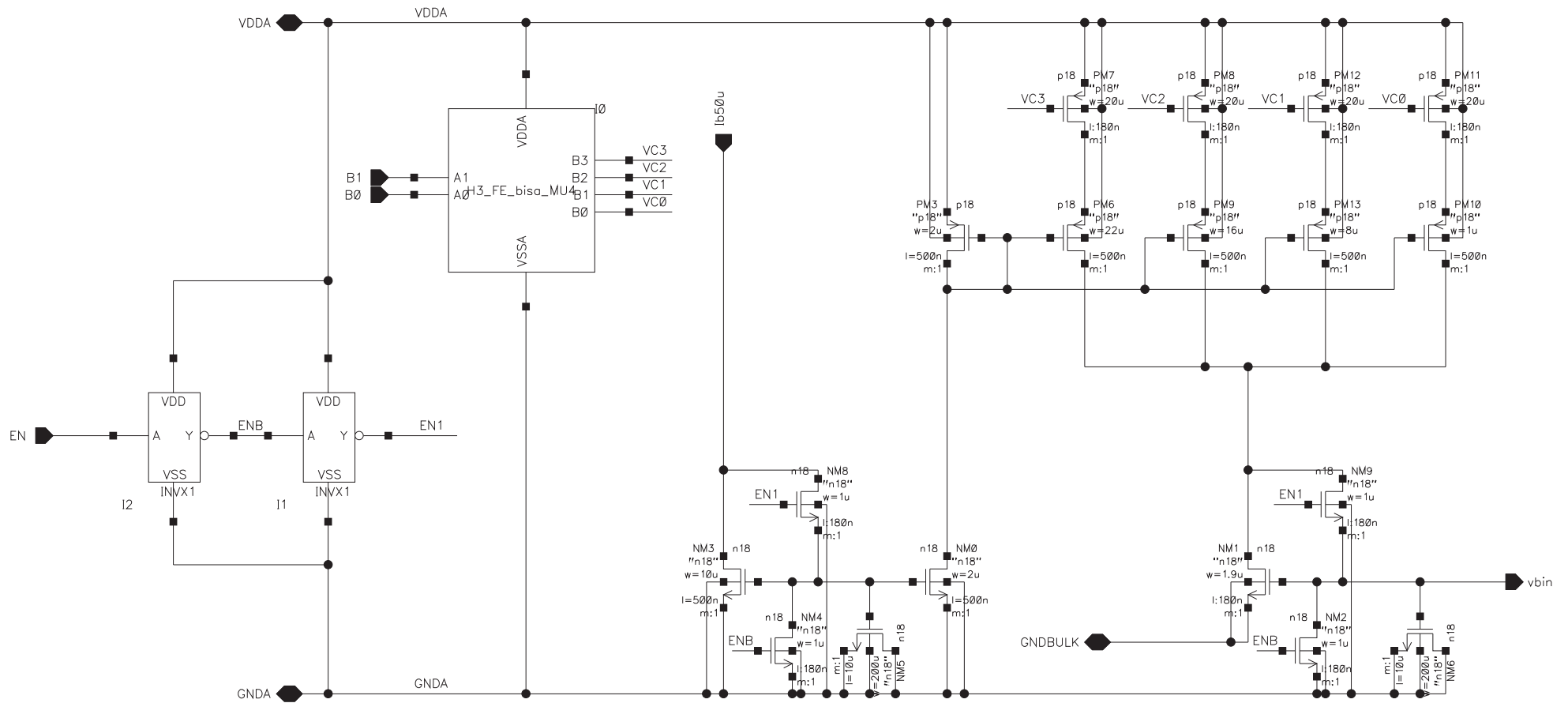
Xiaozhe Chen

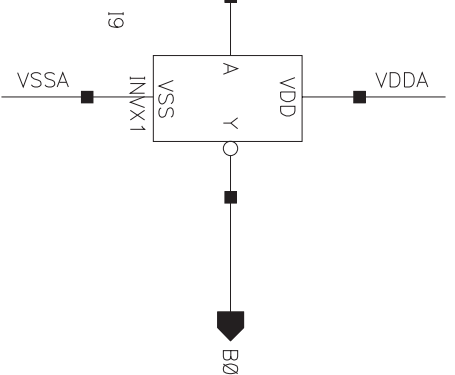
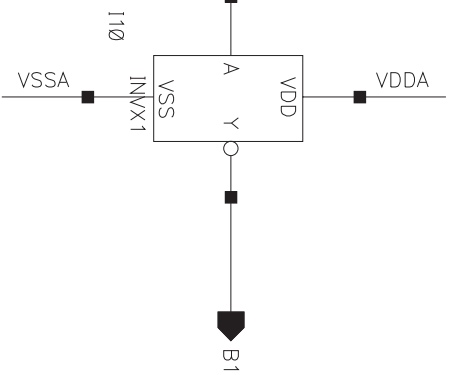
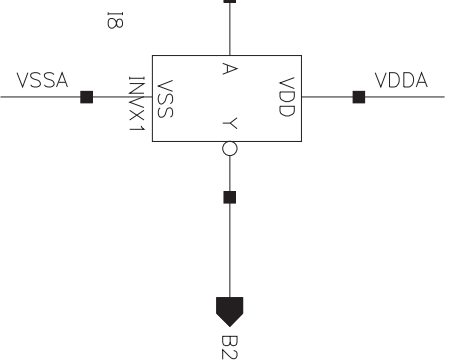
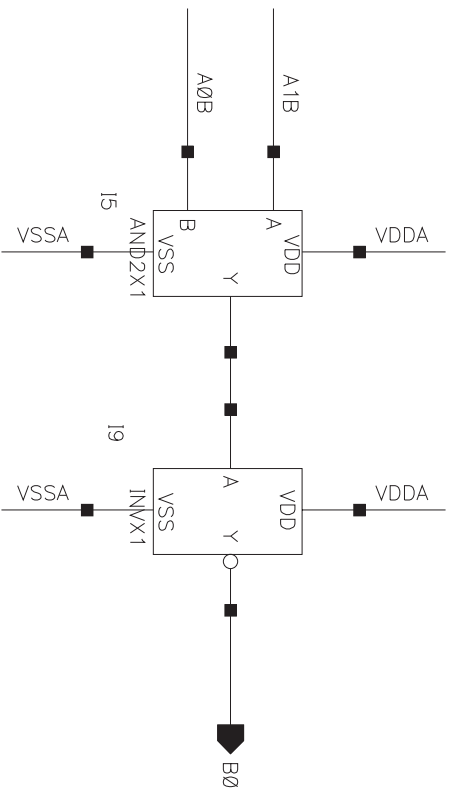
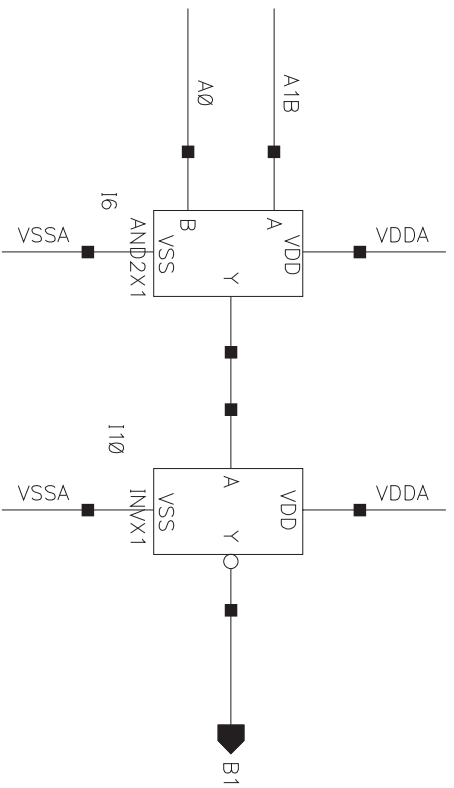
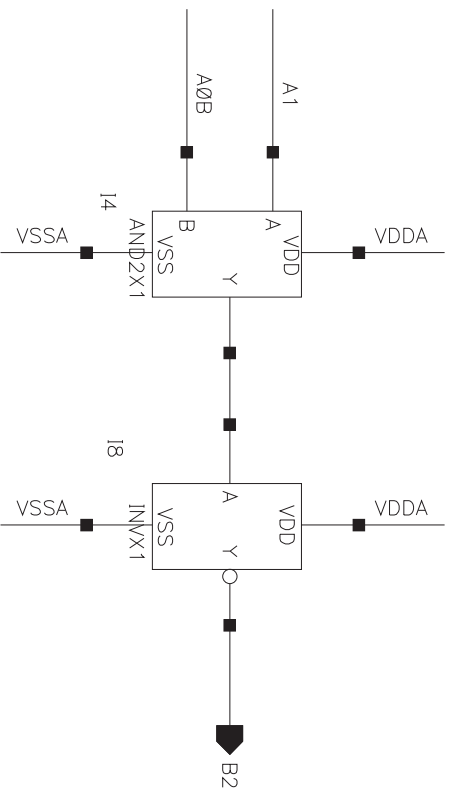
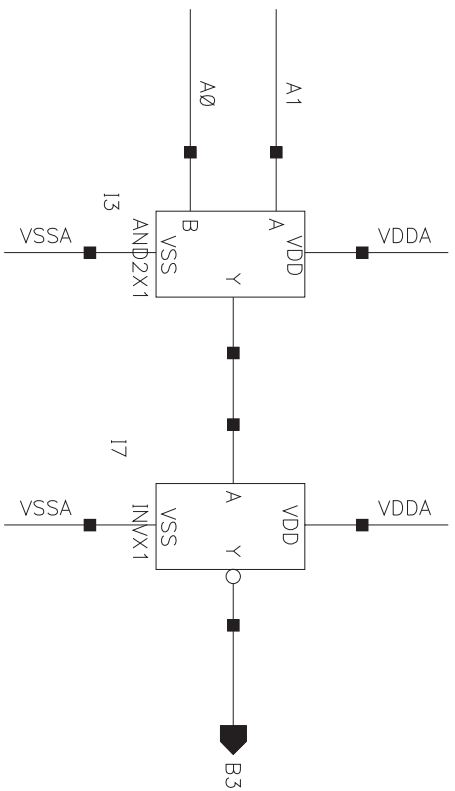
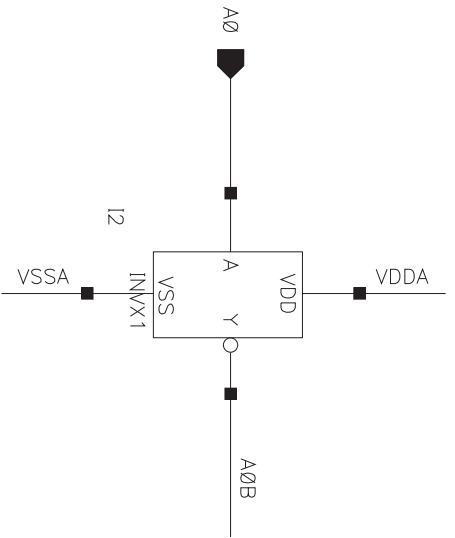
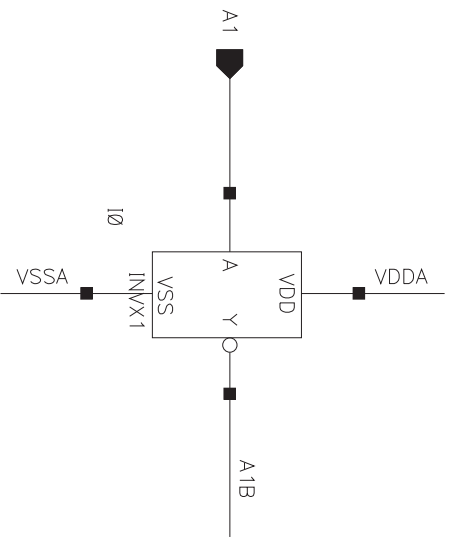
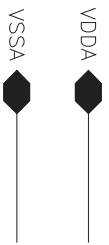


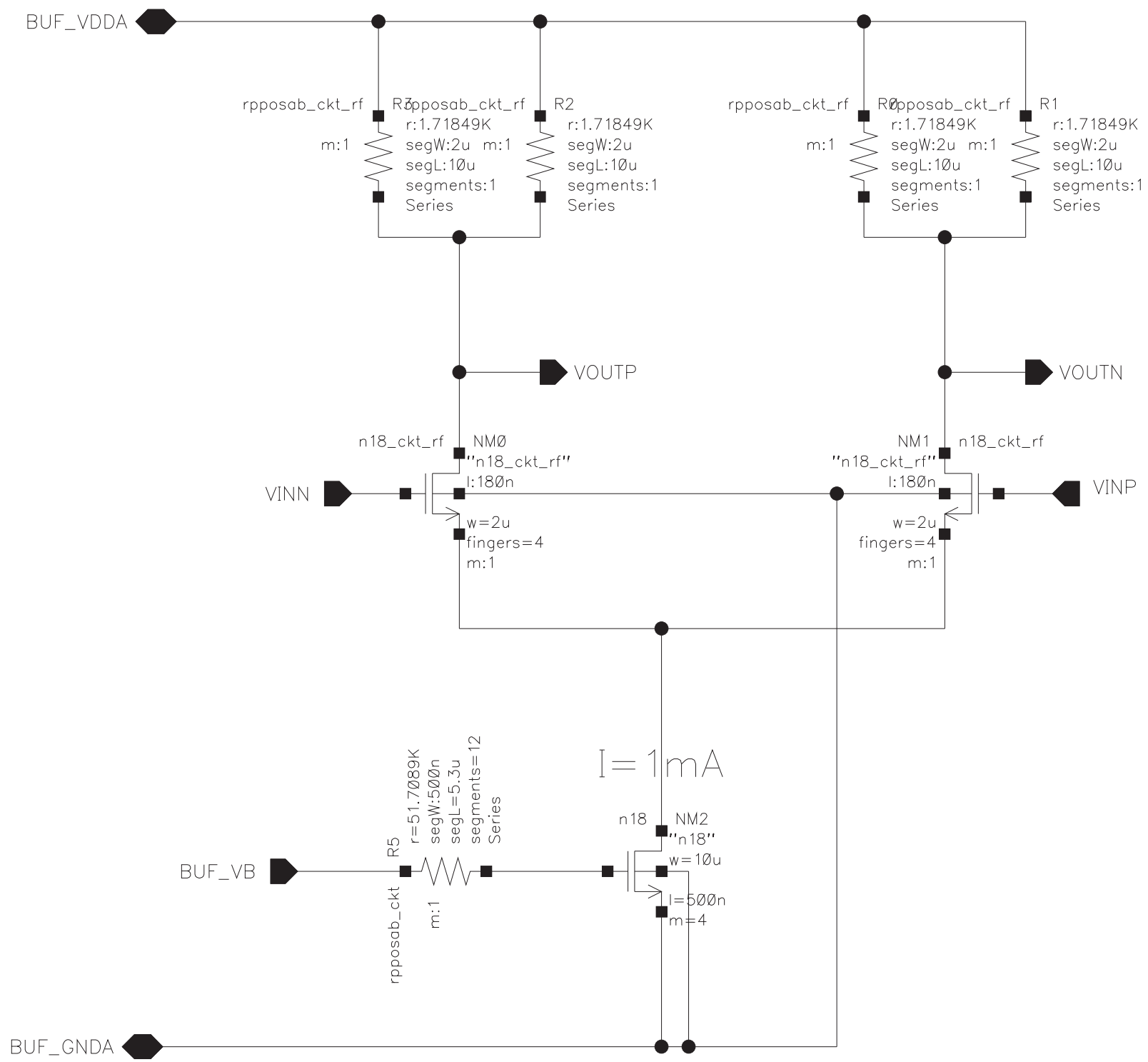


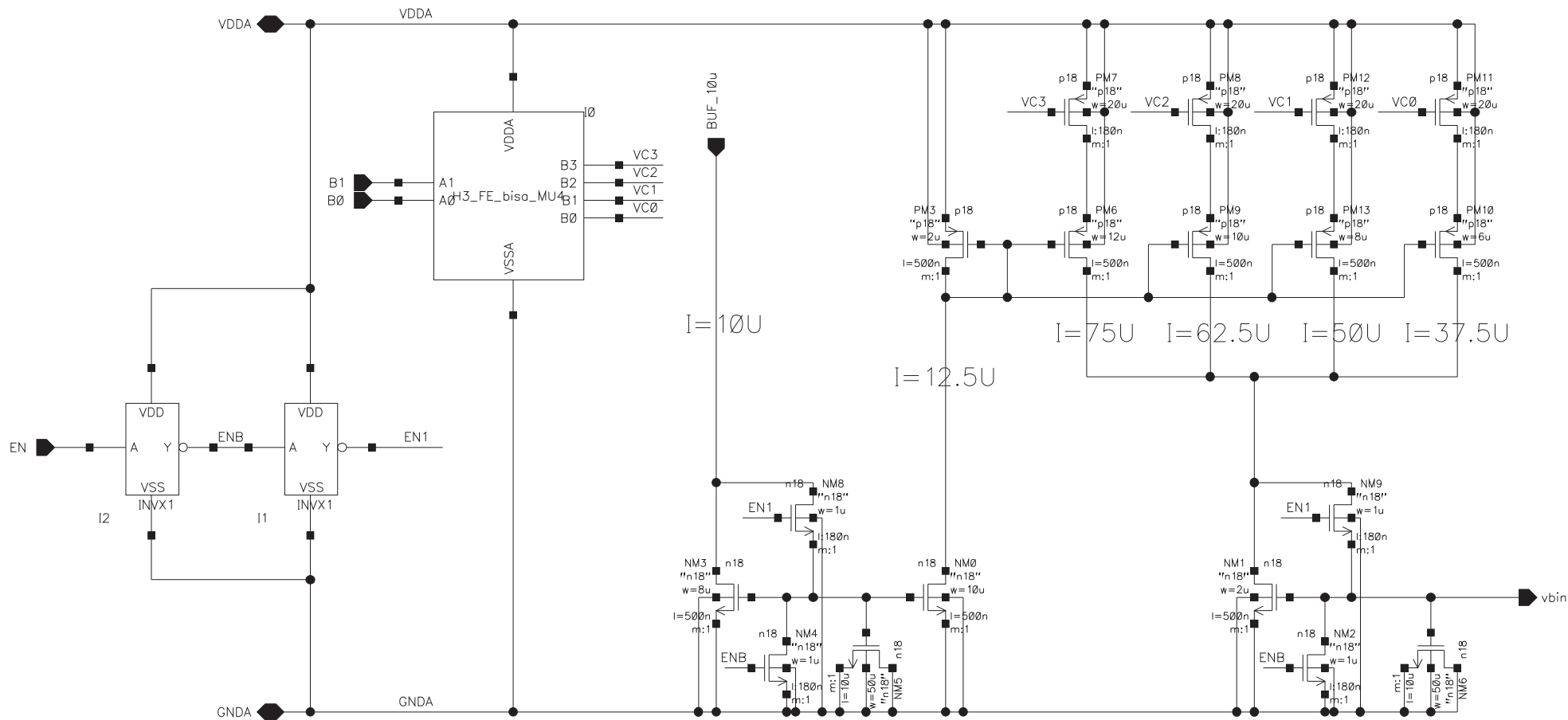
$L_d = 7.649n$   
 $Q = 11.8$  fixed capacitor:  $\varnothing.4p$   
 $R_p = 893$  for RFIC  
 $R_s = 6.416$

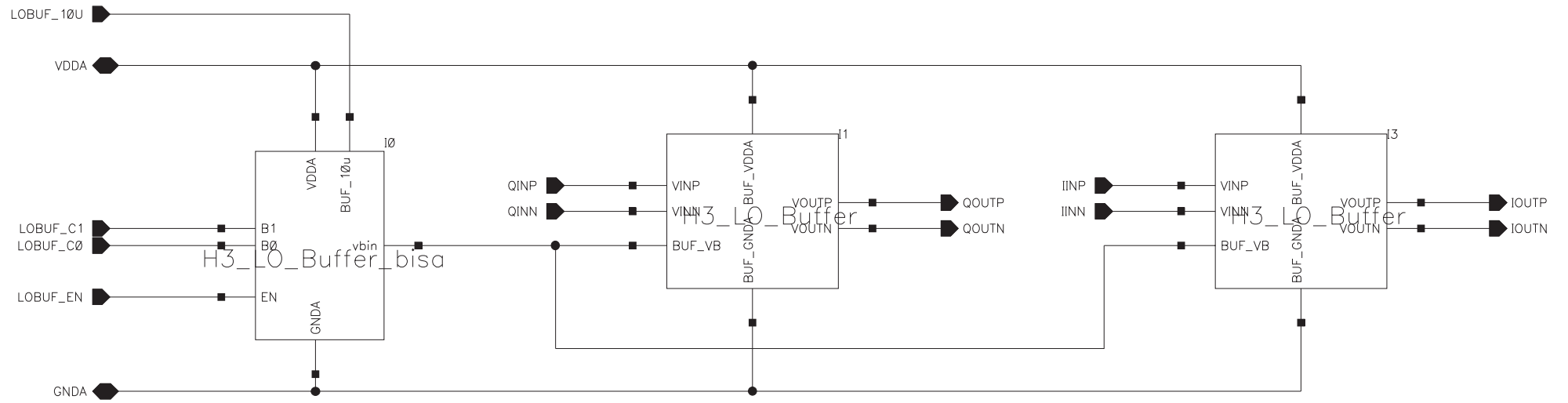








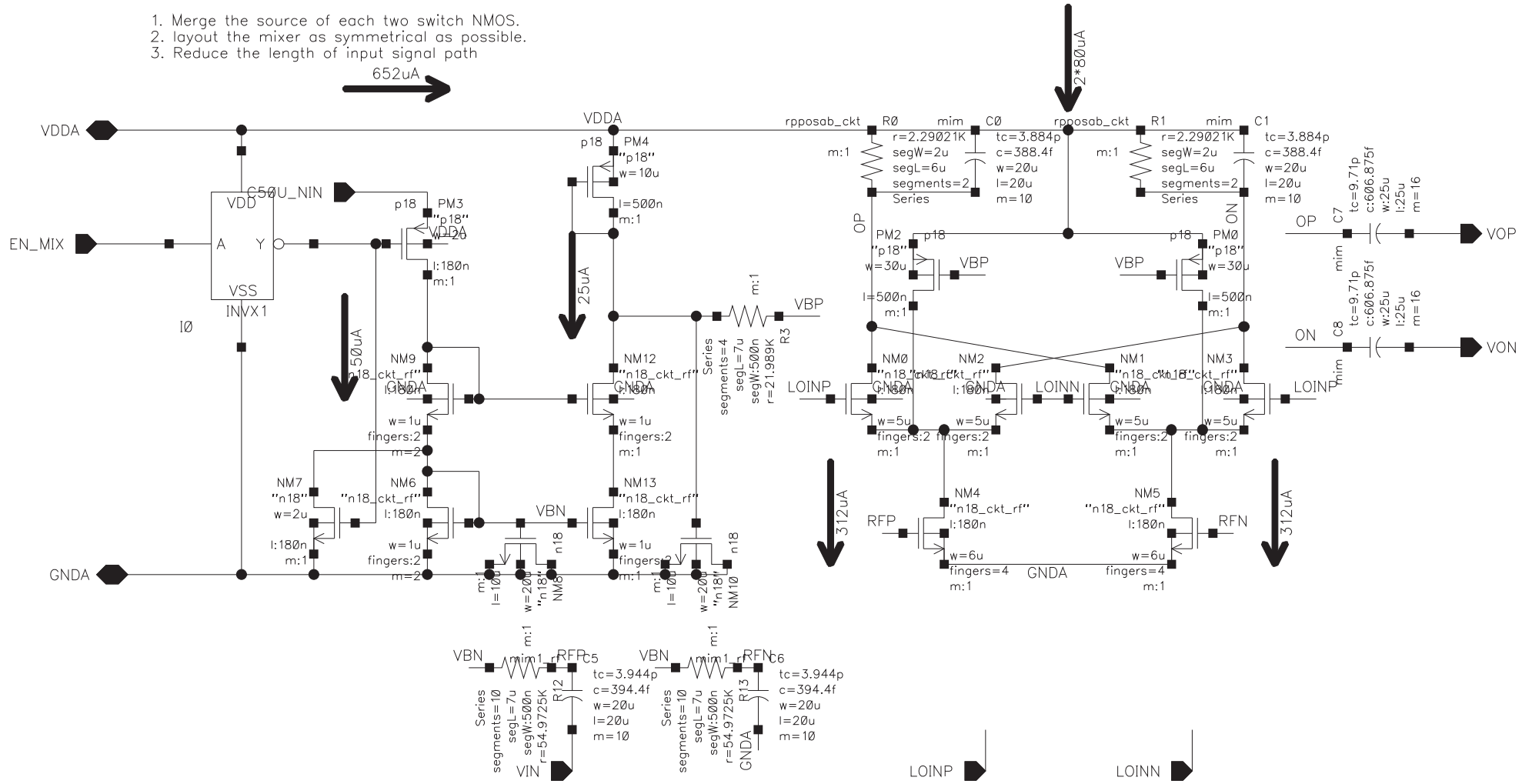


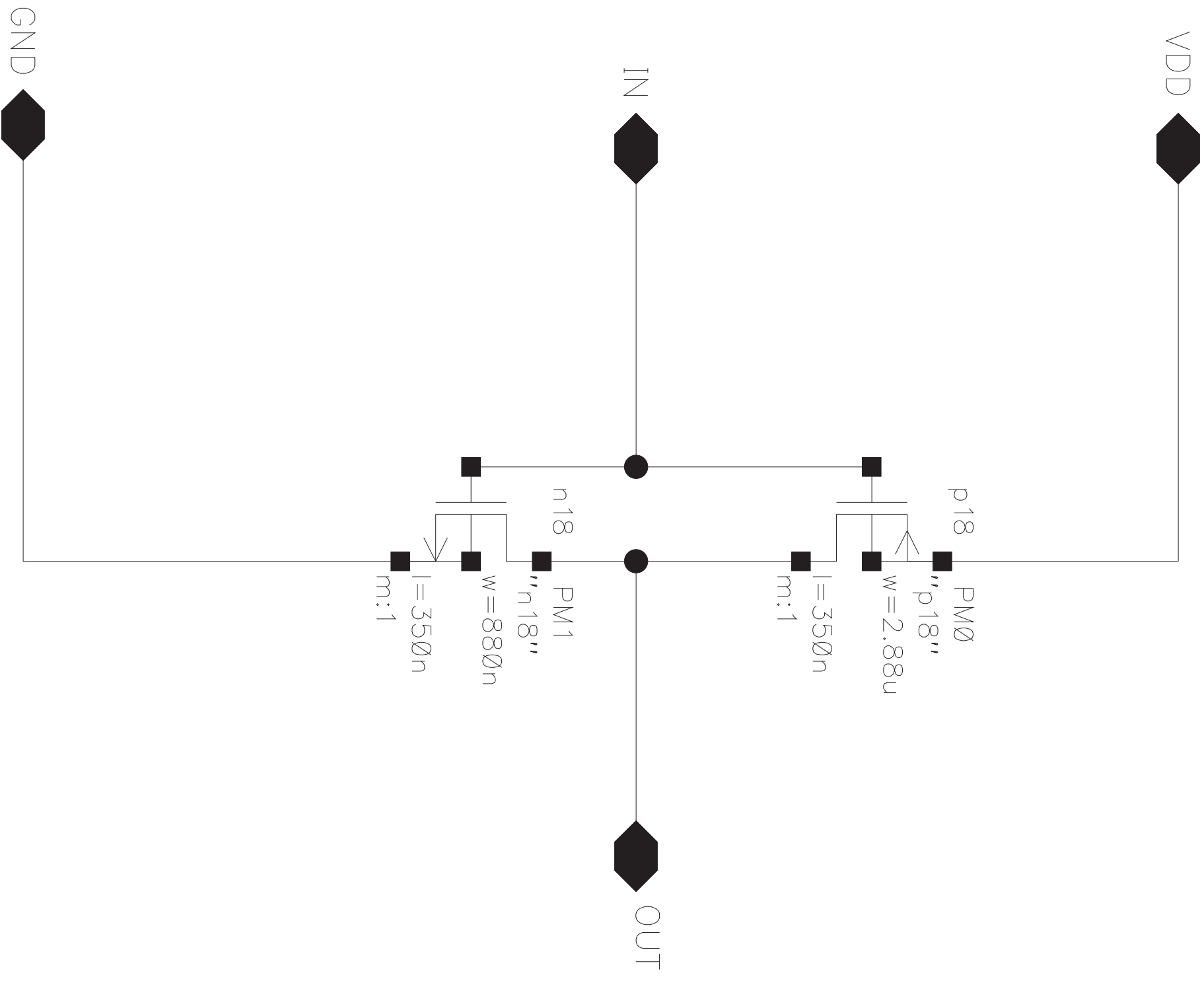


# Notes

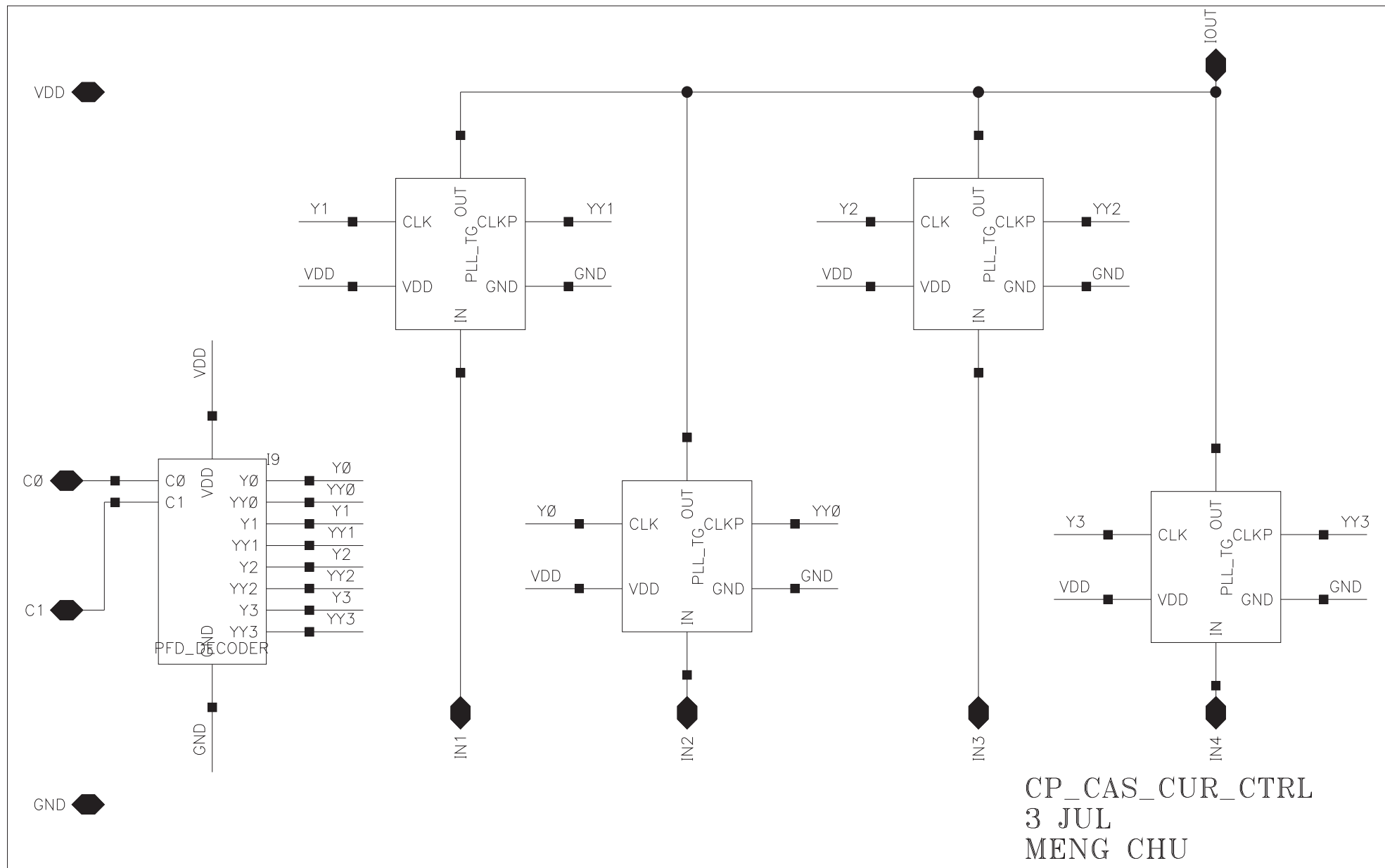
A layout

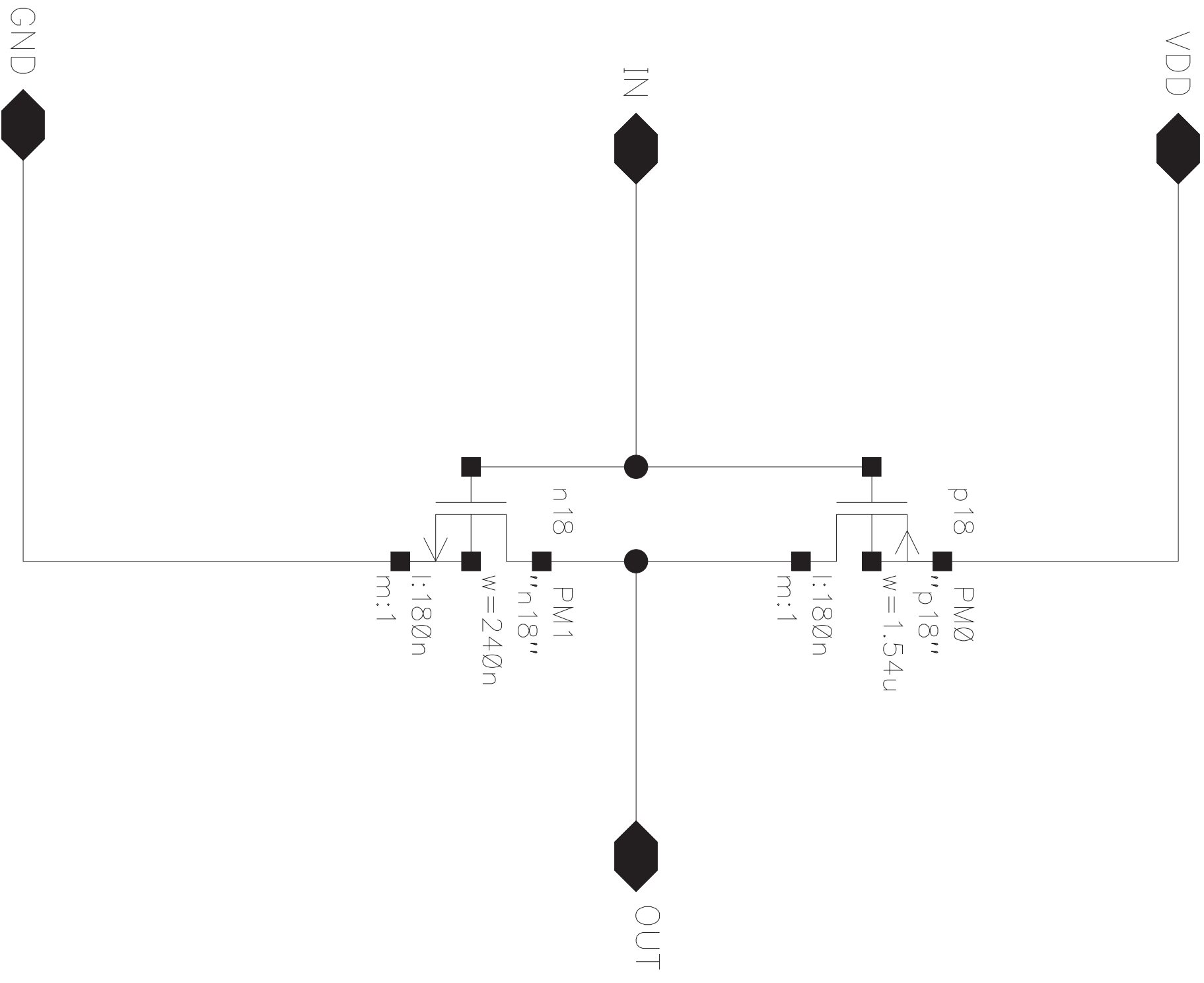
1. Merge the source of each two switch NMOS.
2. layout the mixer as symmetrical as possible.
3. Reduce the length of input signal path

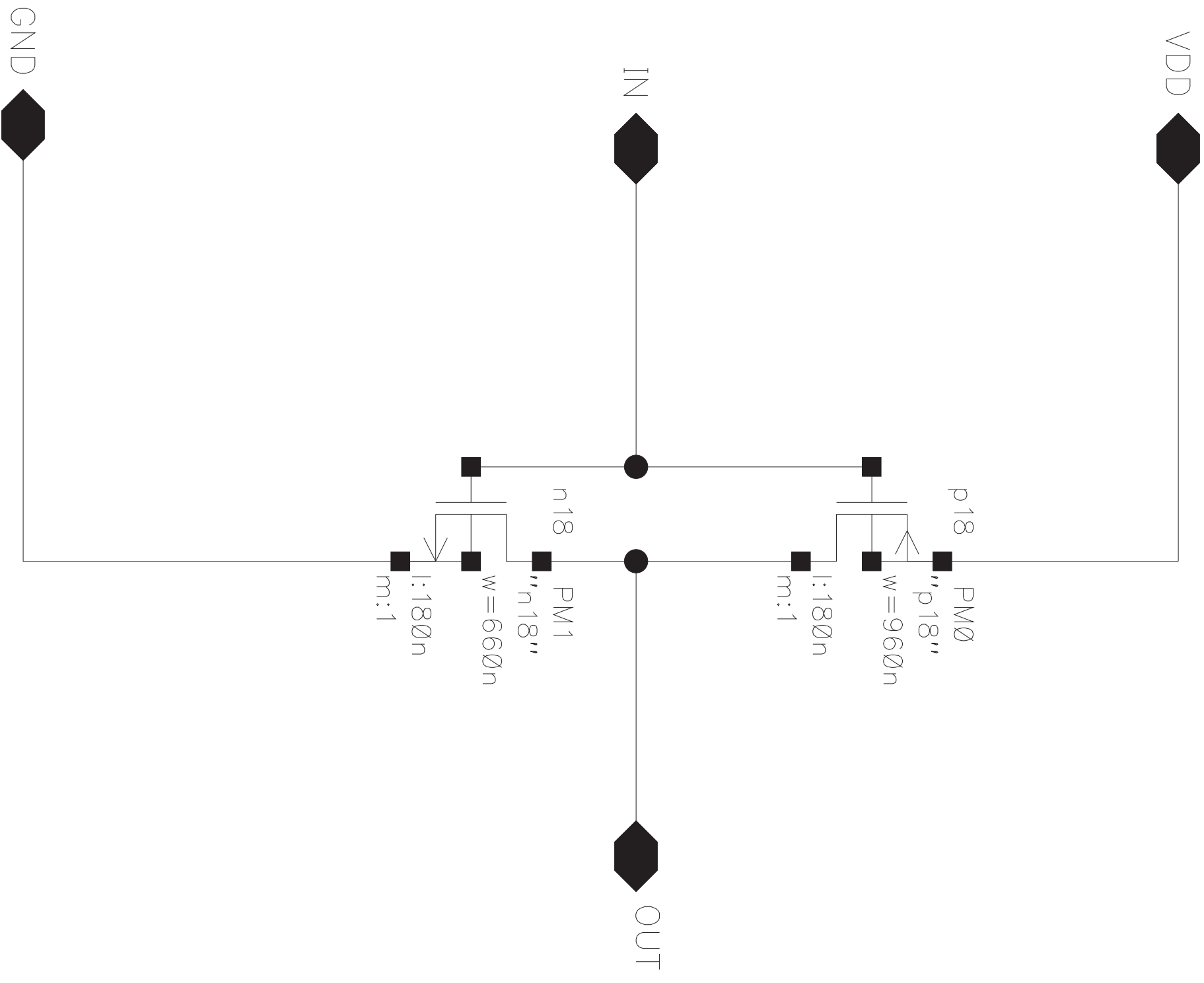


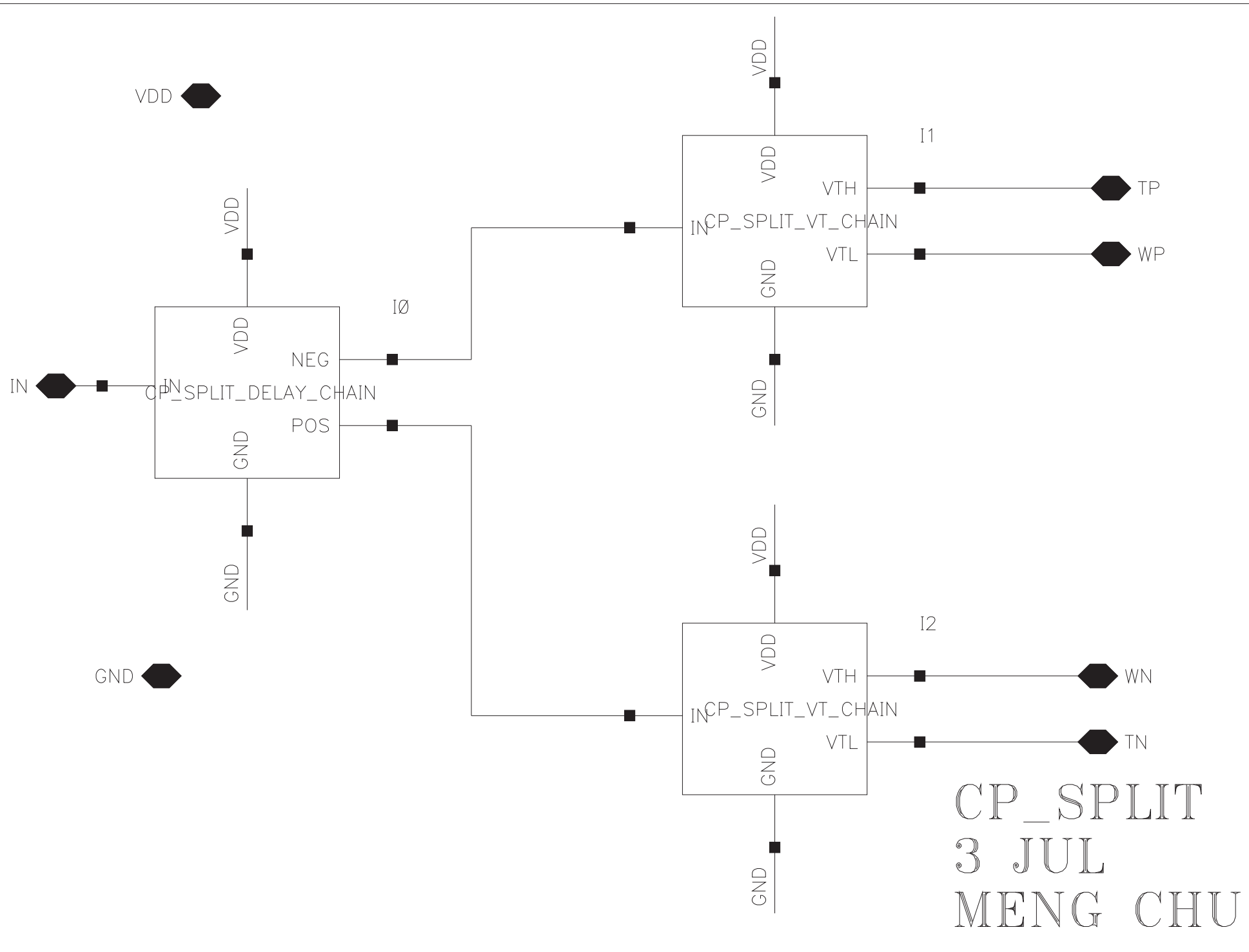


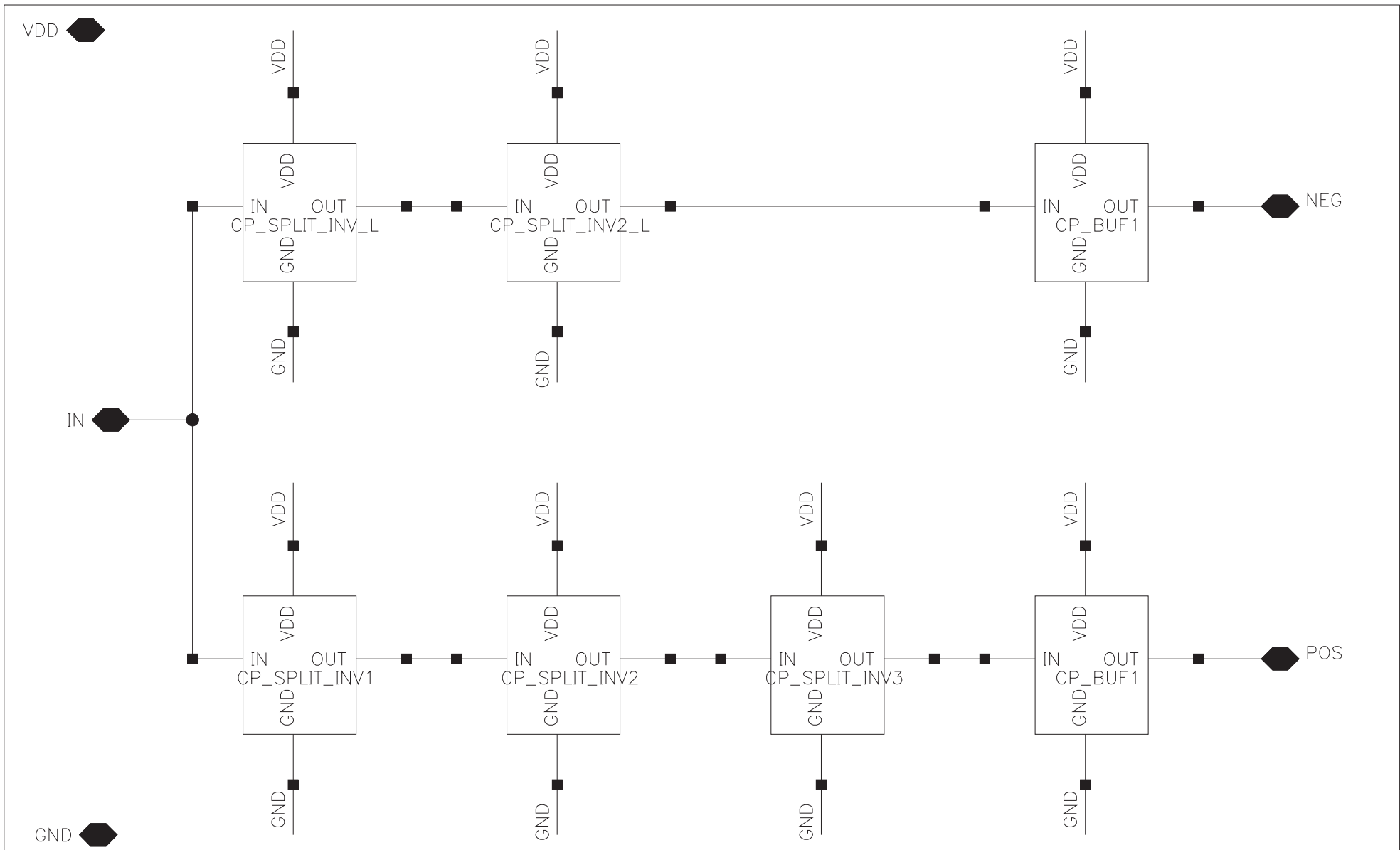




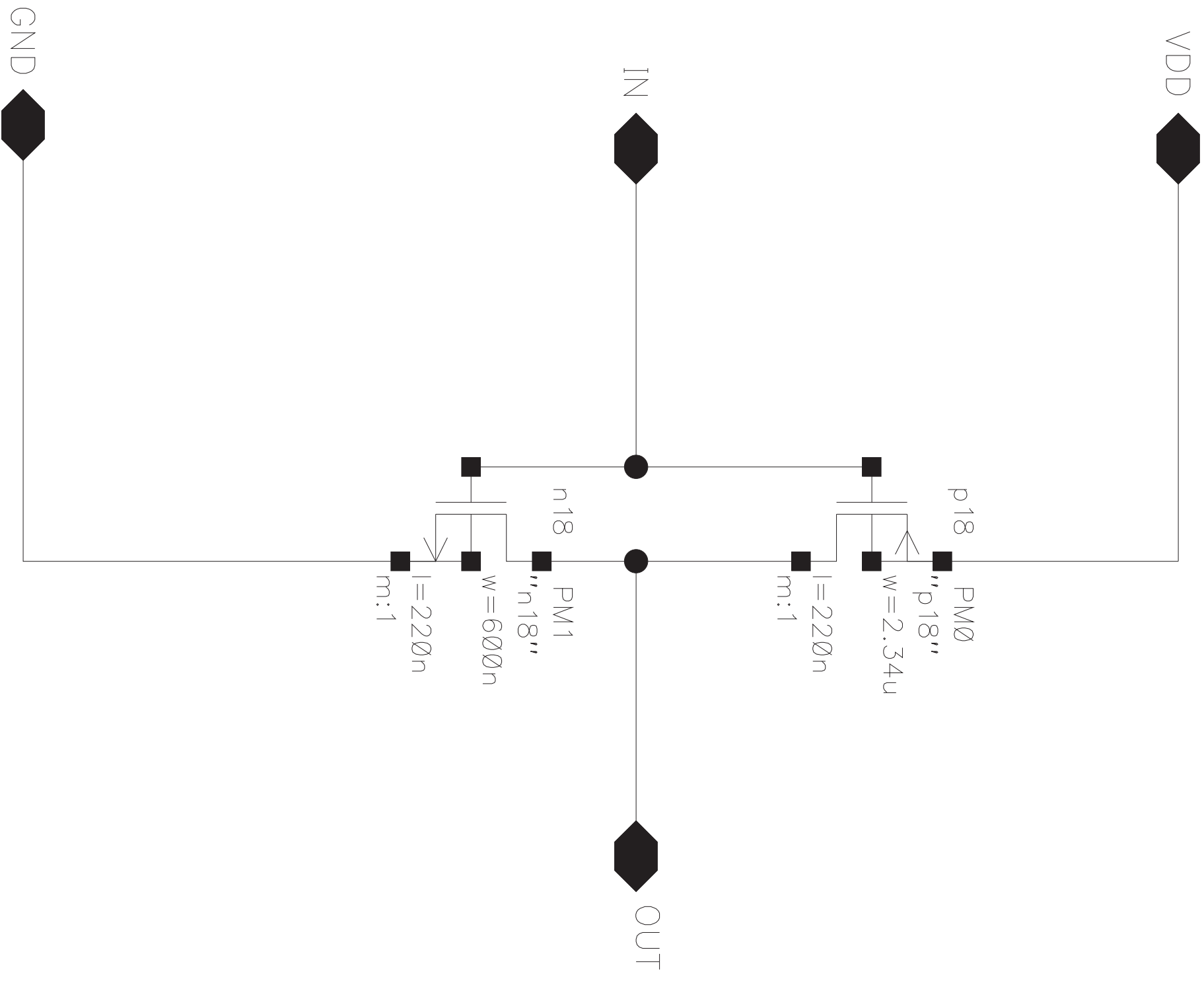


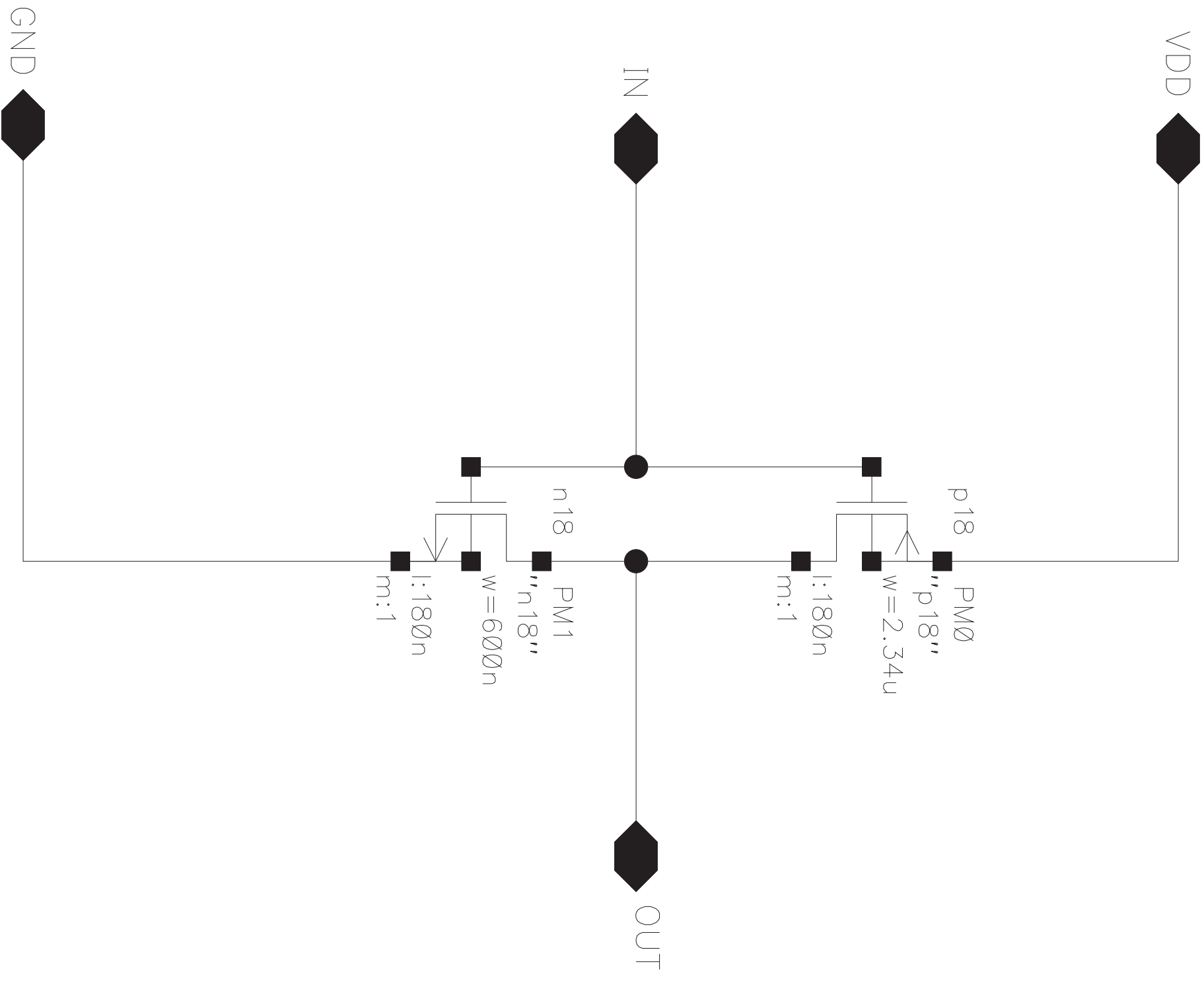


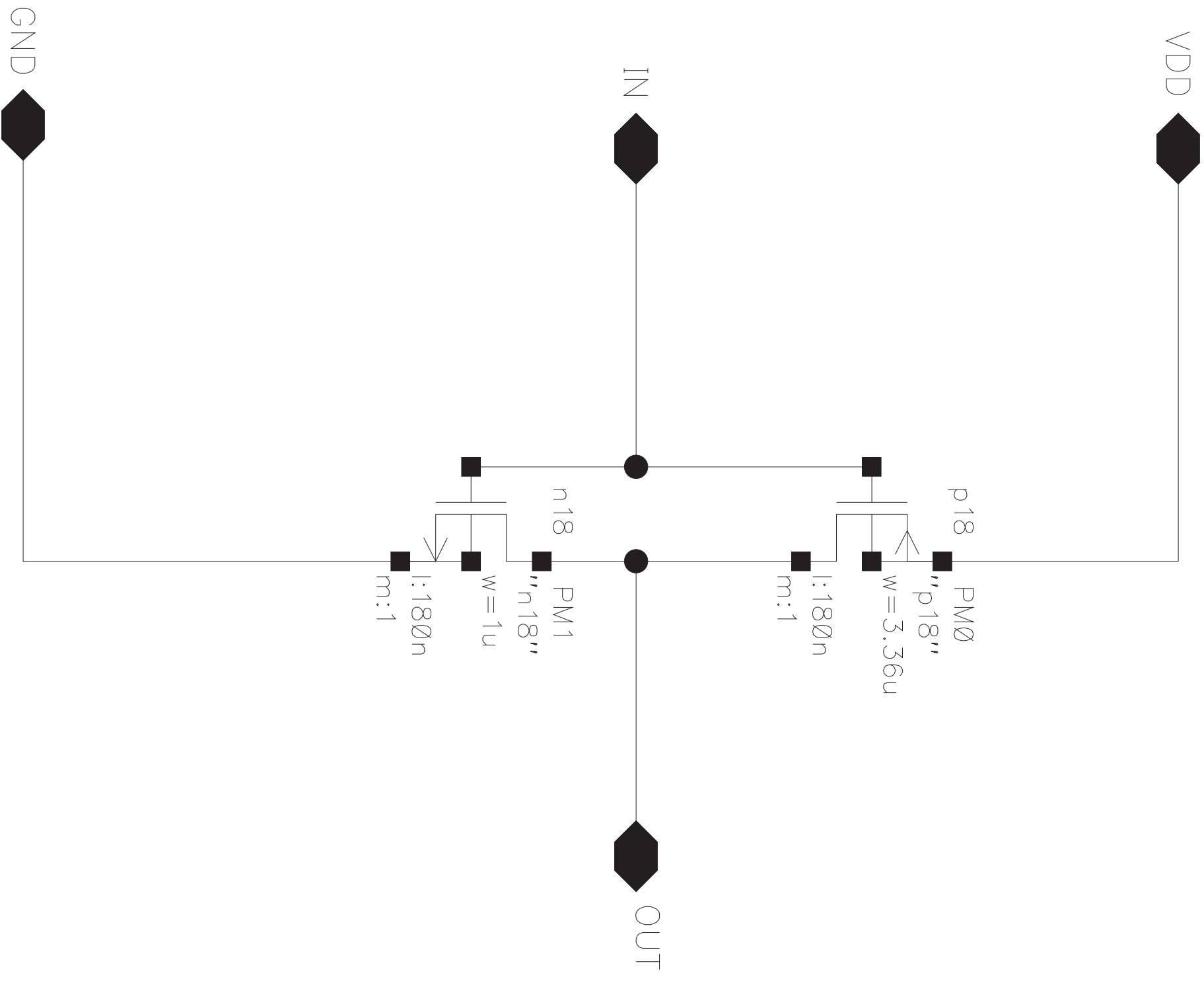




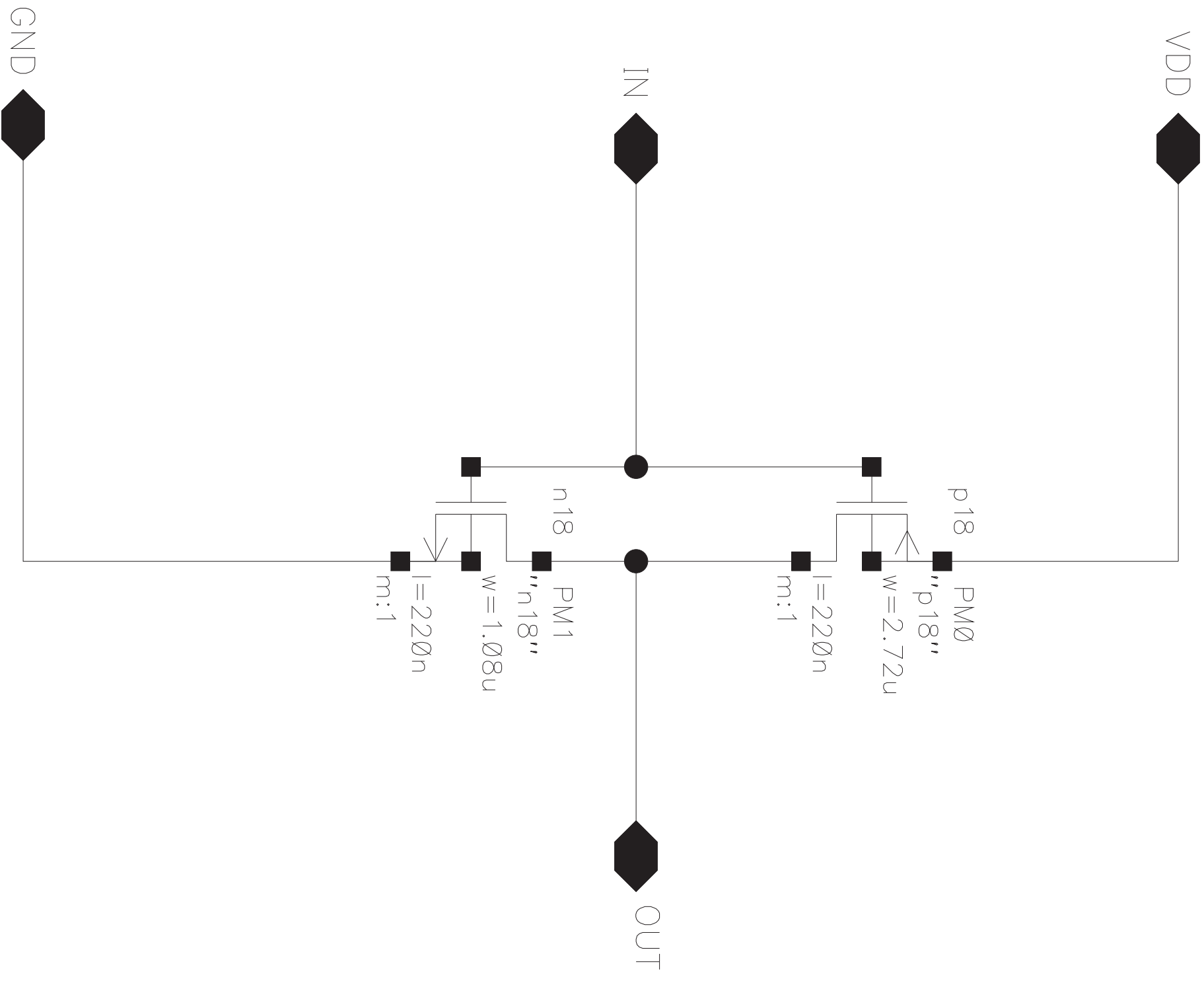
CP\_SPLIT\_DELAY\_CHAIN  
 1 JUL  
 MENG CHU

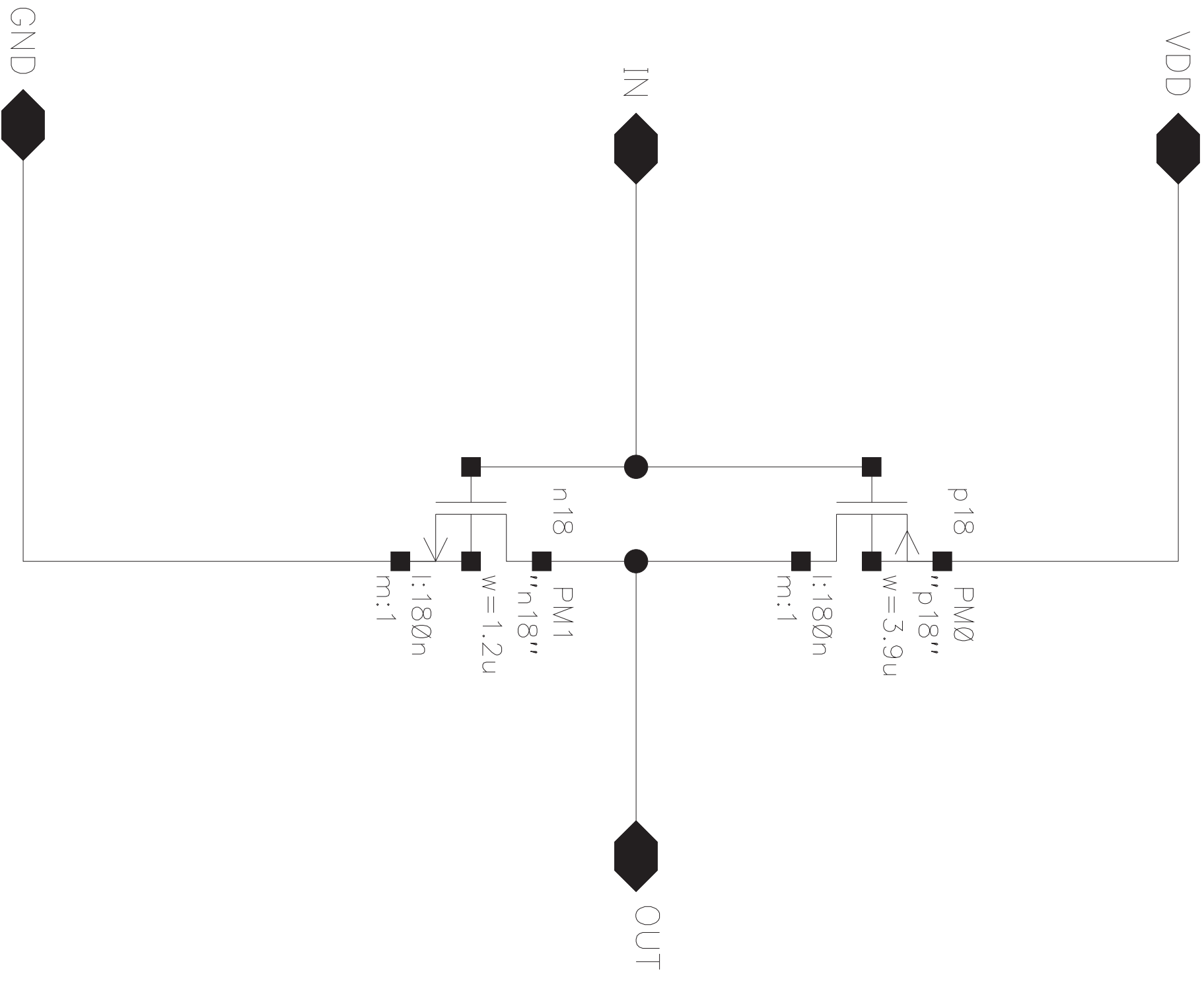


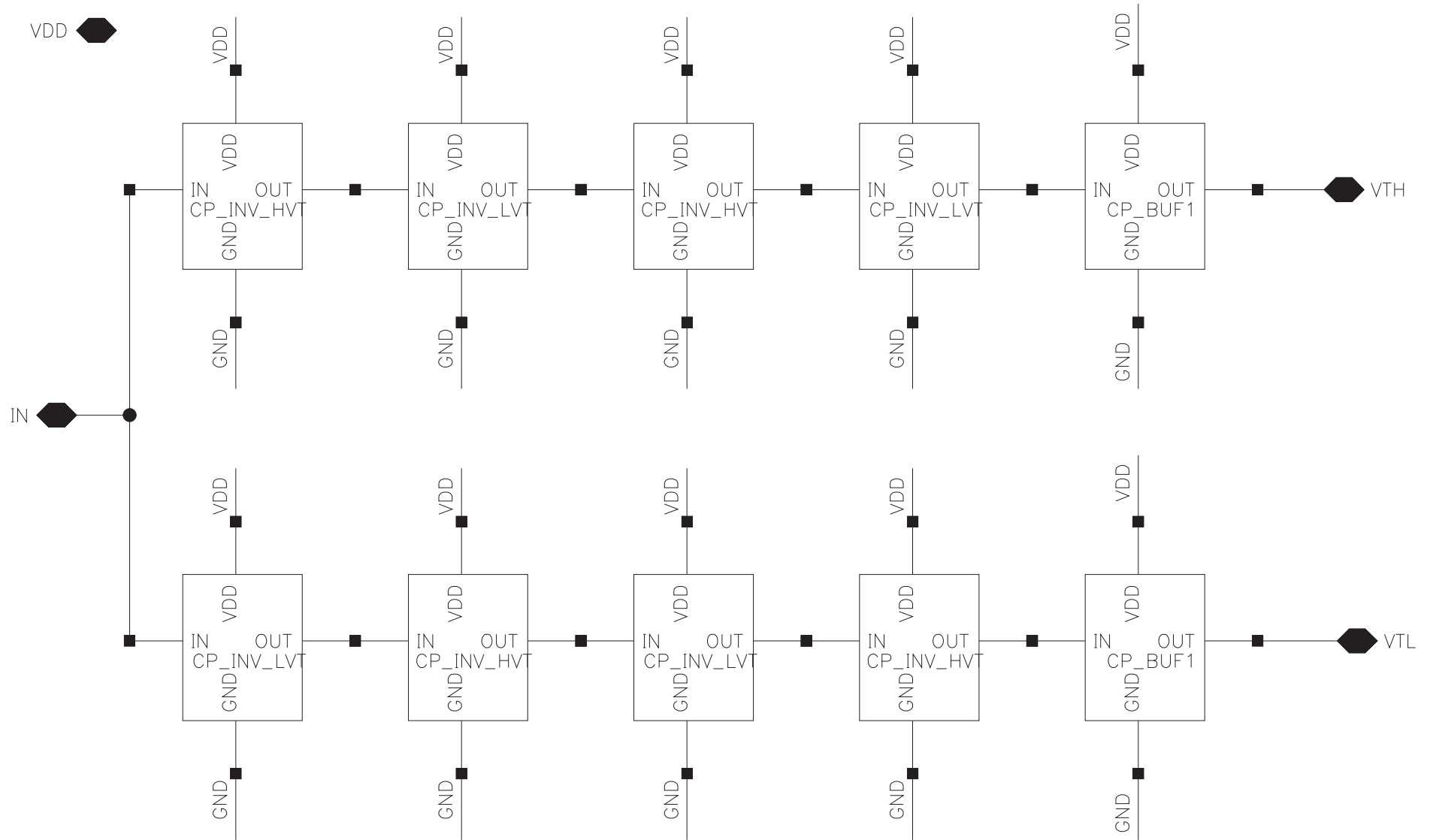




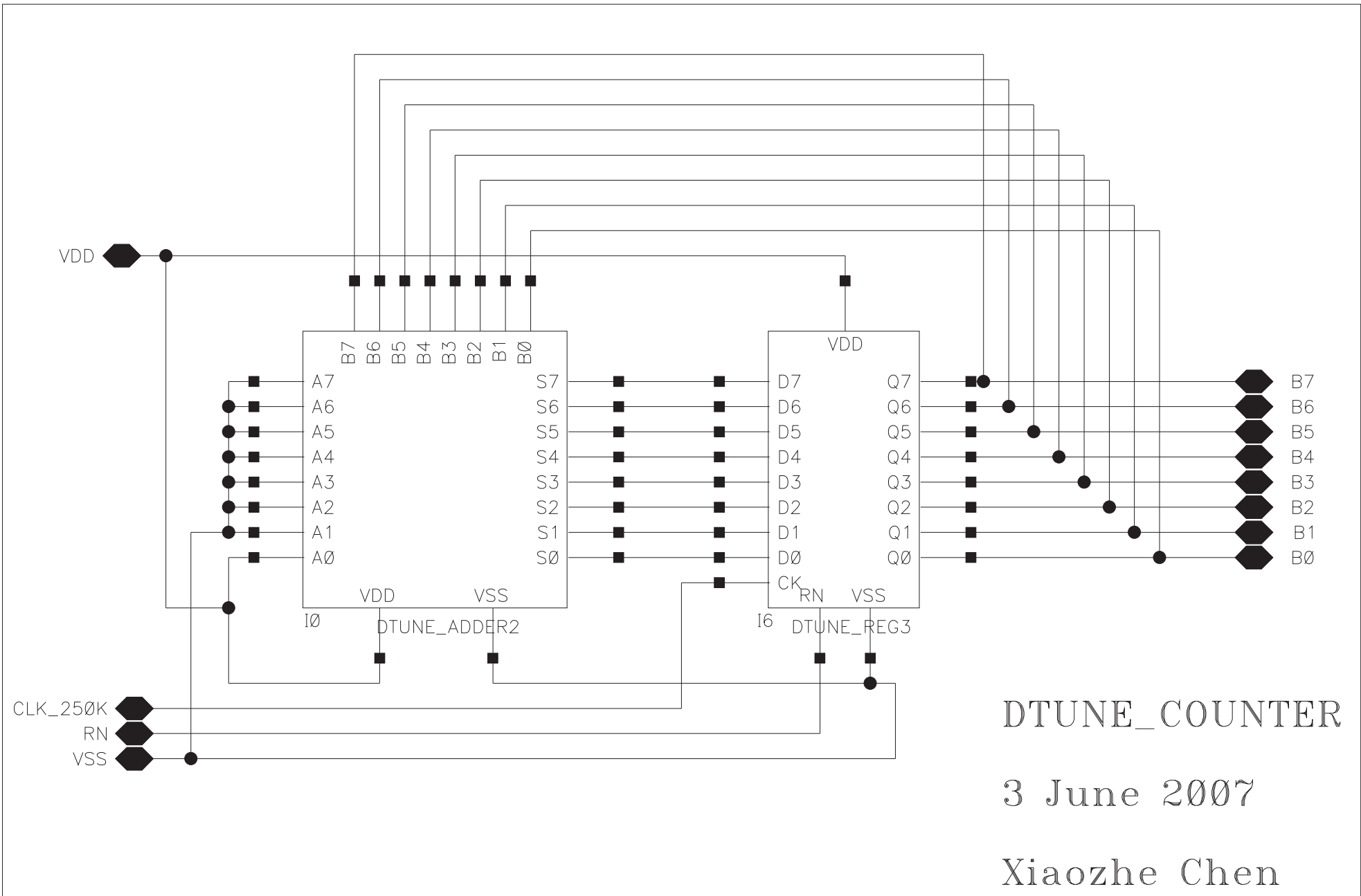








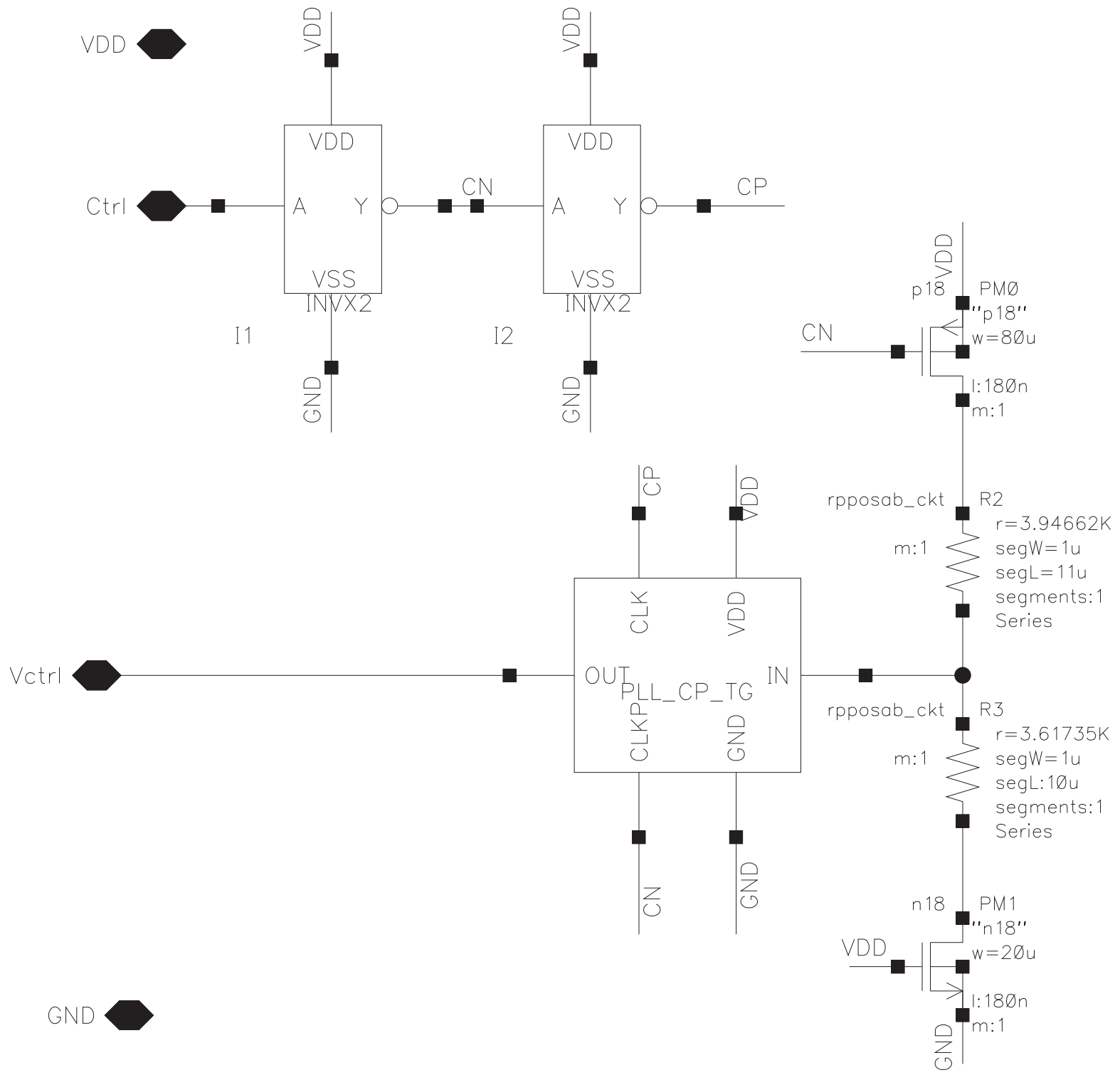
CP\_SPLIT\_VT\_CHAIN  
 3 JUL  
 MENG CHU



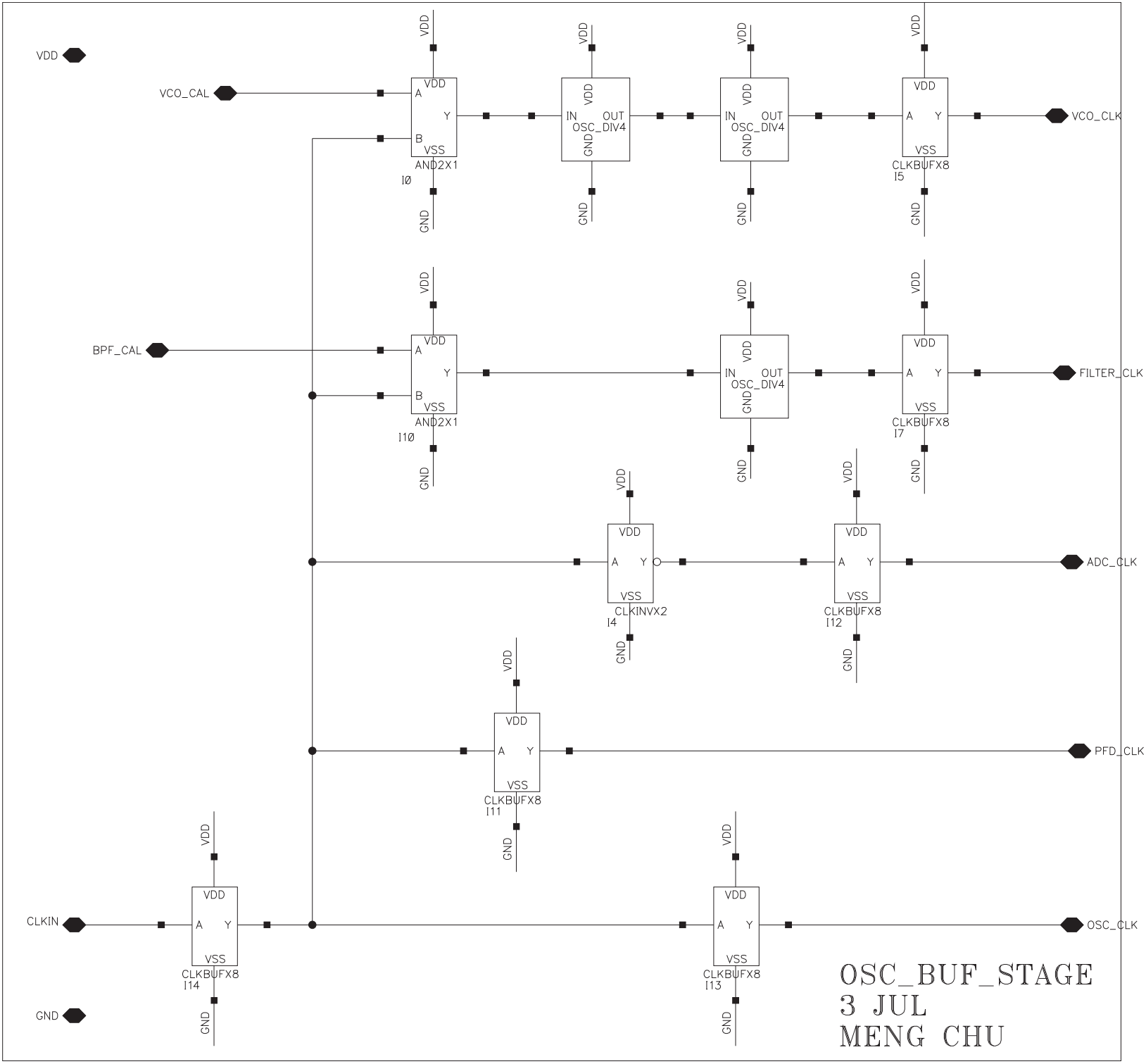
DTUNE\_COUNTER

3 June 2007

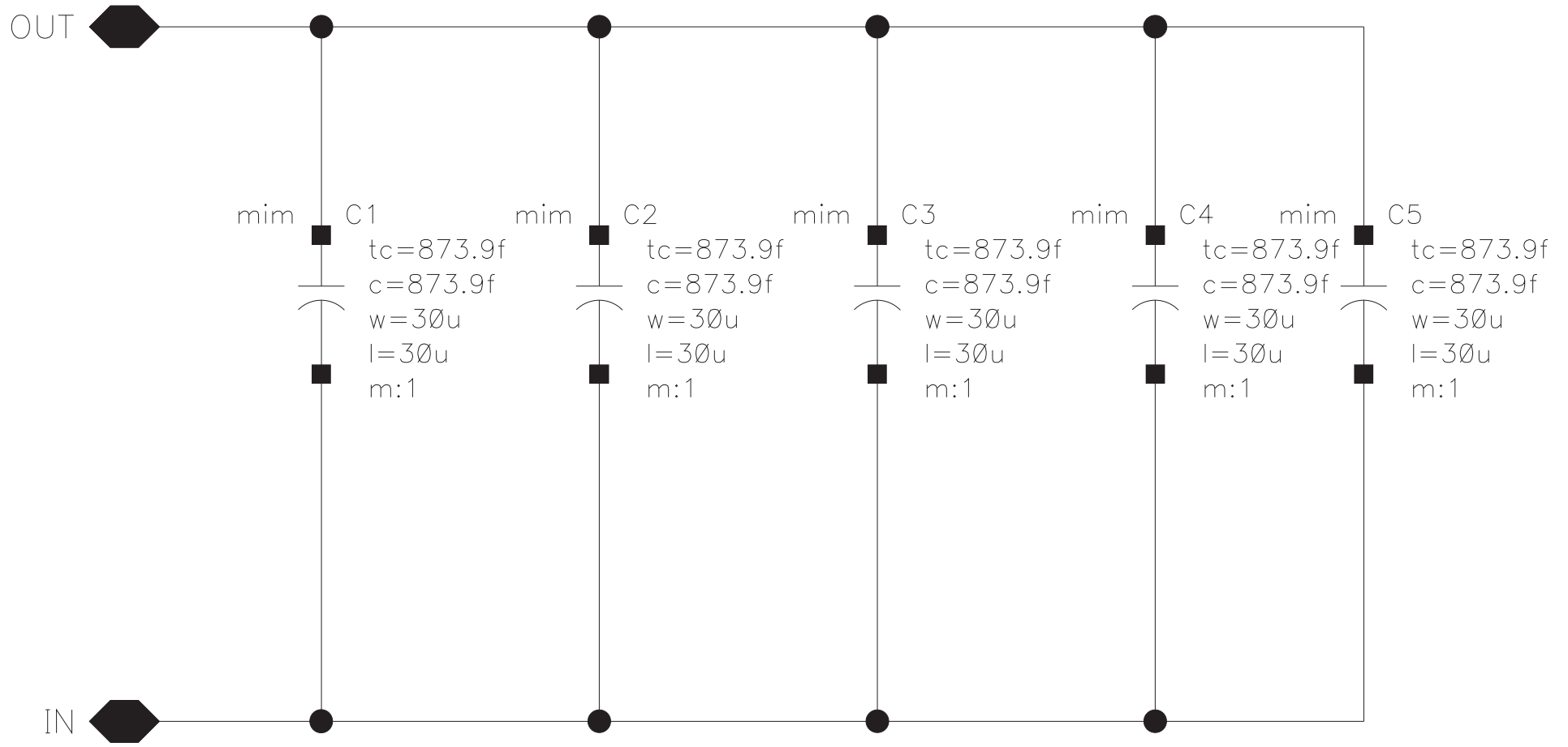
Xiaozhe Chen



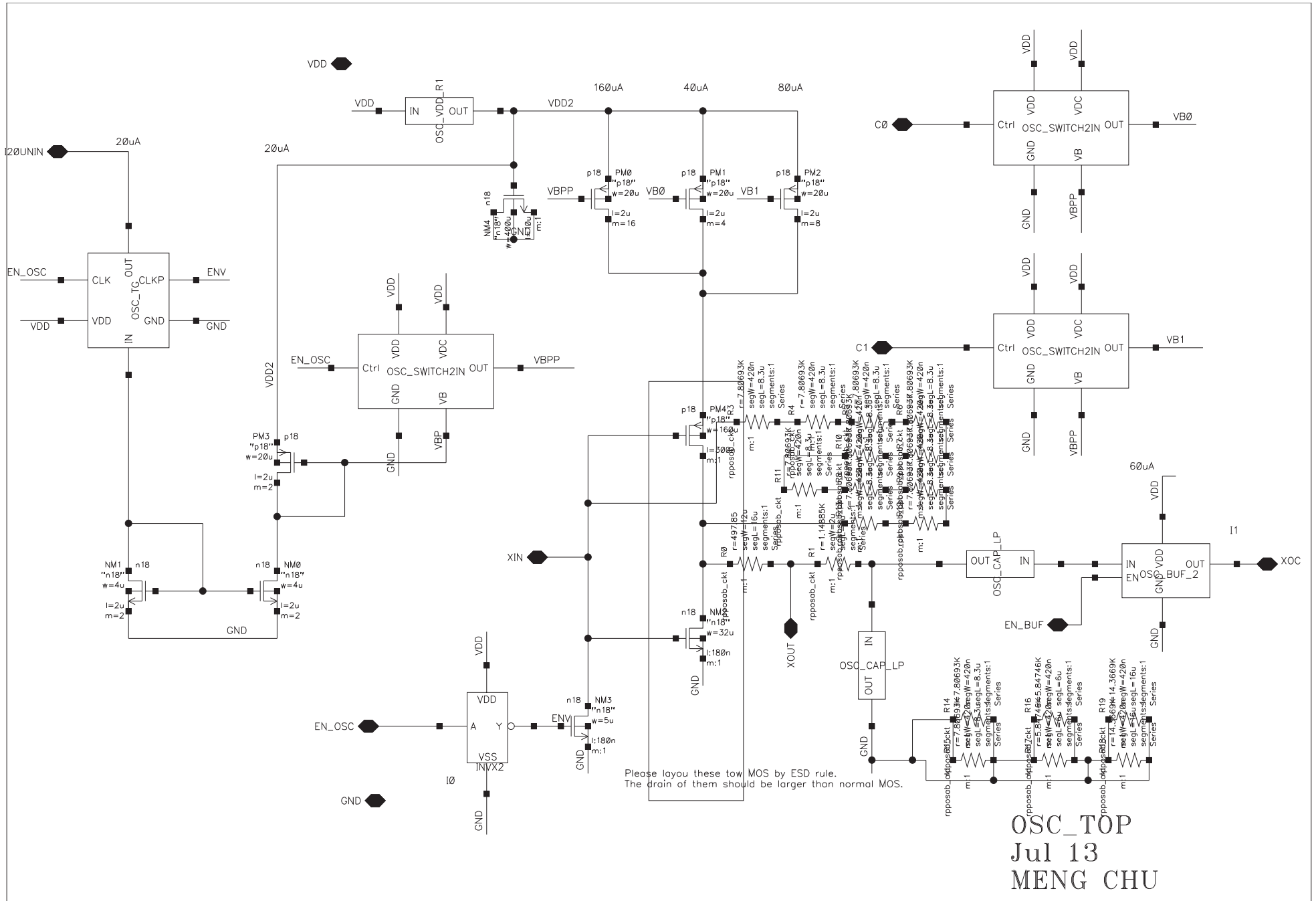




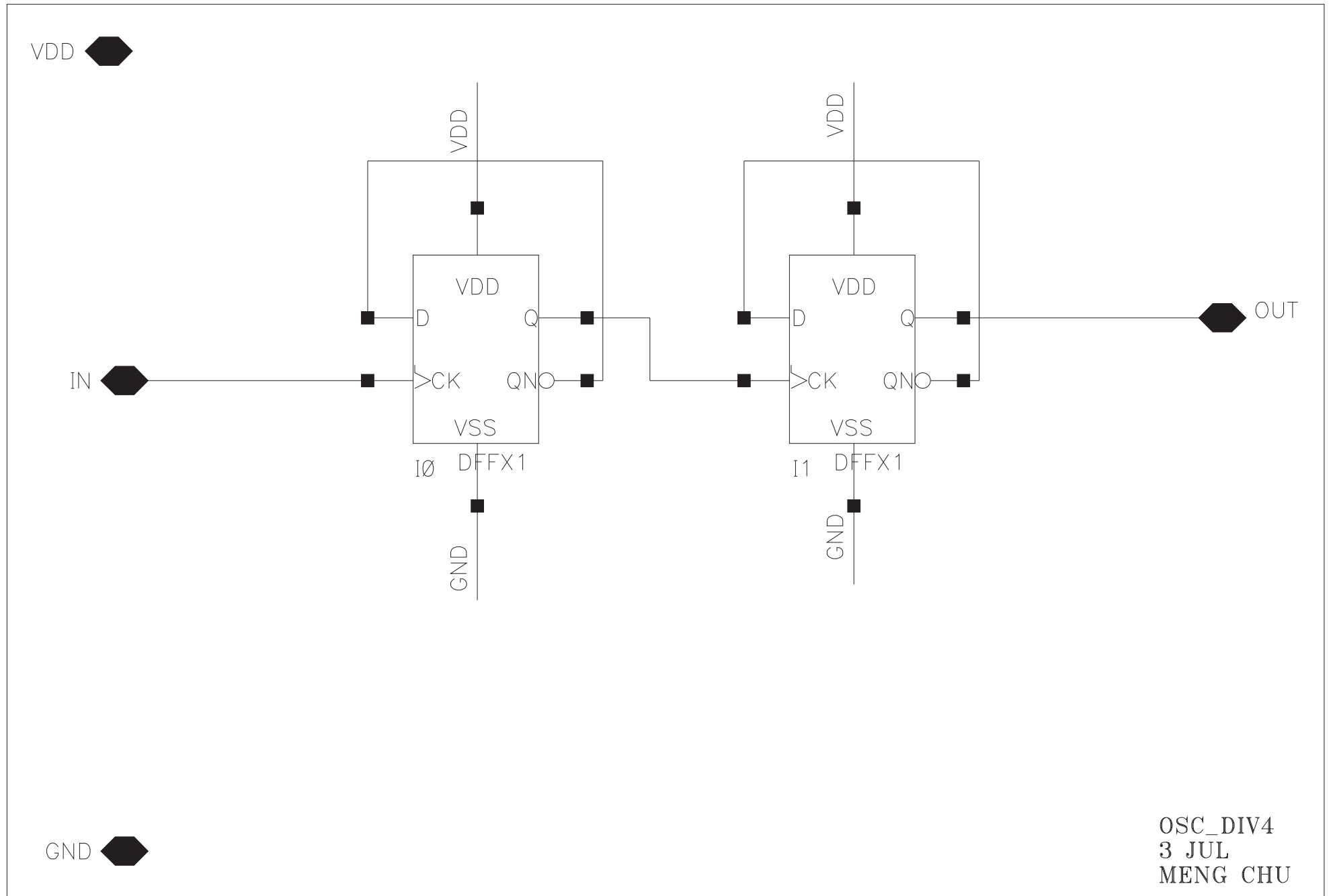
OSC\_BUF\_STAGE  
 3 JUL  
 MENG CHU



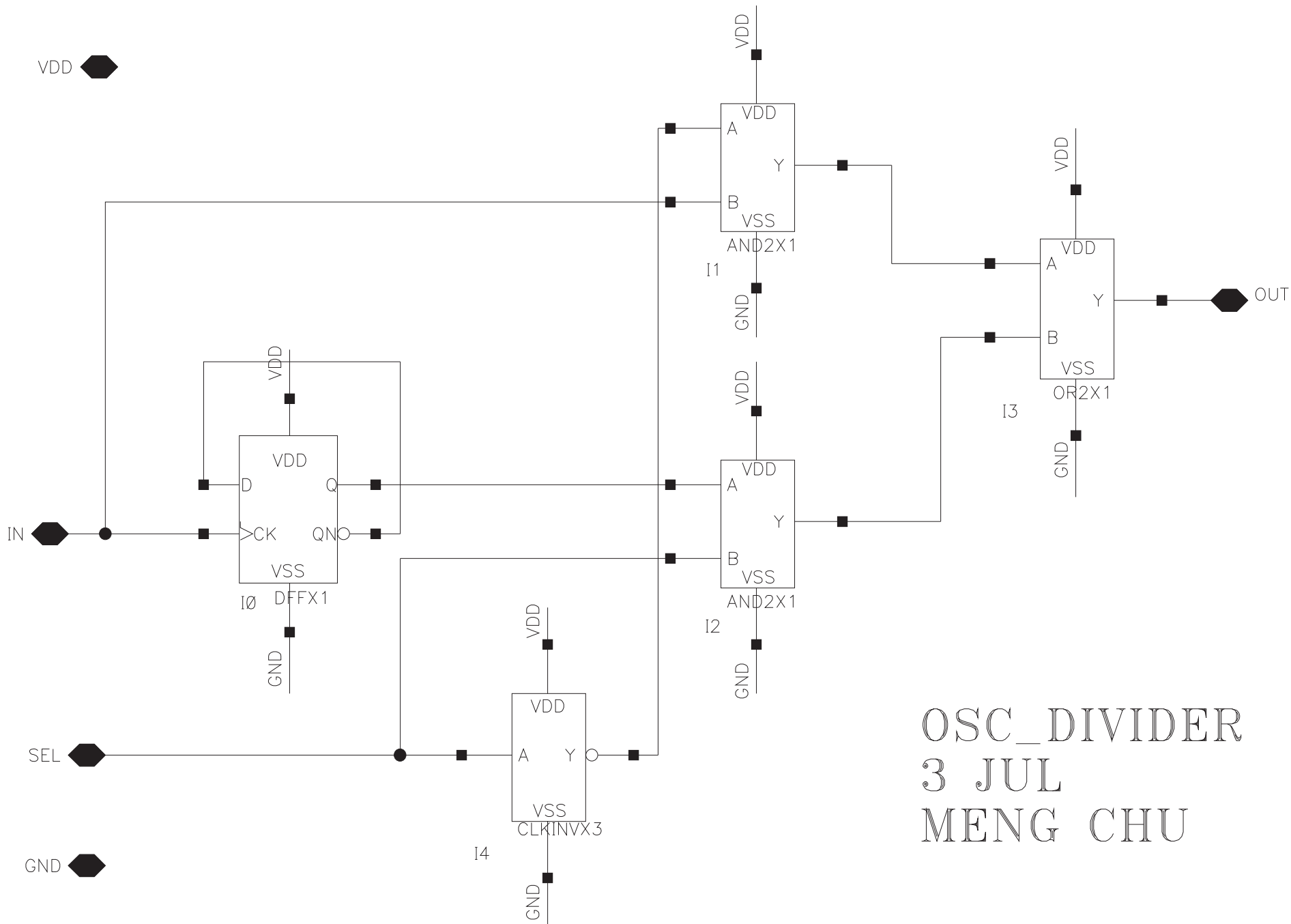




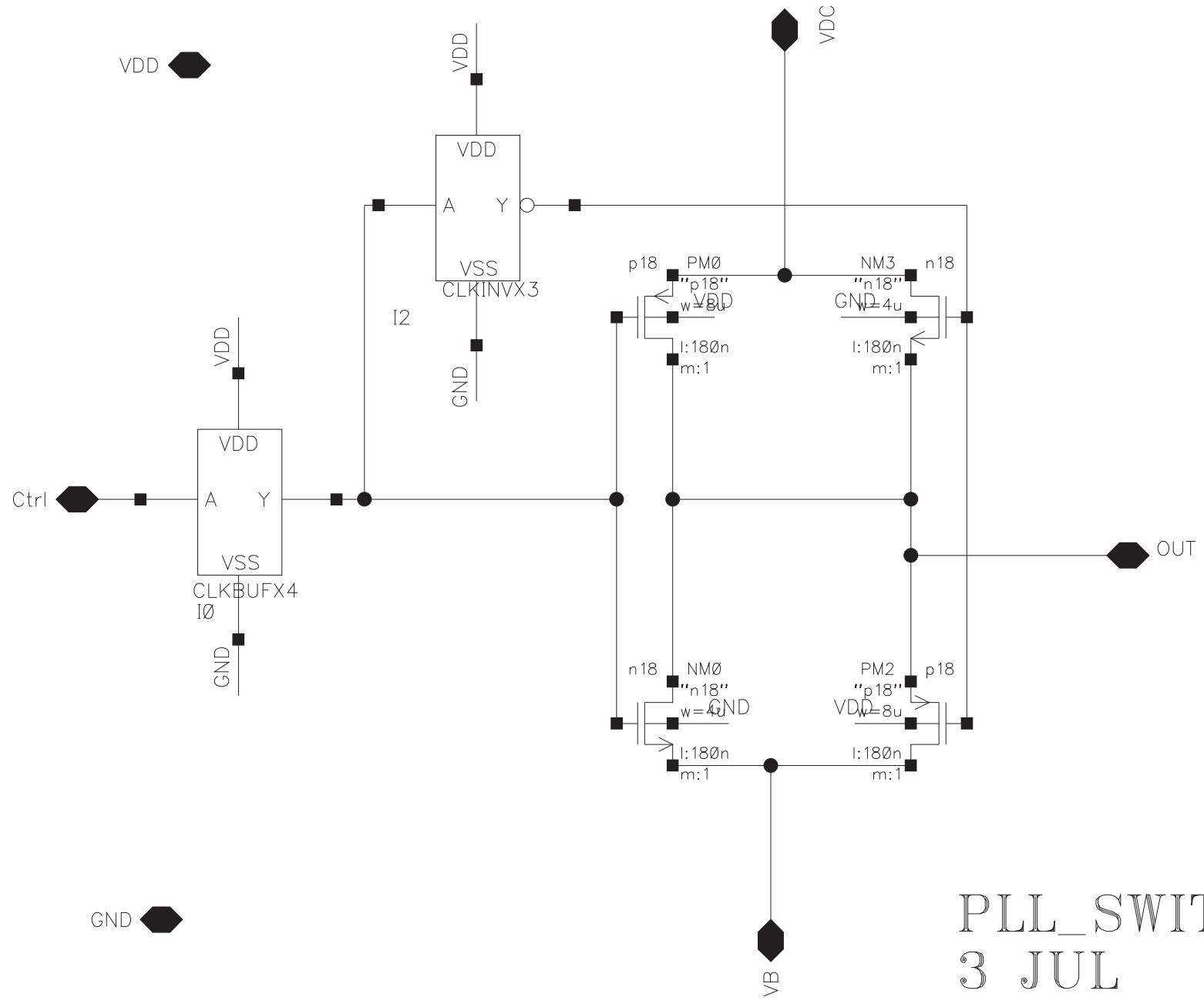
OSC\_TOP  
Jul 13  
MENG CHU



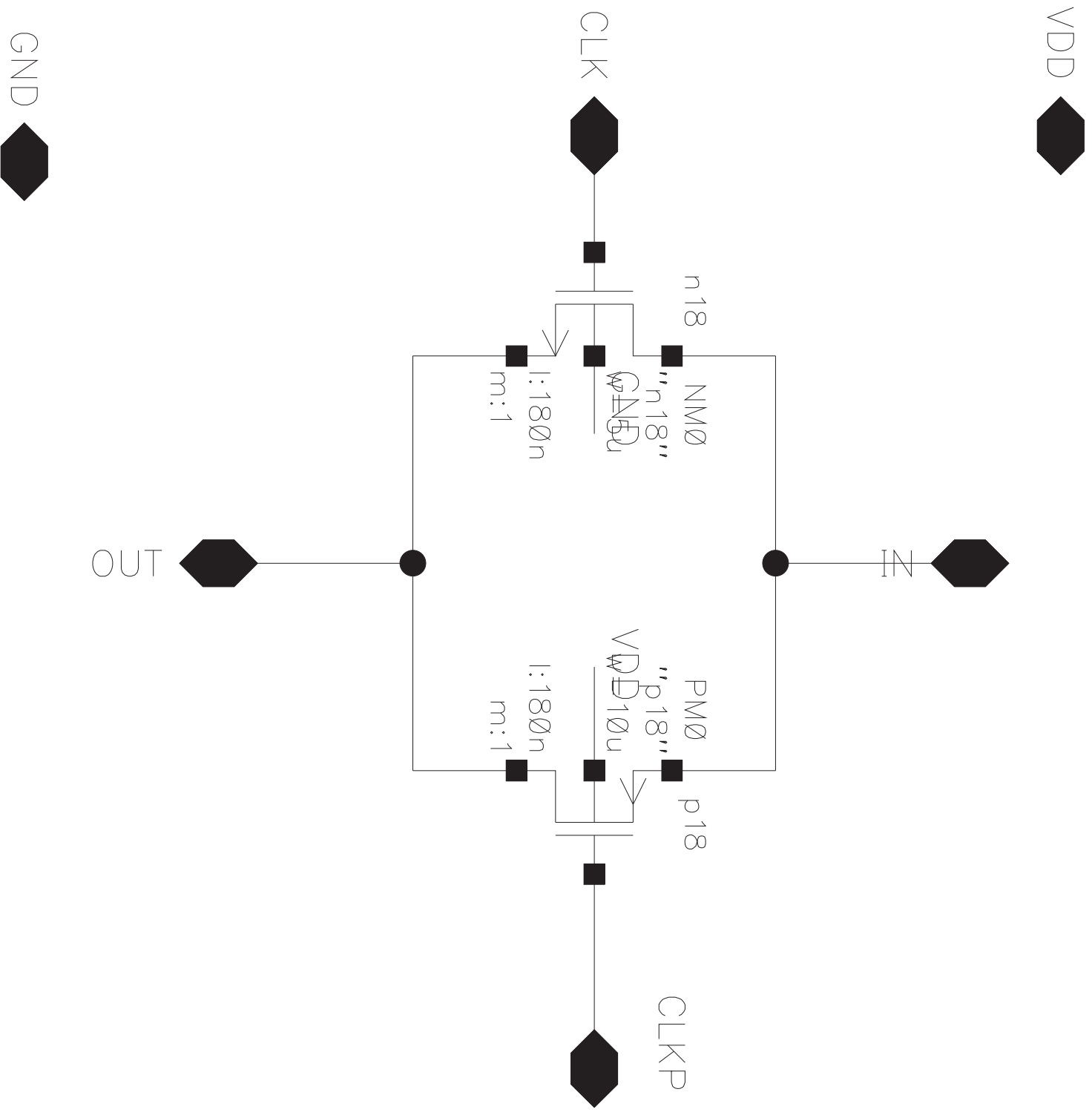


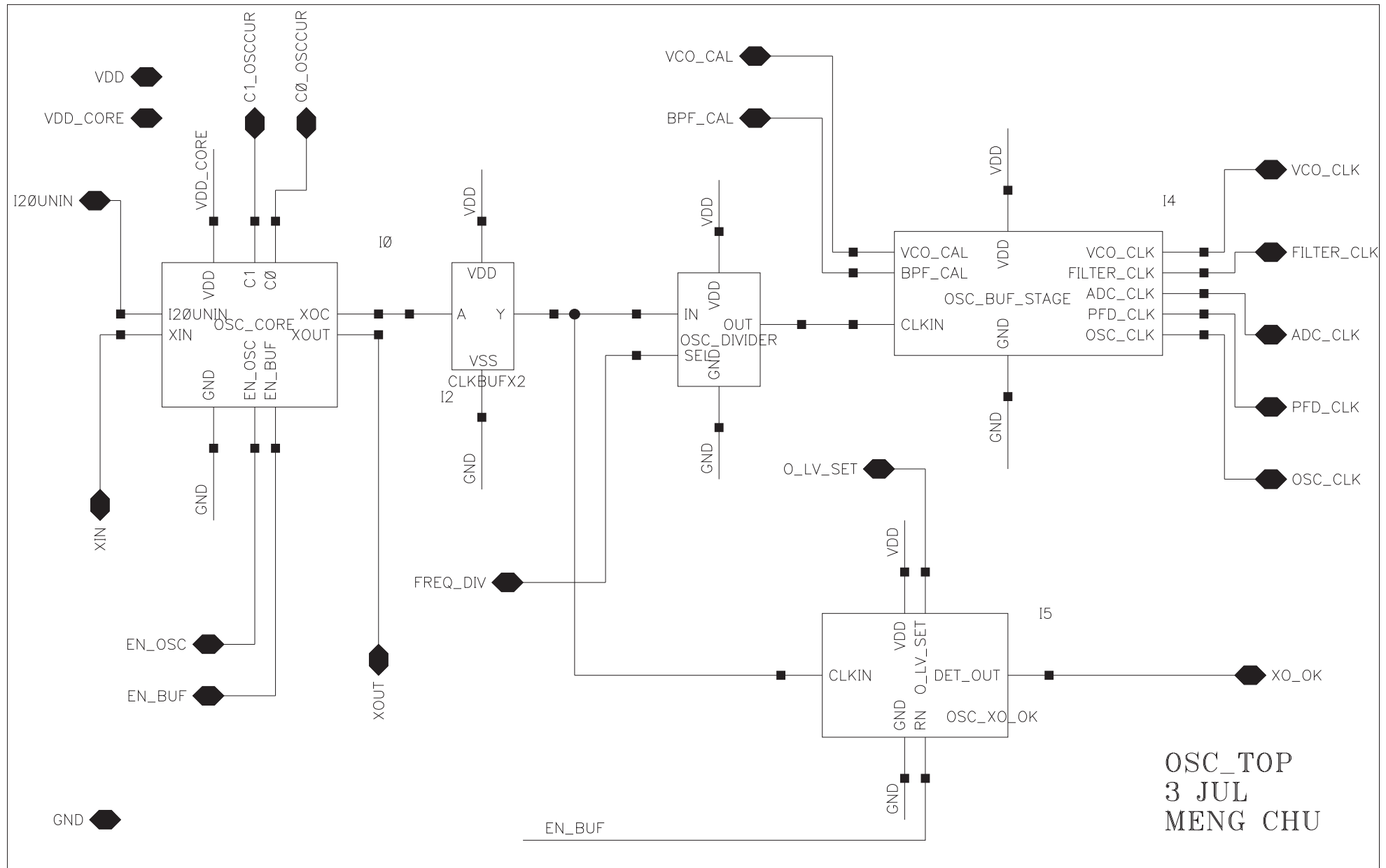


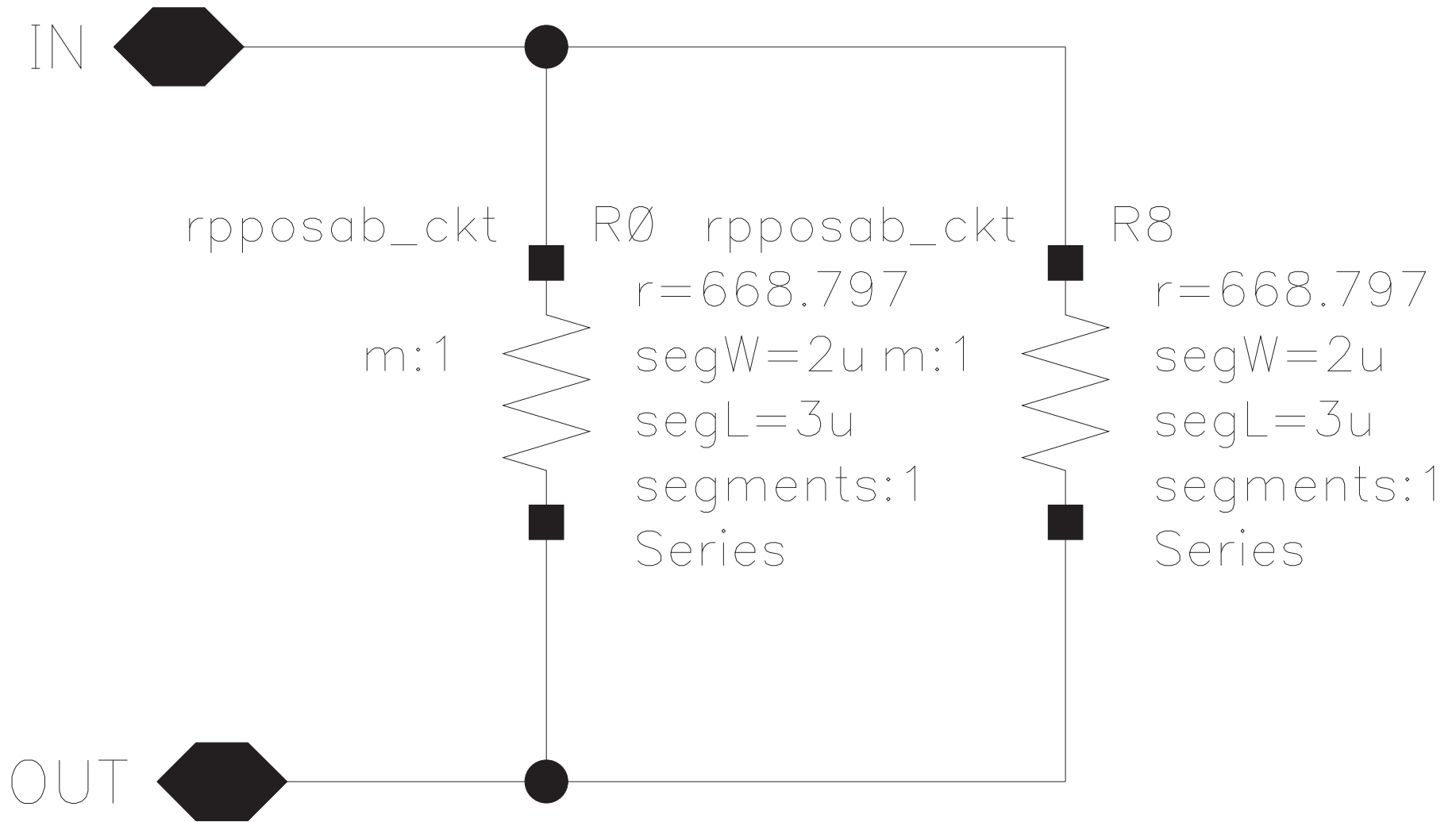
OSC\_DIVIDER  
 3 JUL  
 MENG CHU



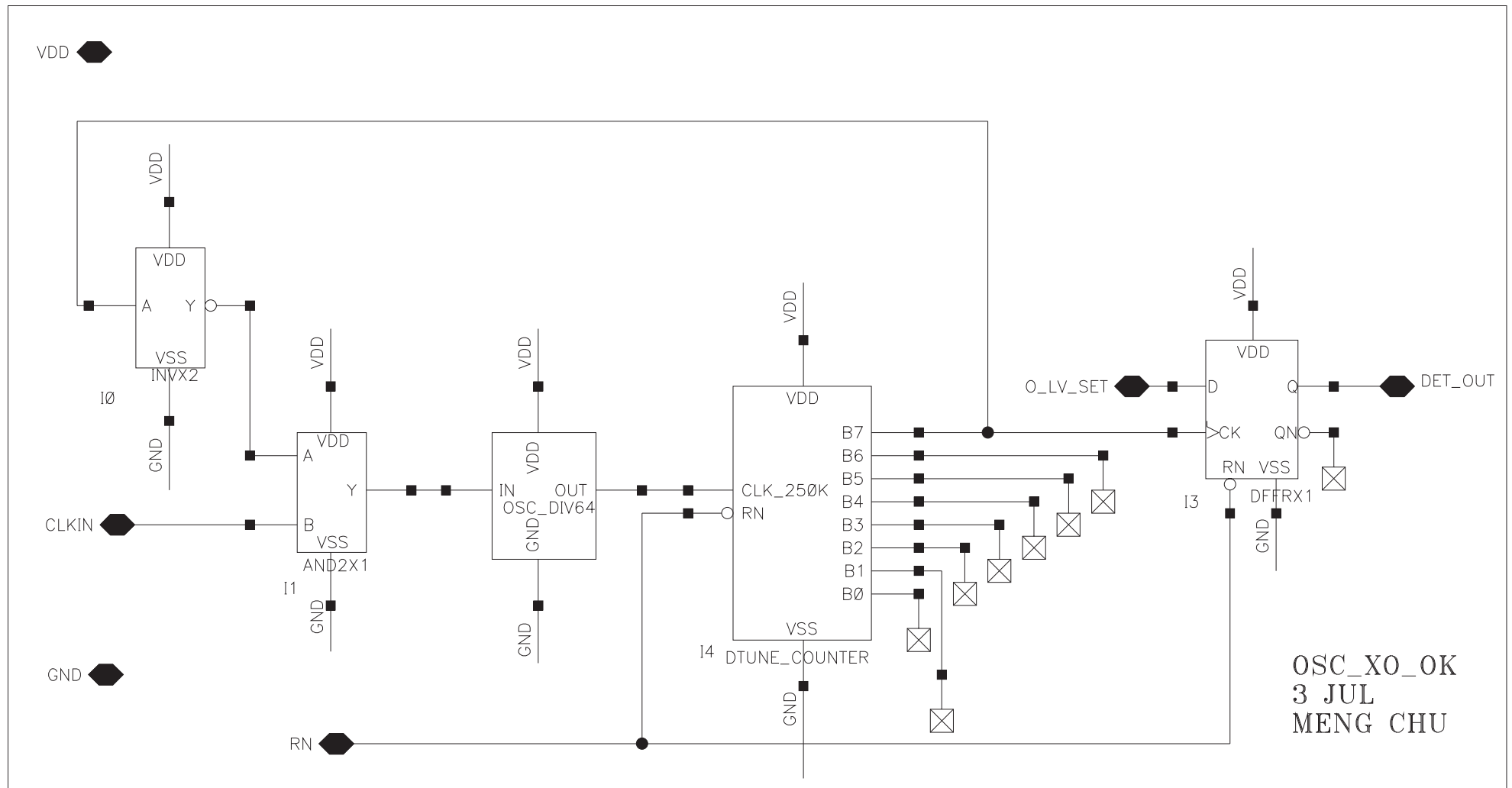
PLL\_SWITCH2IN  
 3 JUL  
 MENG CHU

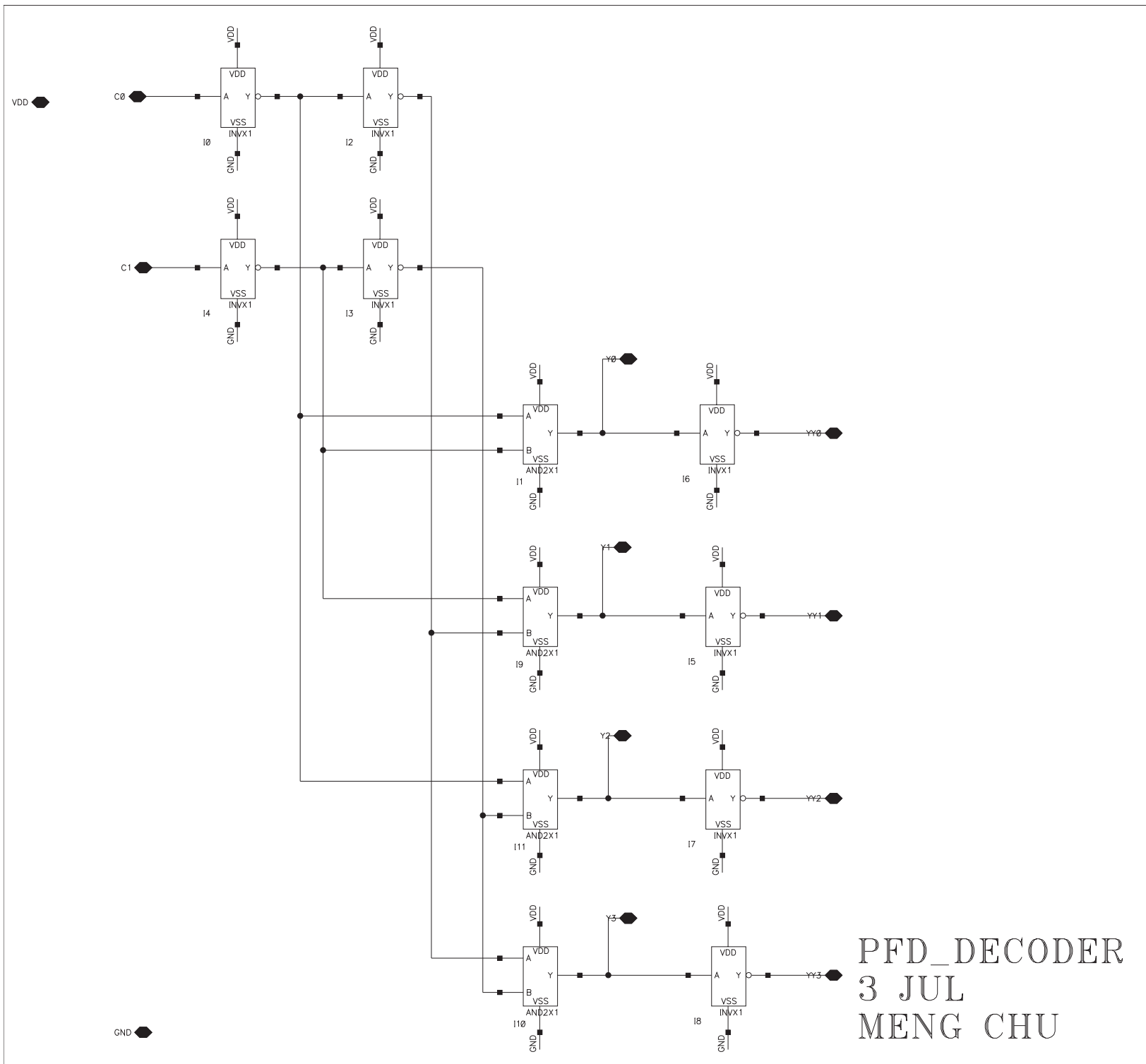




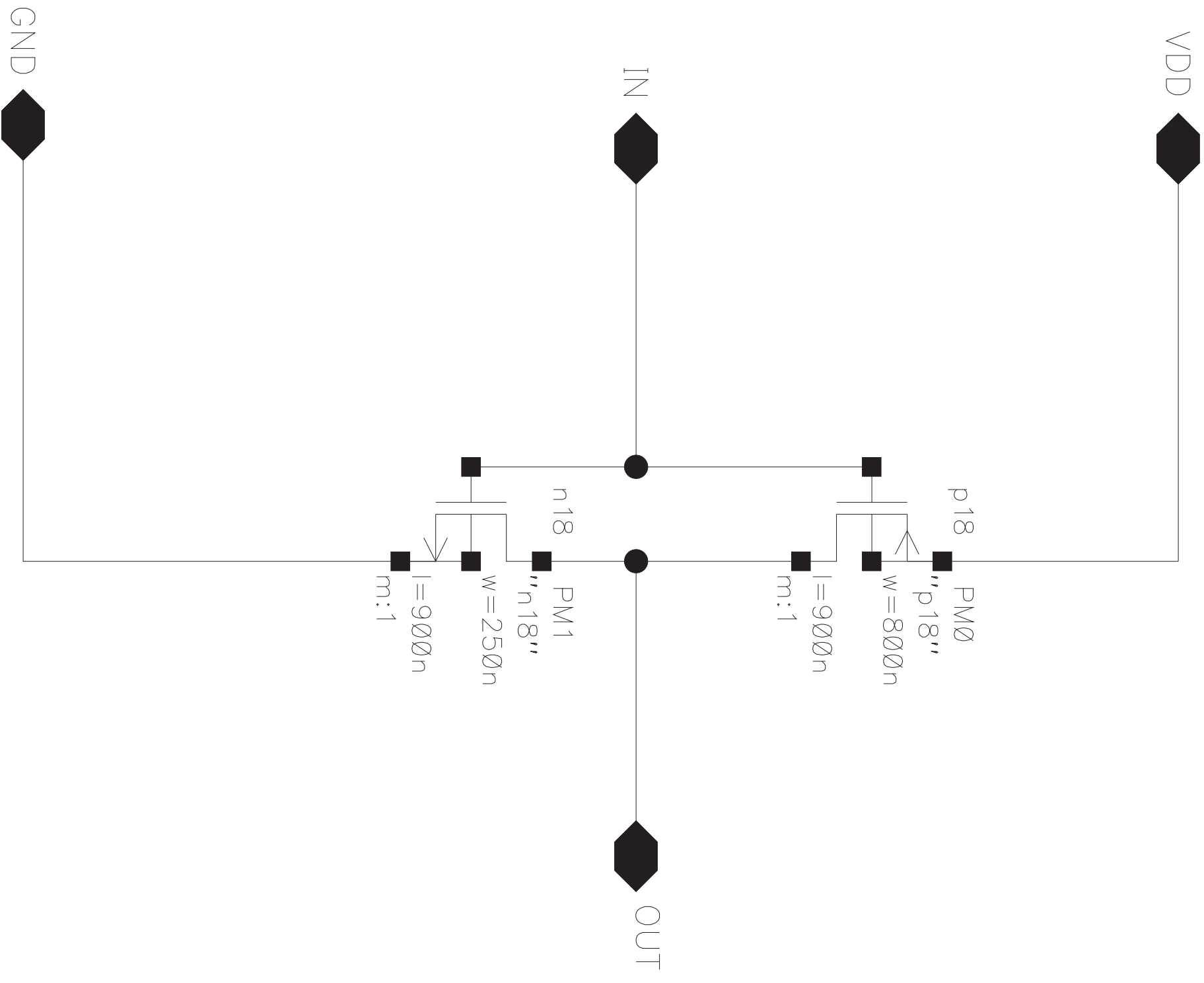




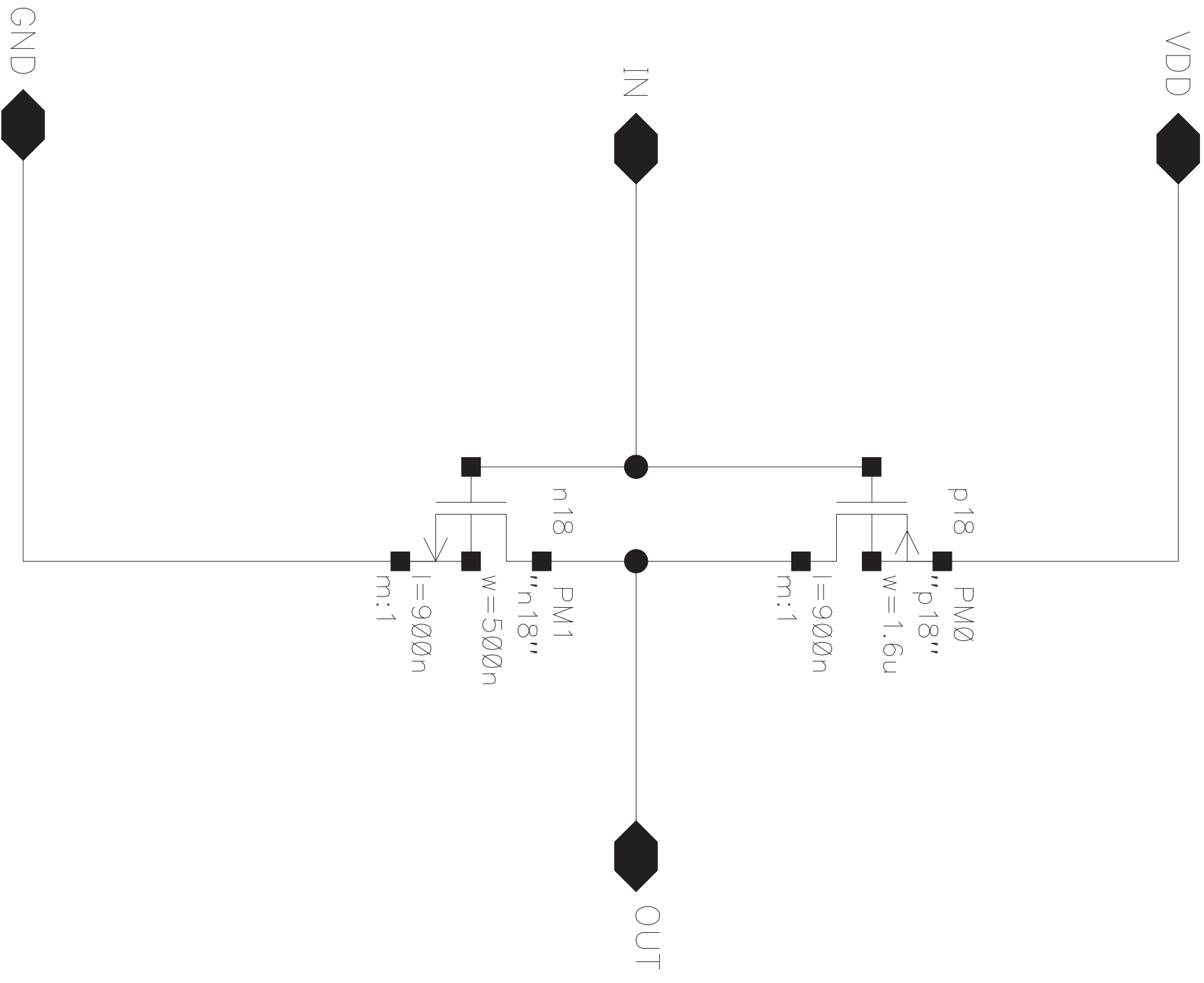




PFD\_DECODER  
 3 JUL  
 MENG CHU



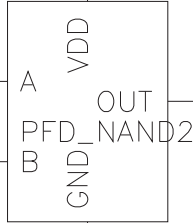




VDD

A

VDD

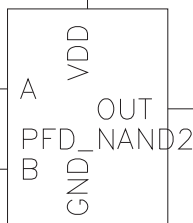


AOUT

GND

VDD

B

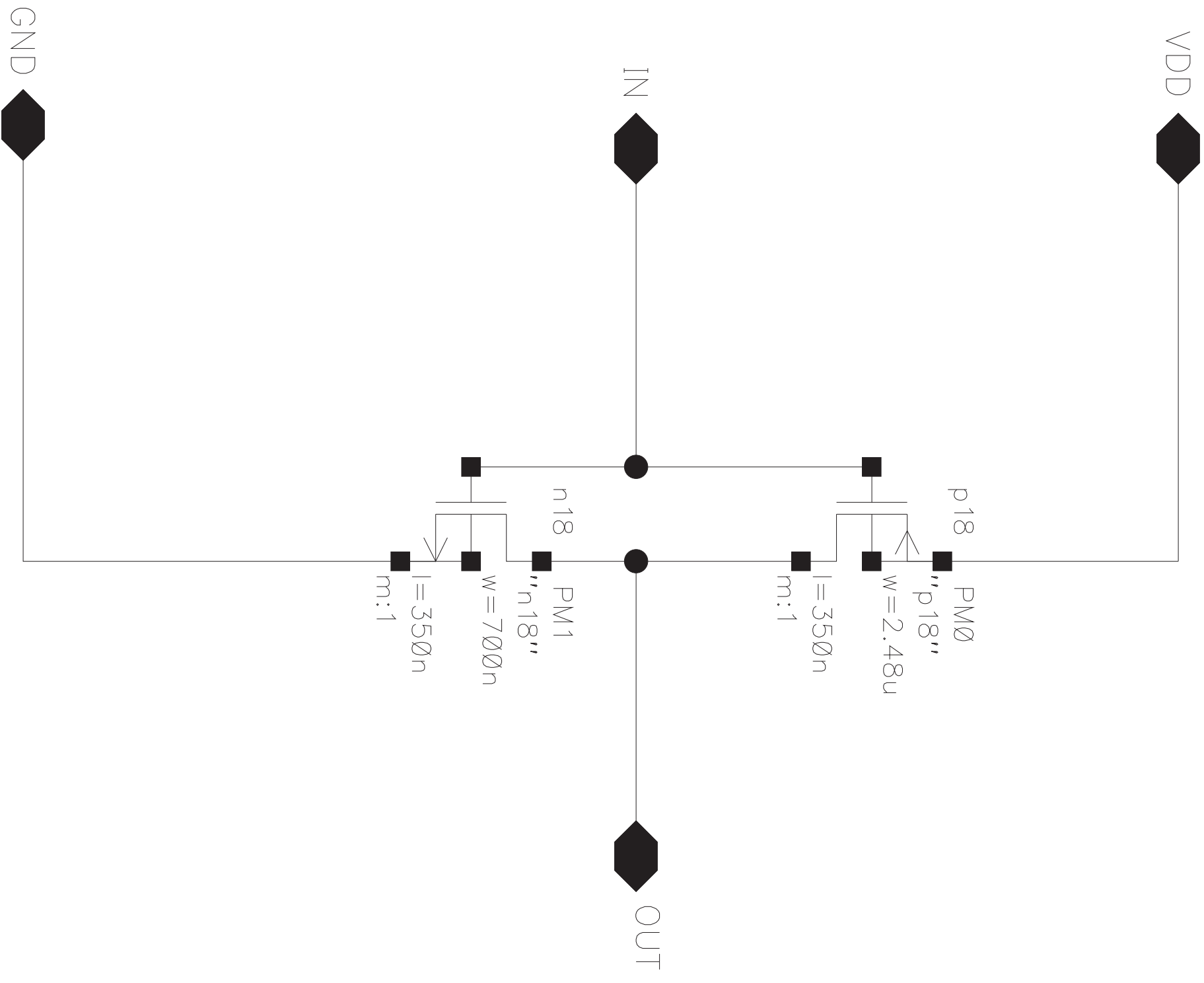


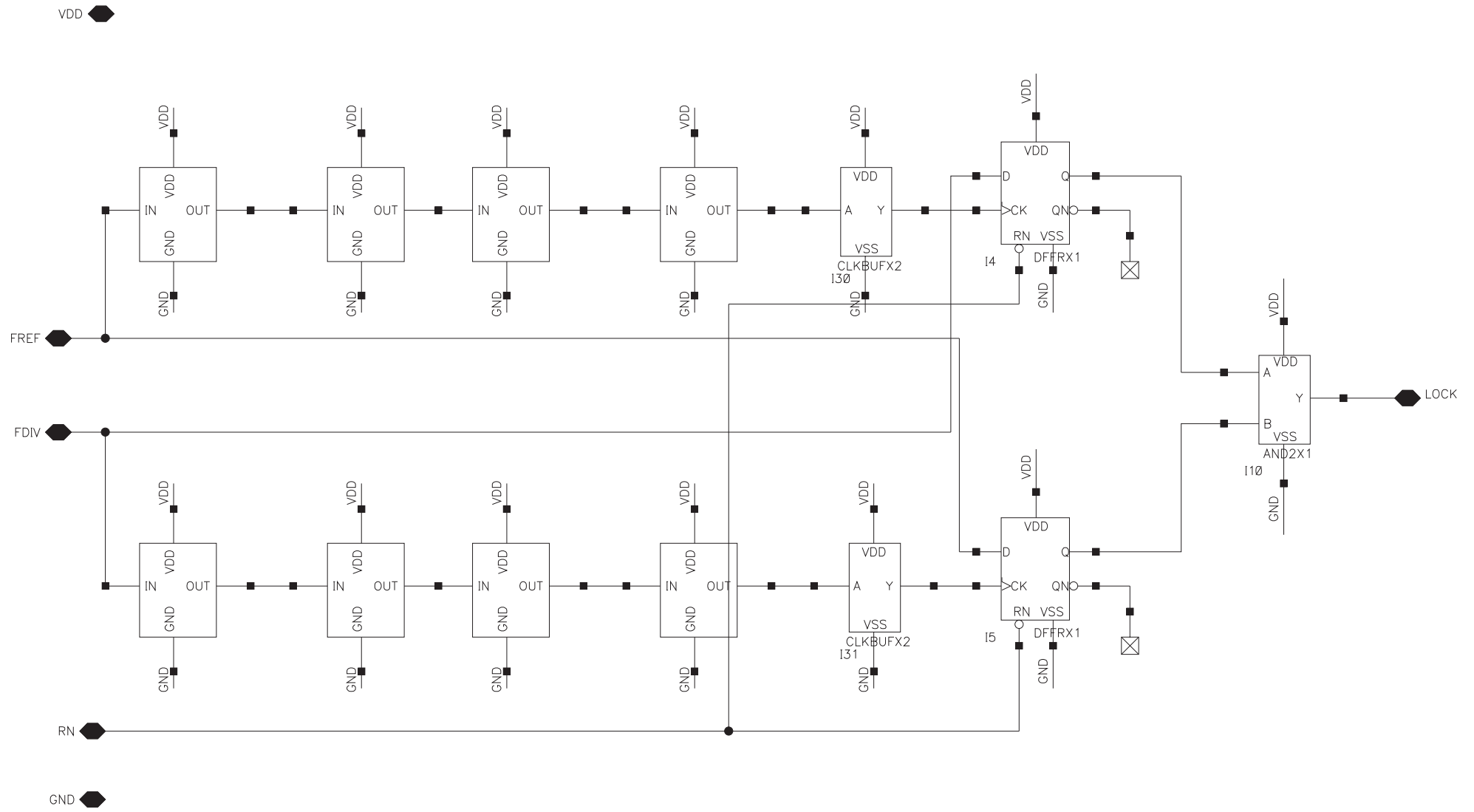
BOUT

GND

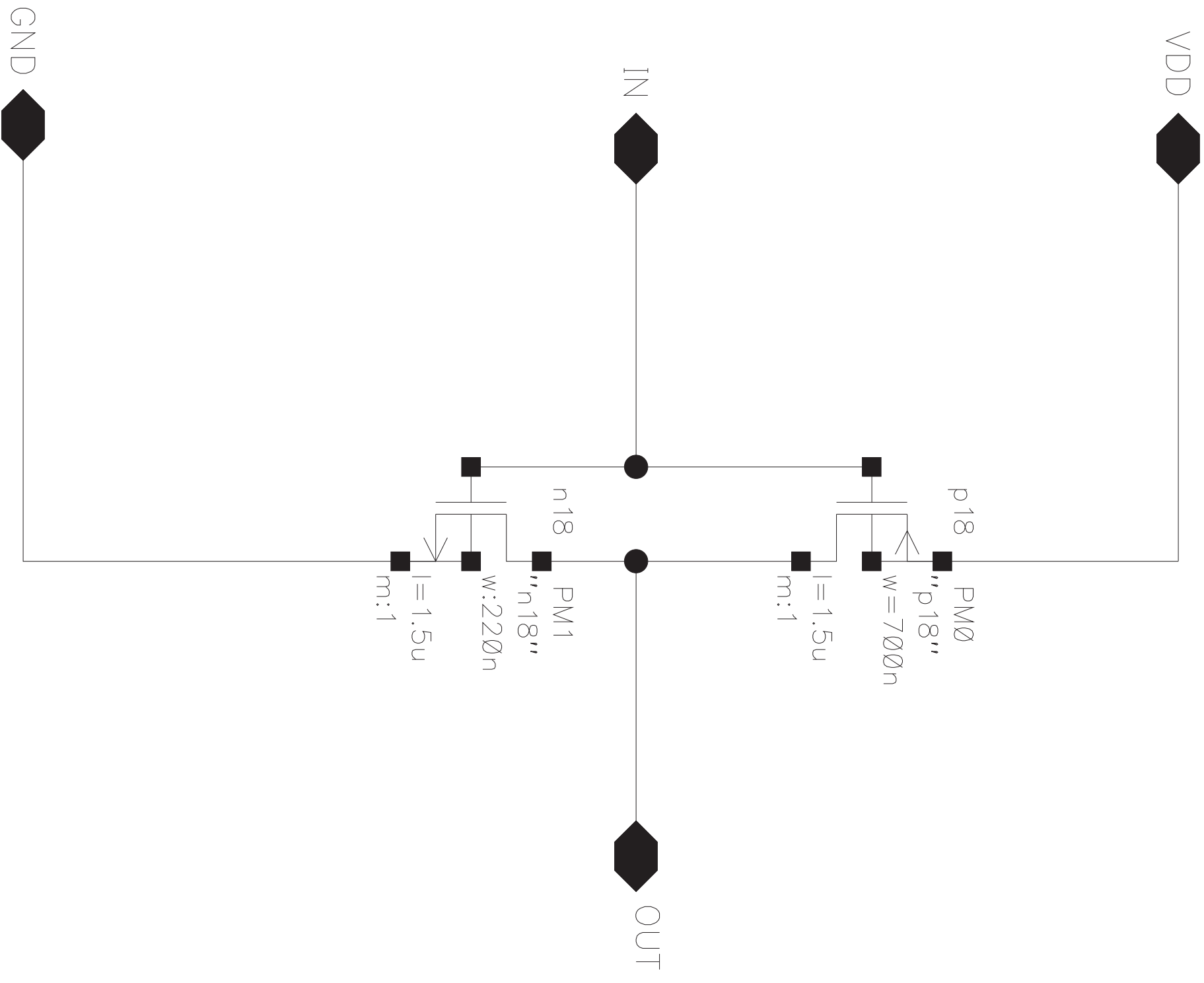
GND

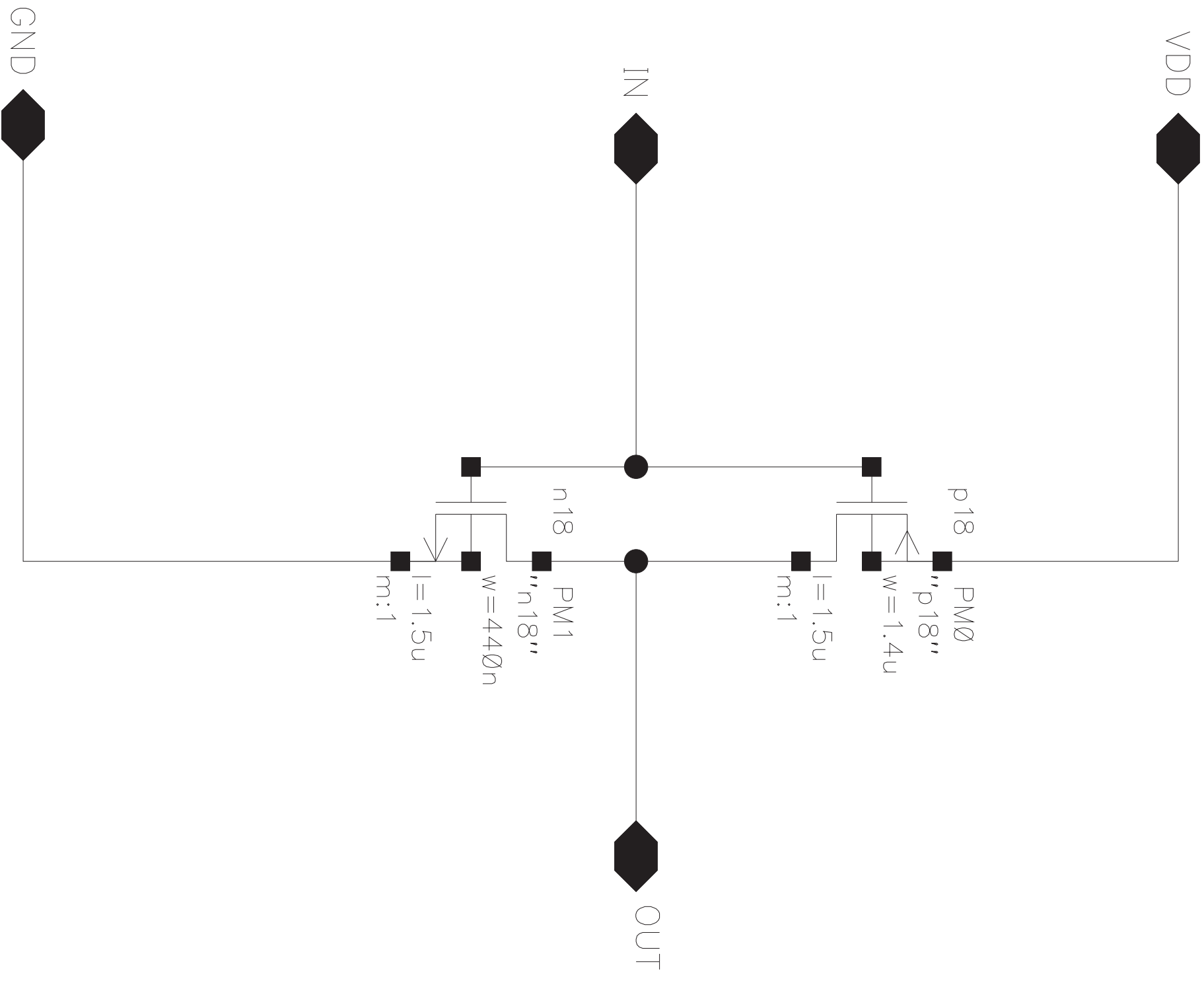
PFD\_DFF\_DUAL\_NAND  
3 JUL  
MENG CHU

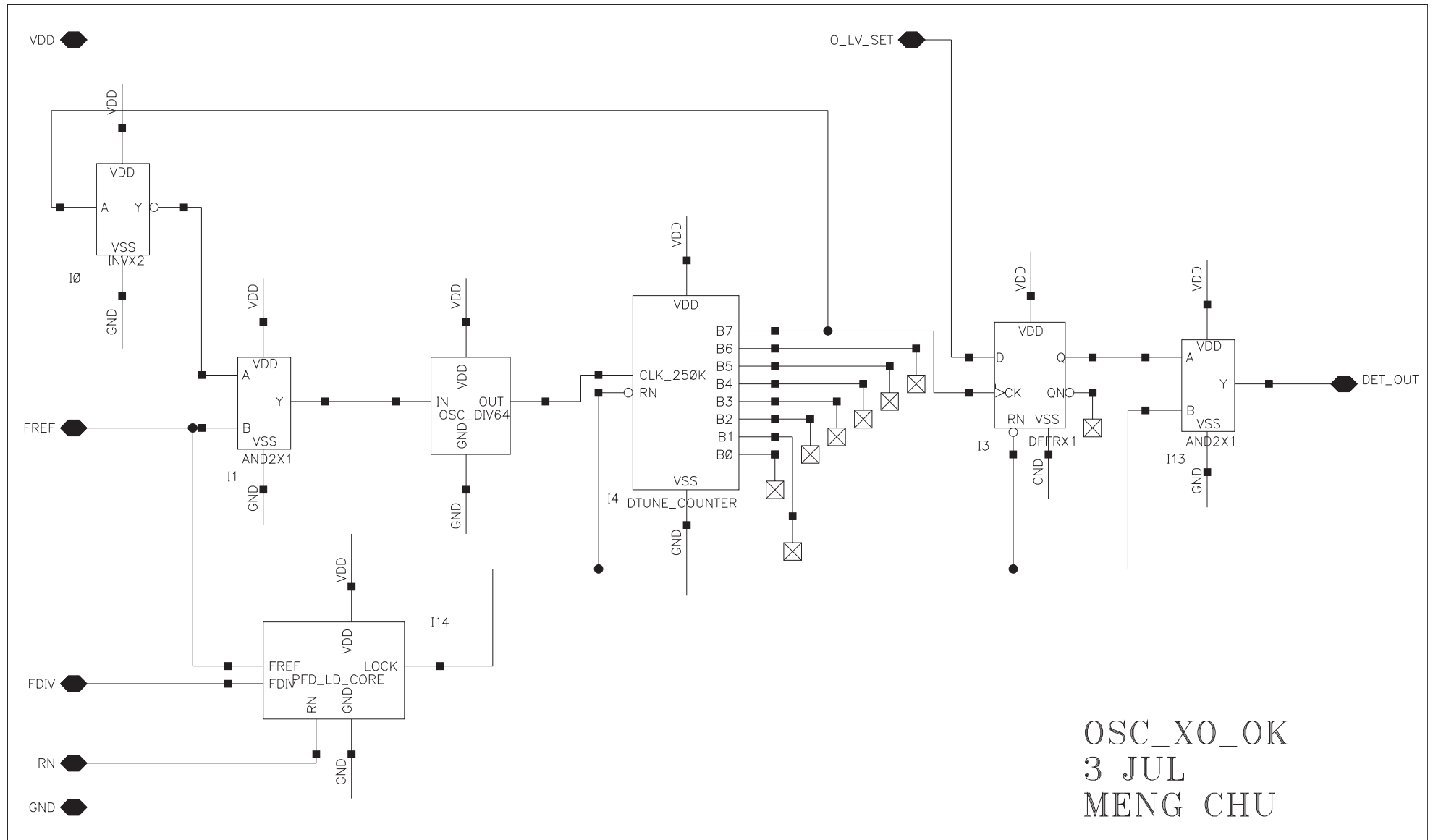


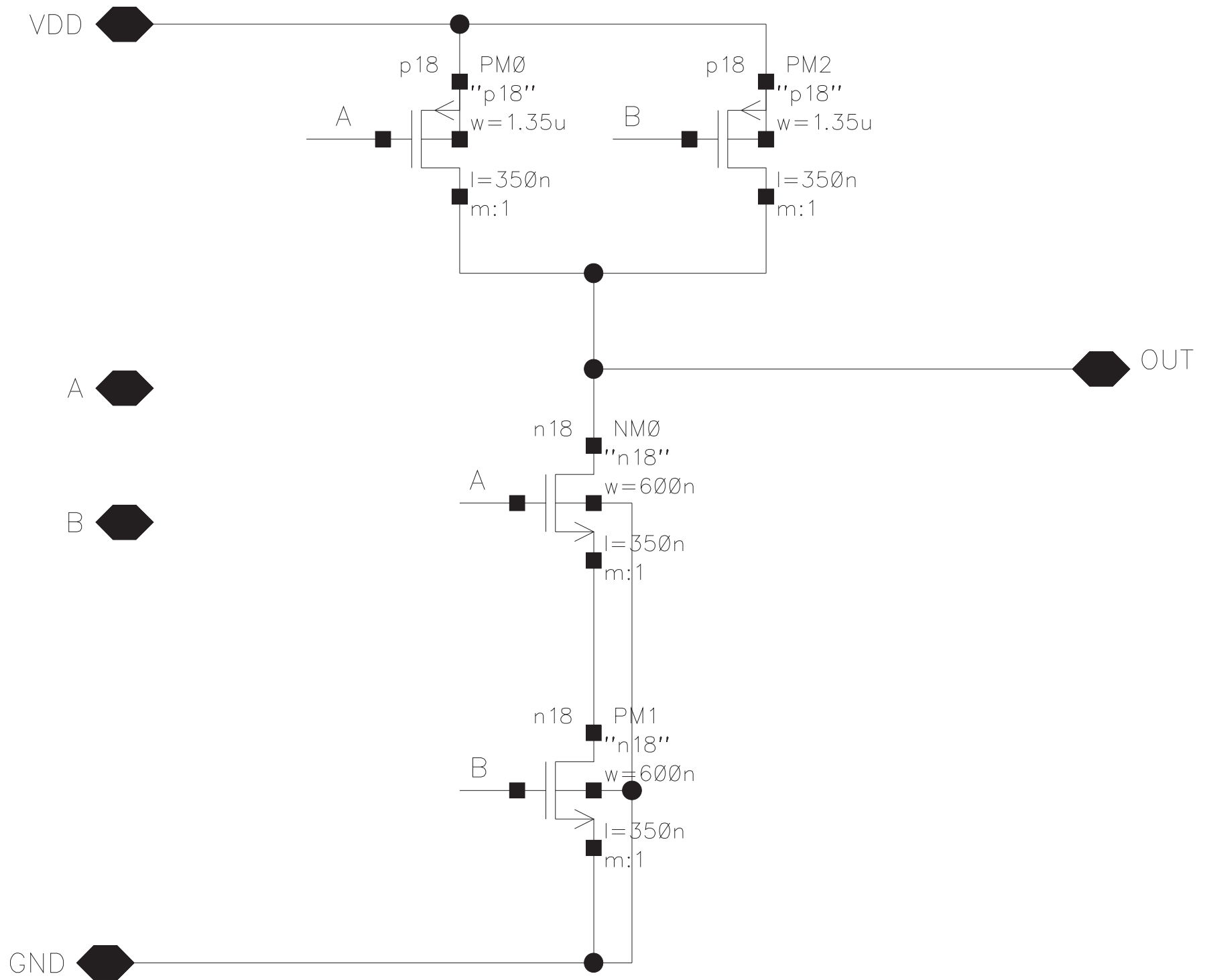










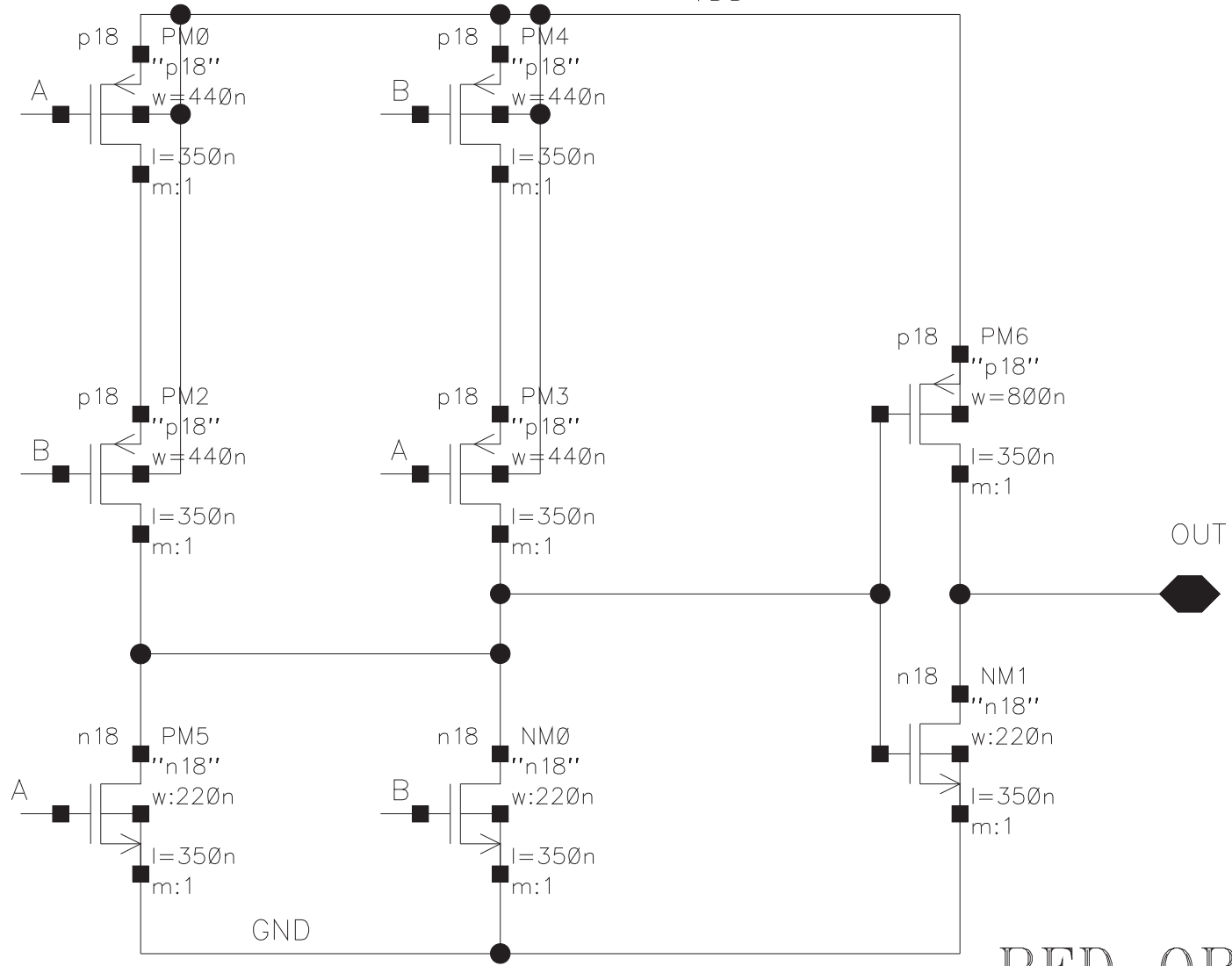


VDD

A

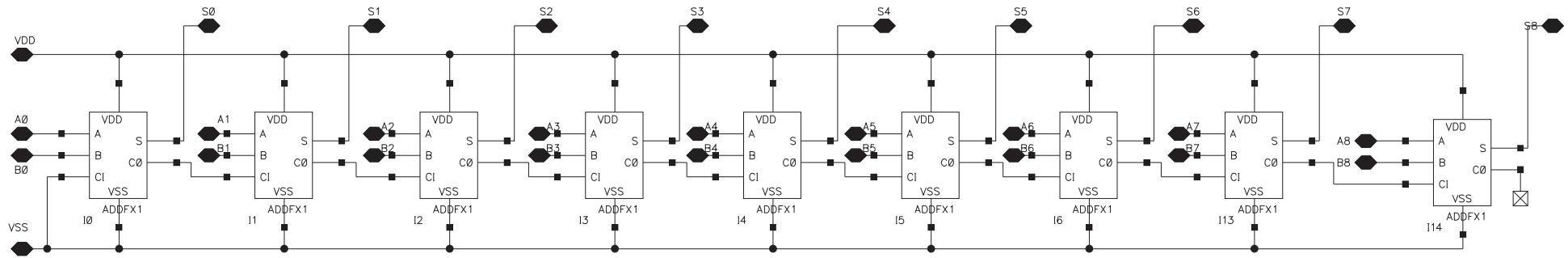
B

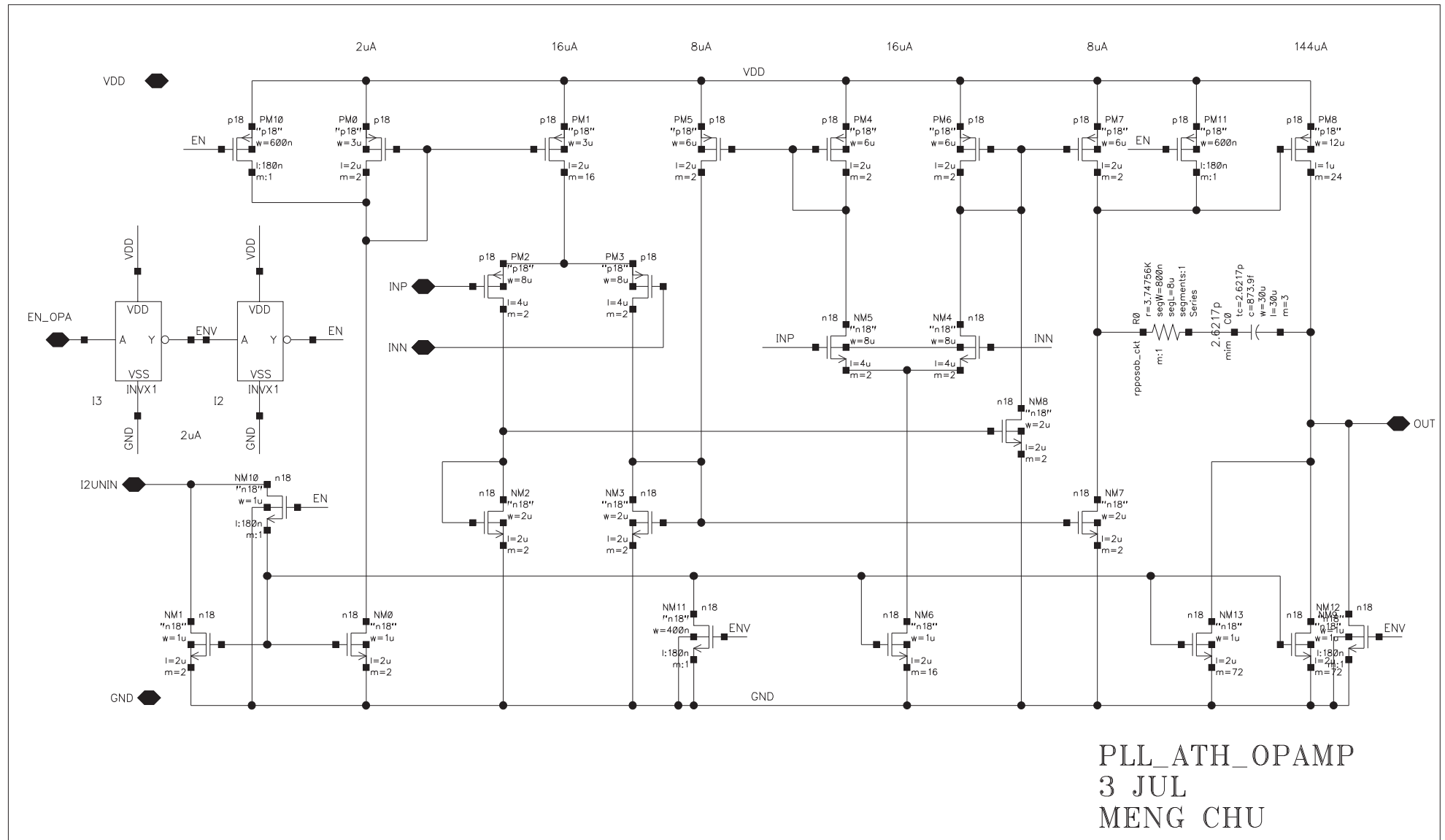
VDD

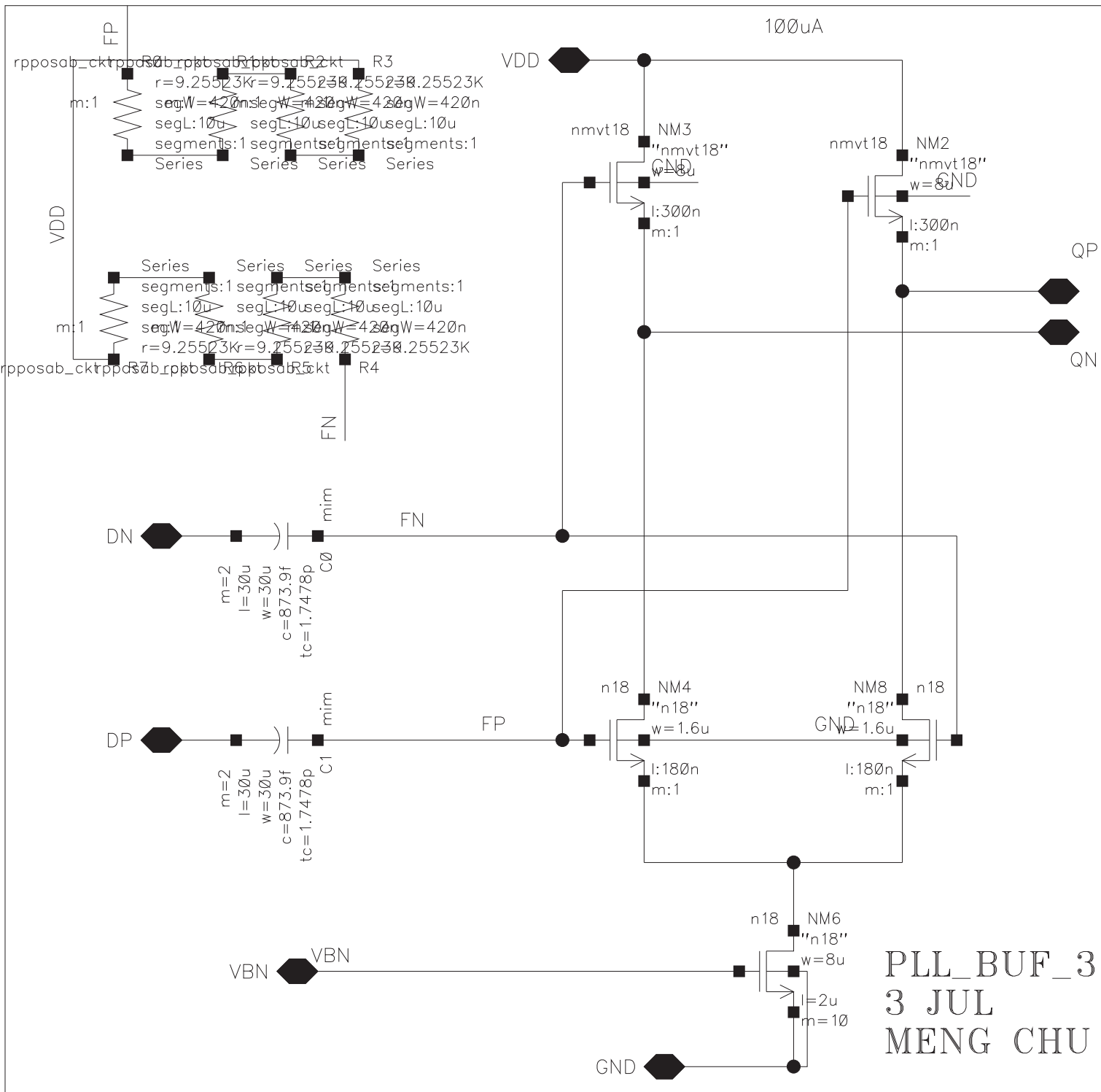


GND

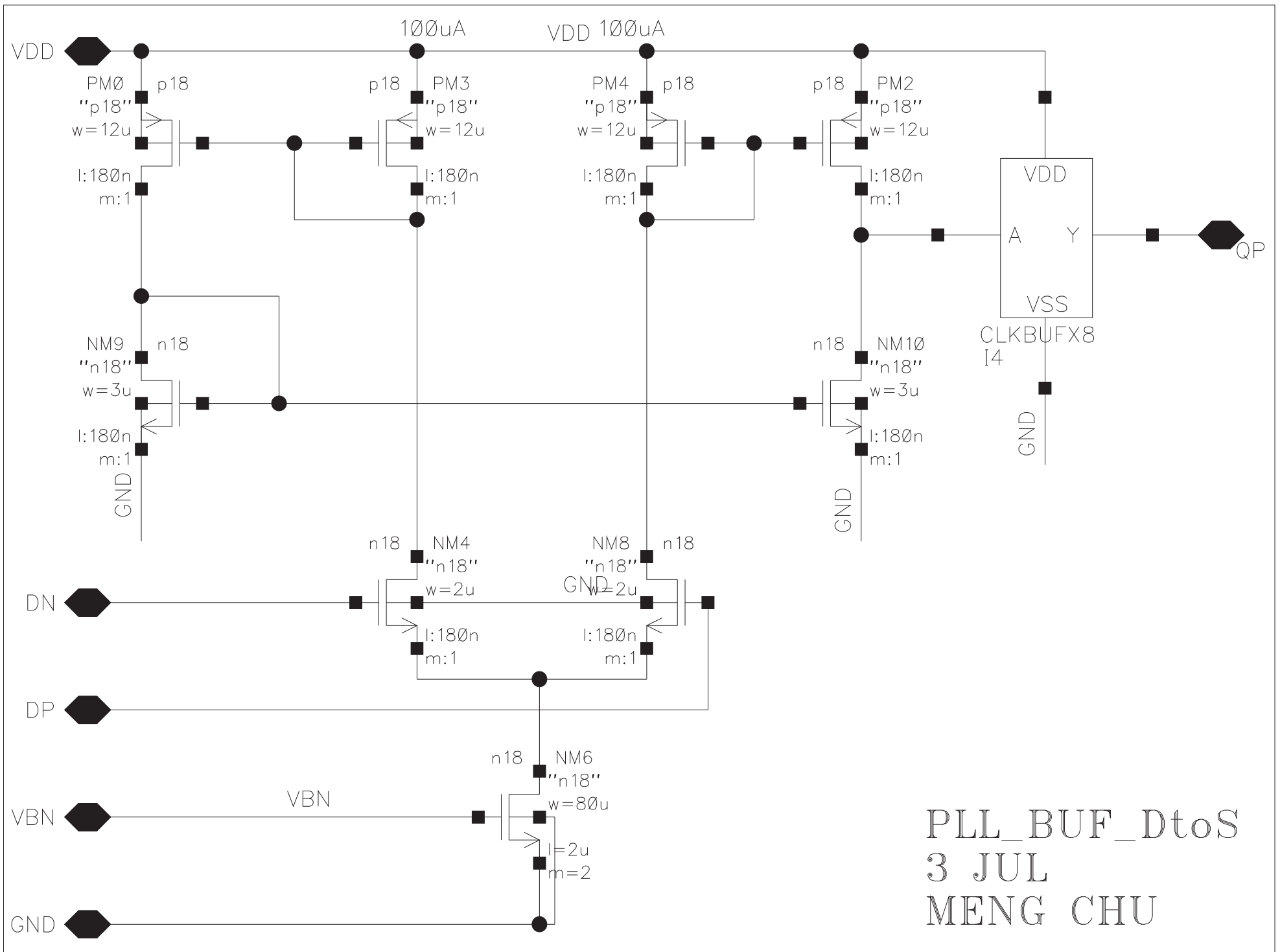
PFD\_OR\_2IN  
 3 JUL  
 MENG CHU





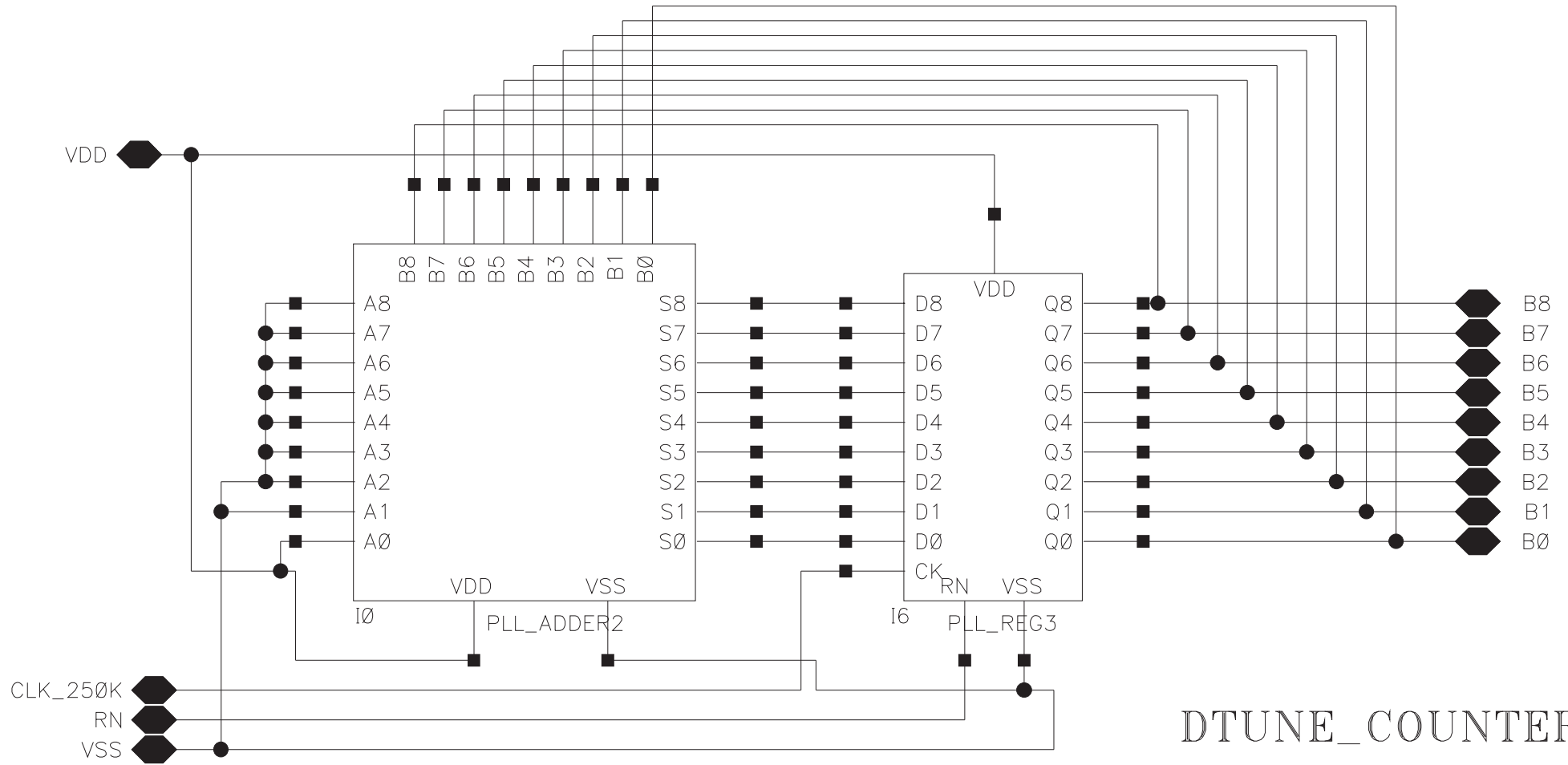






PLL\_BUF\_DtoS  
 3 JUL  
 MENG CHU

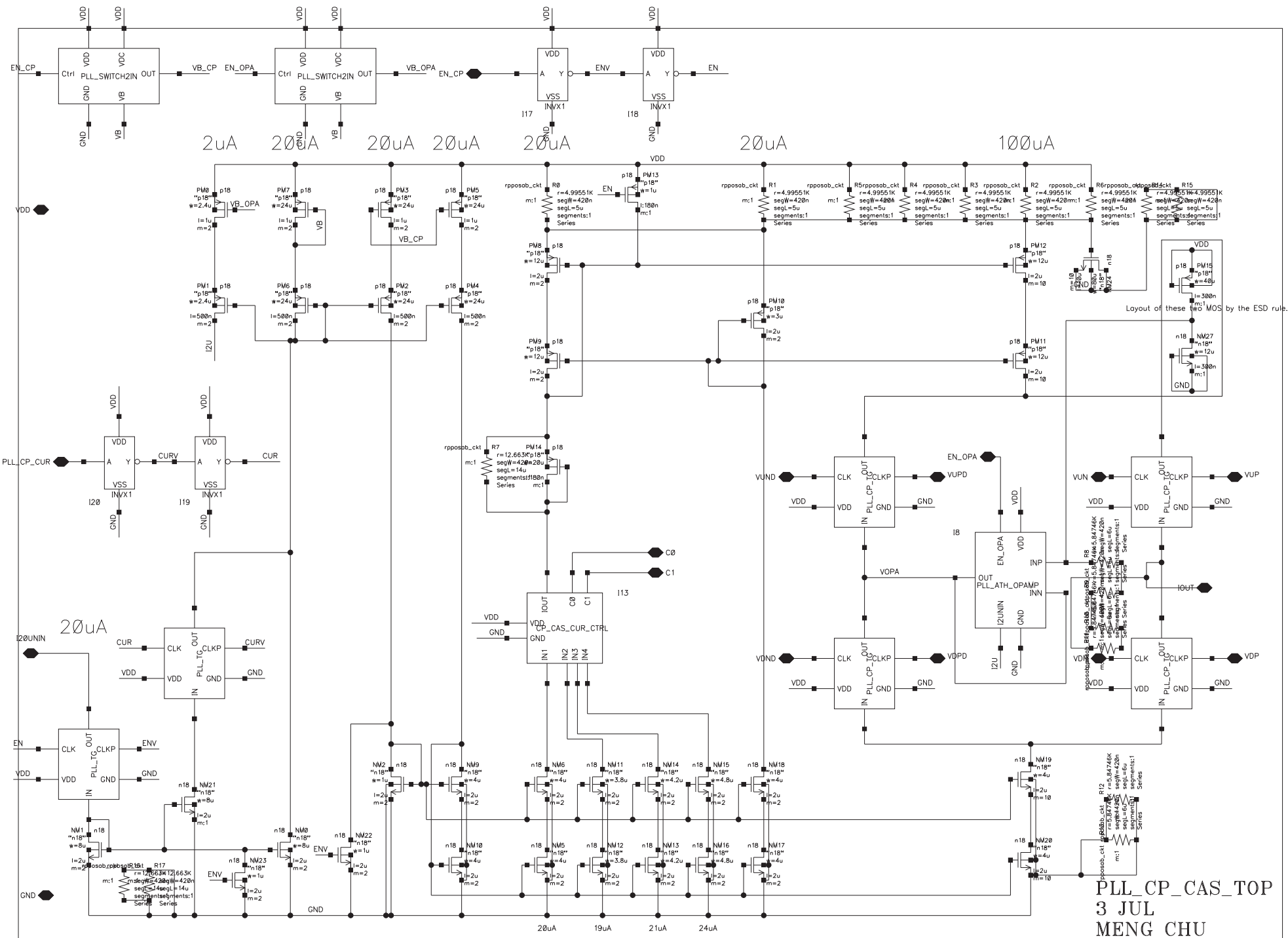




DTUNE\_COUNTER

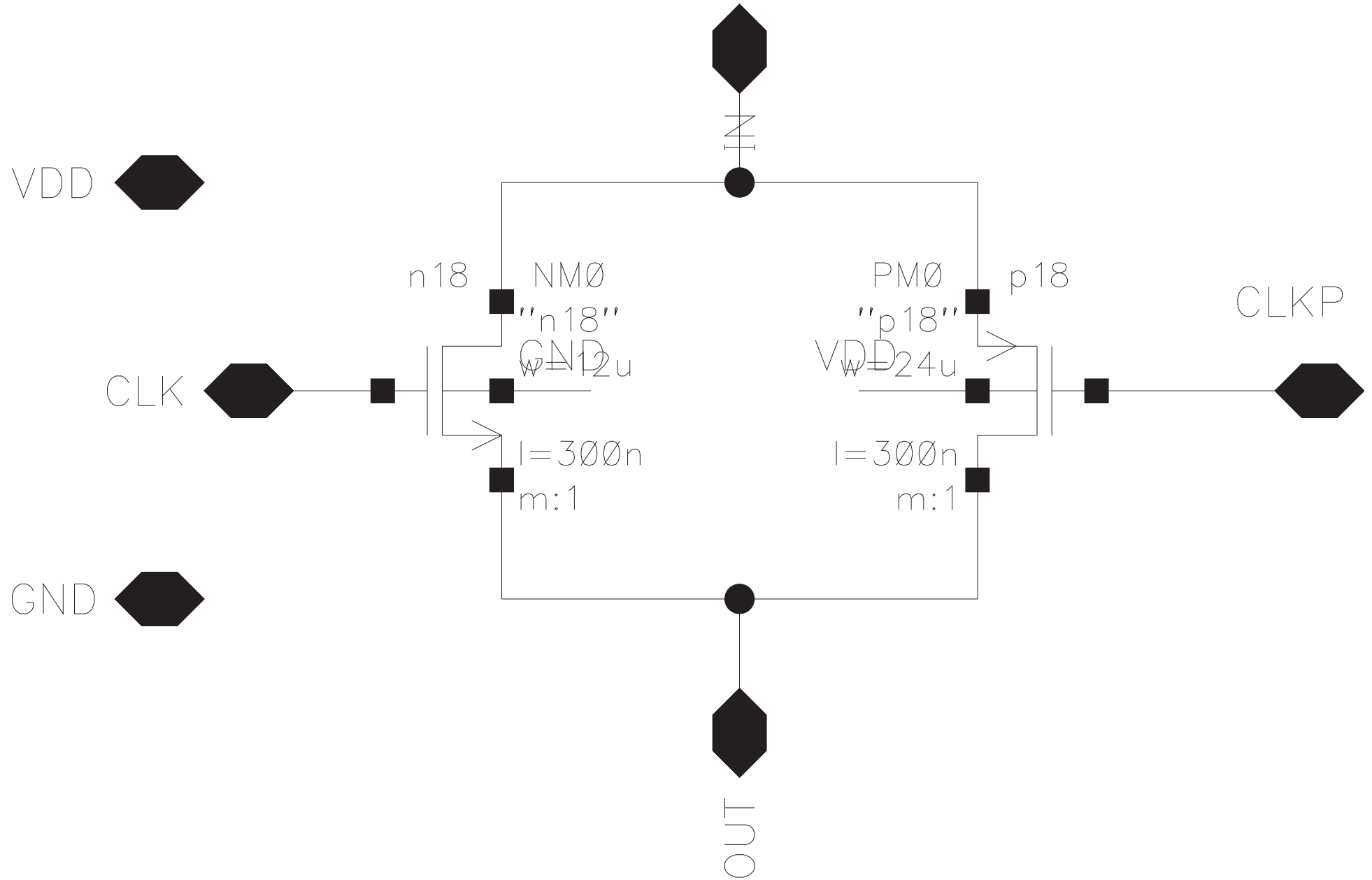
30 June 2007

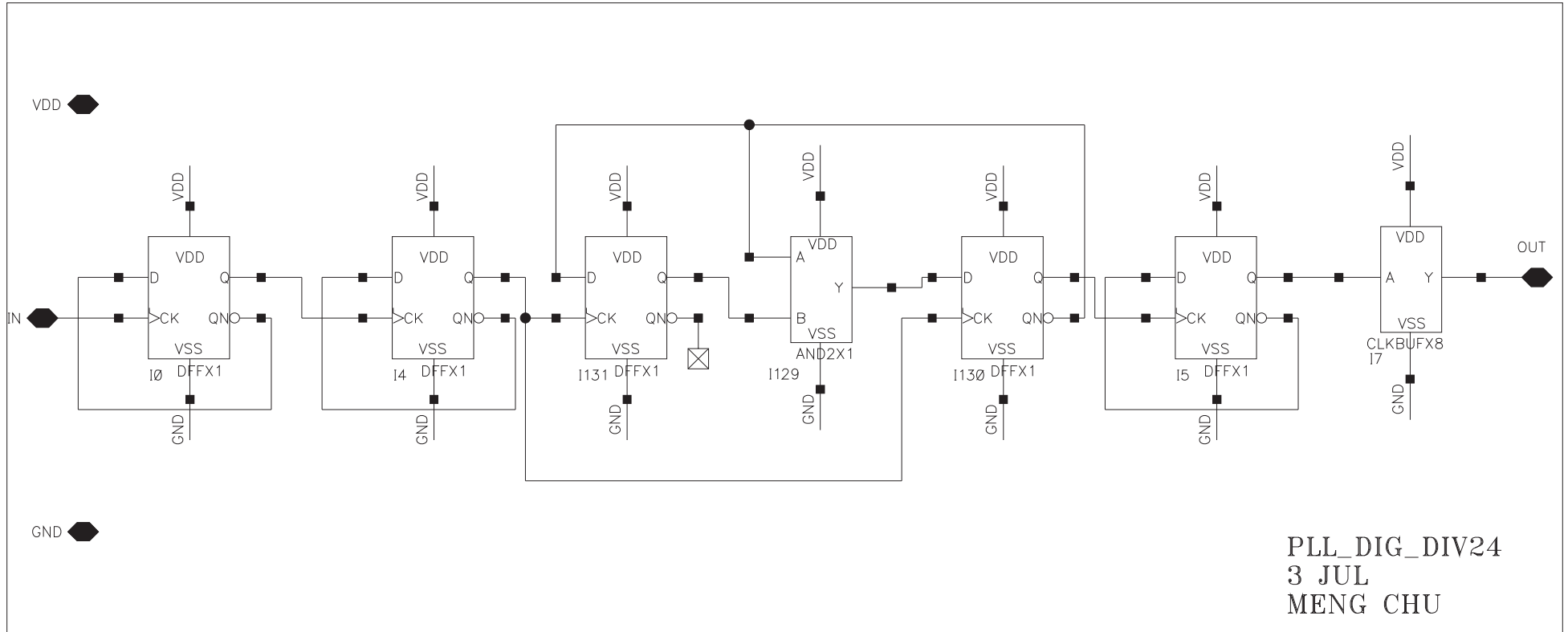
MENG CHU

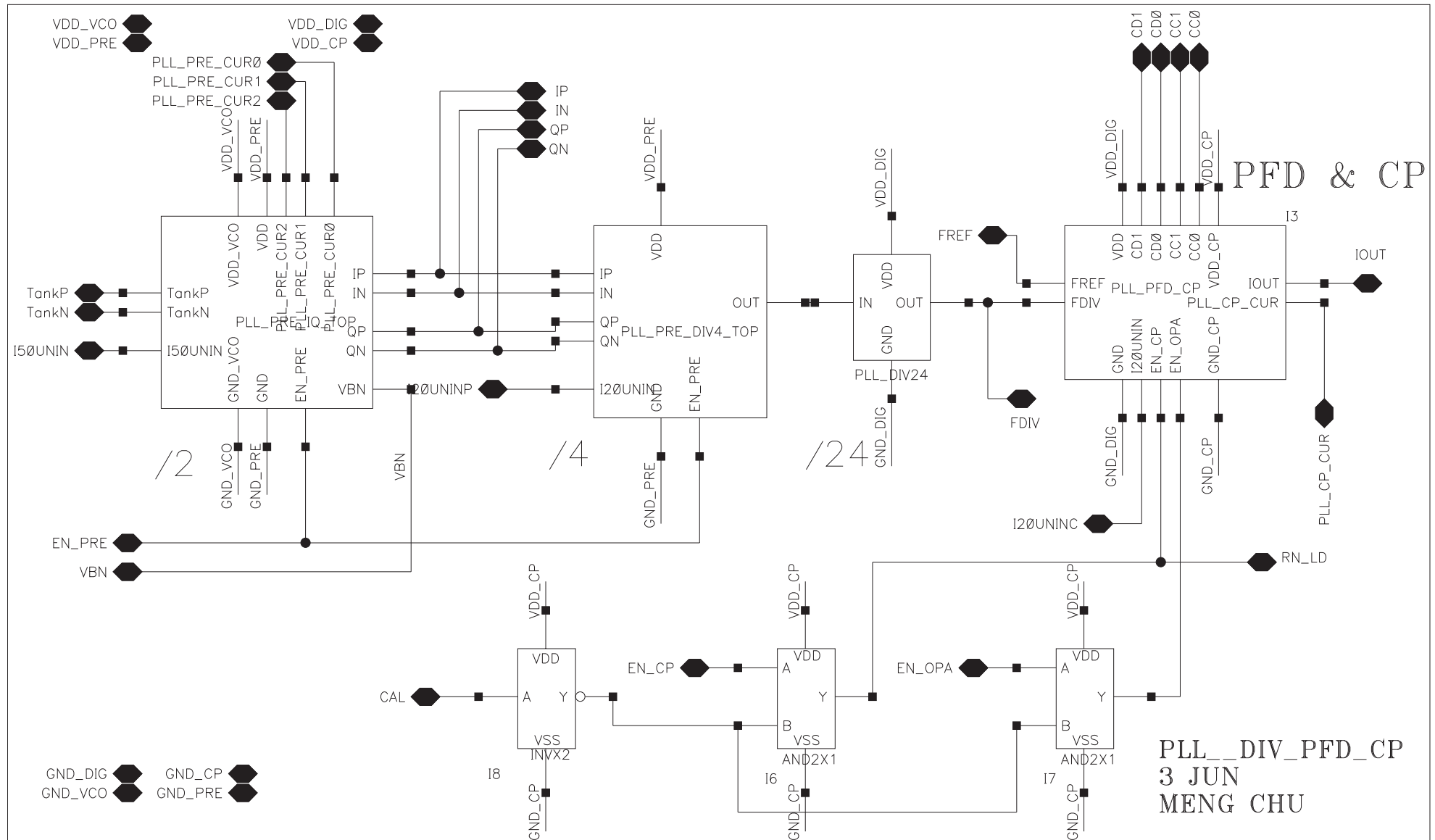


PLL\_CP\_CAS\_TOP  
 3 JUL  
 MENG CHU

Layout of these two MOS by the ESD rule.

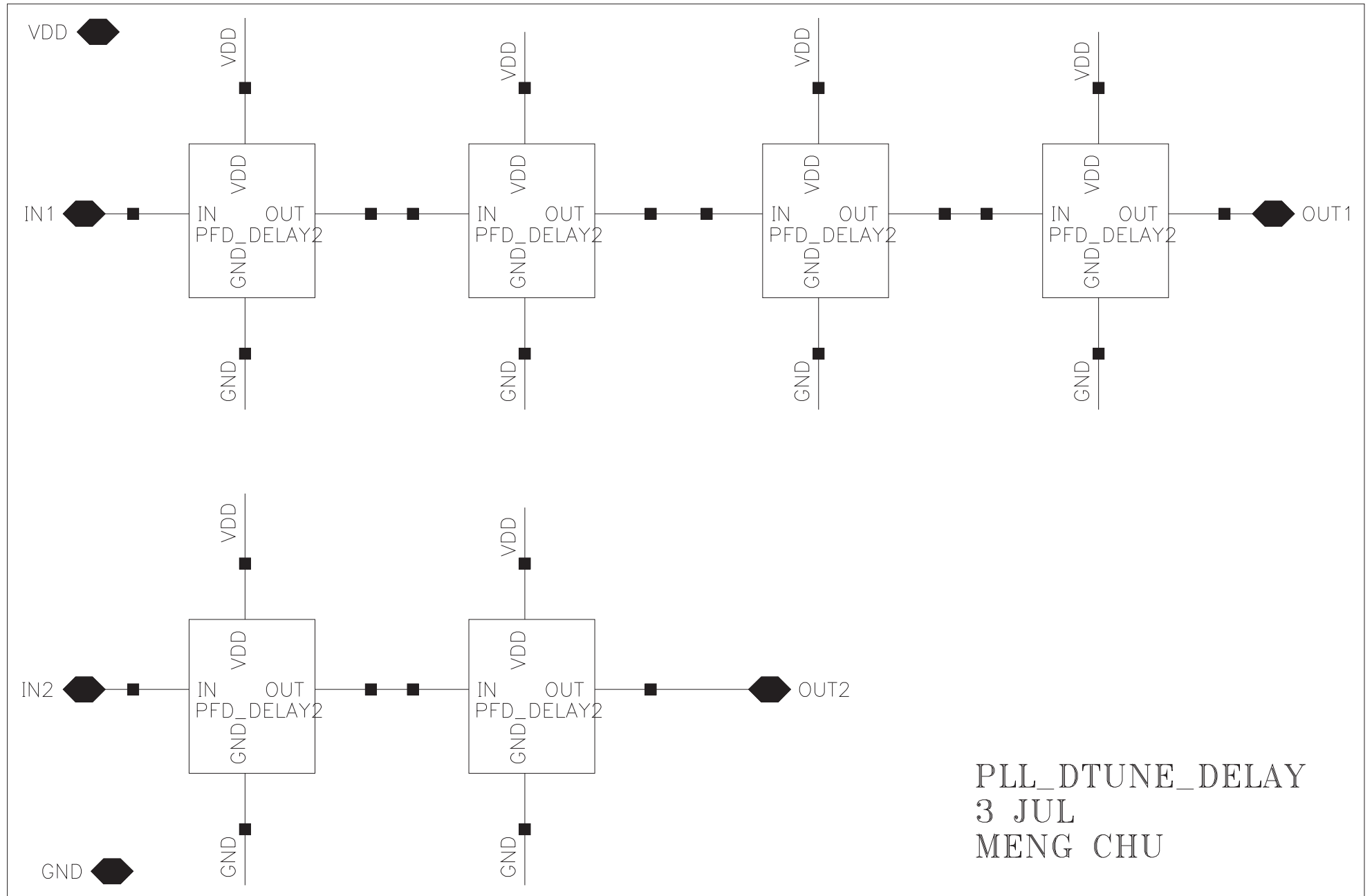


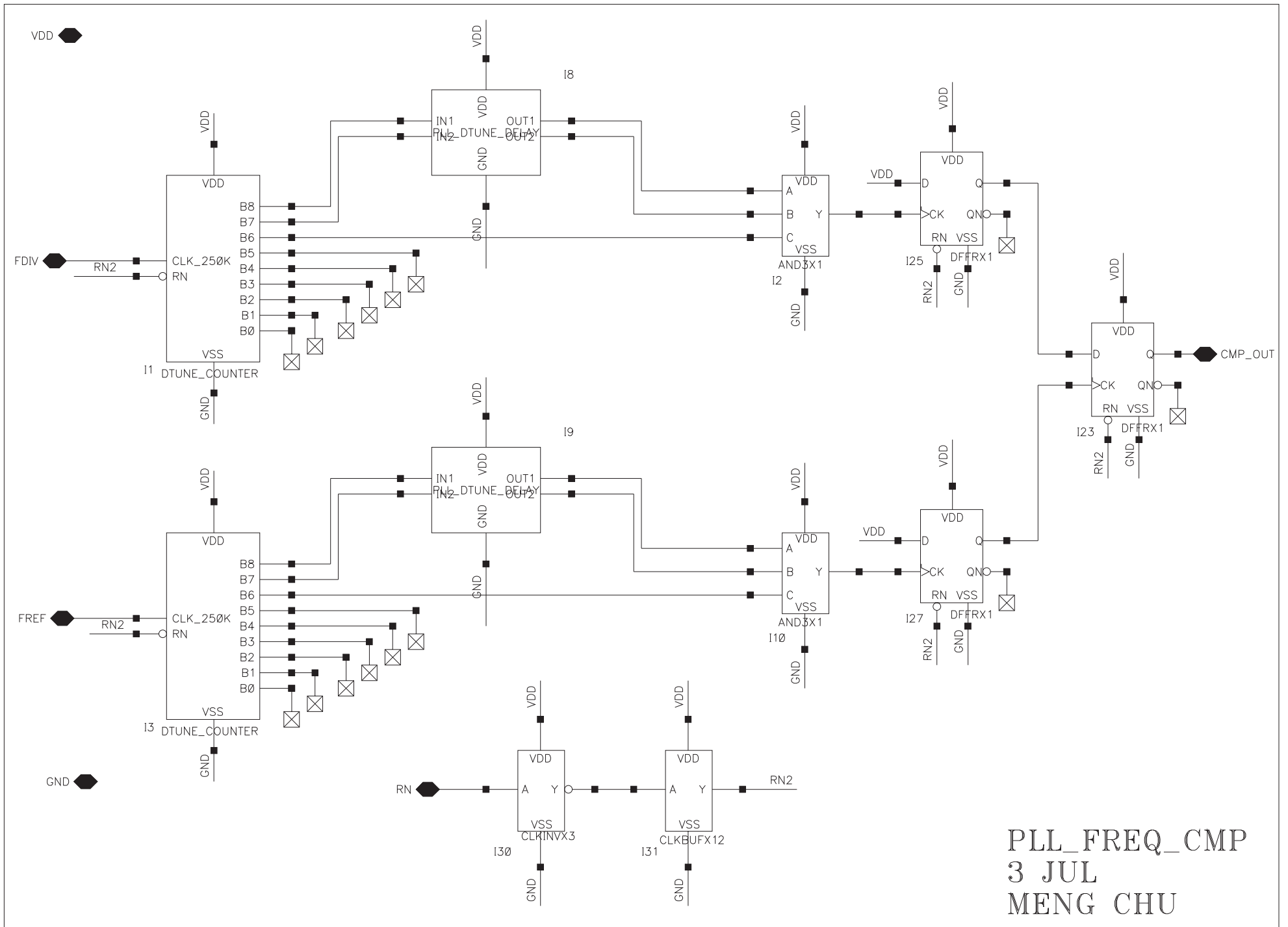




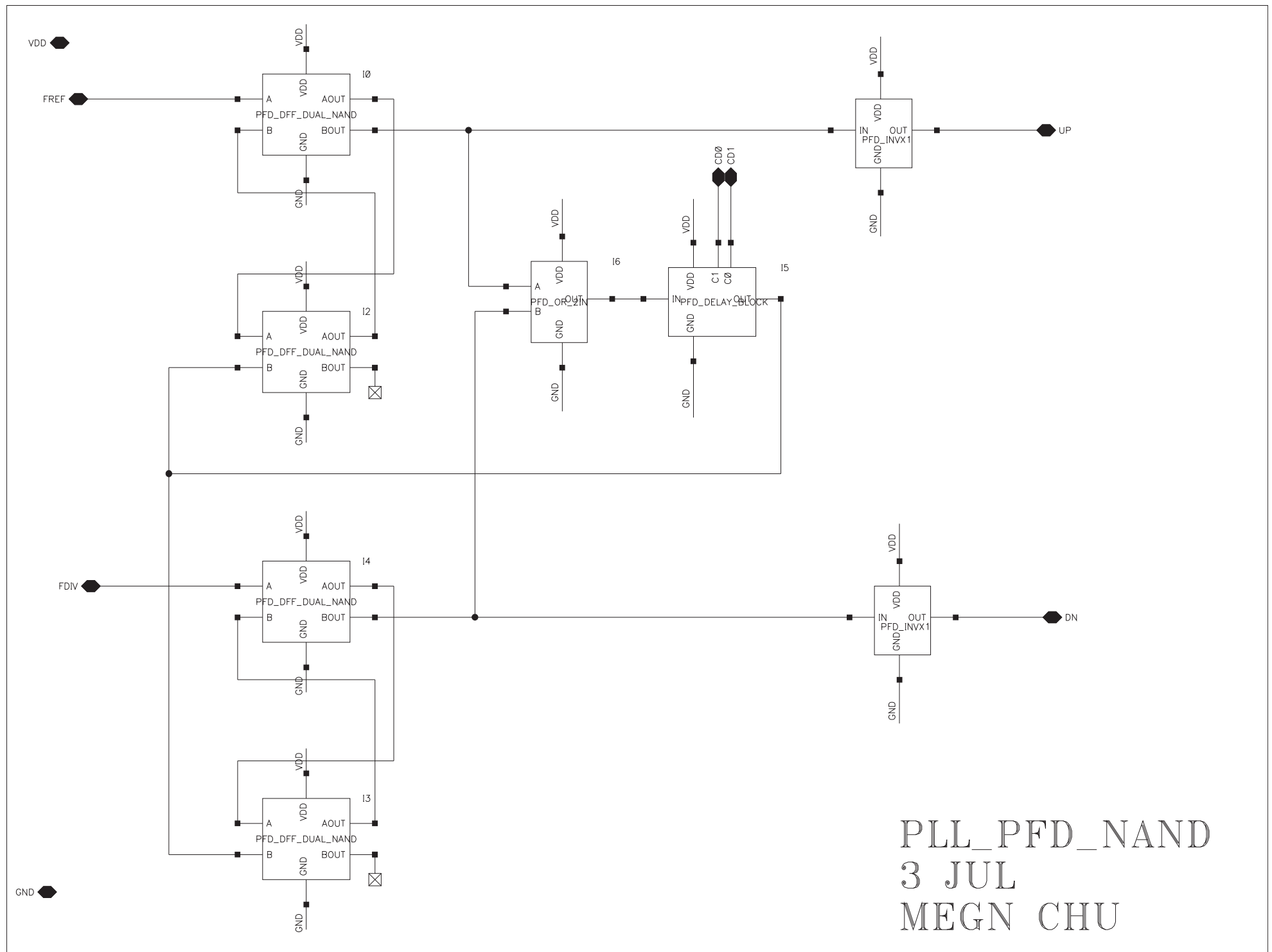




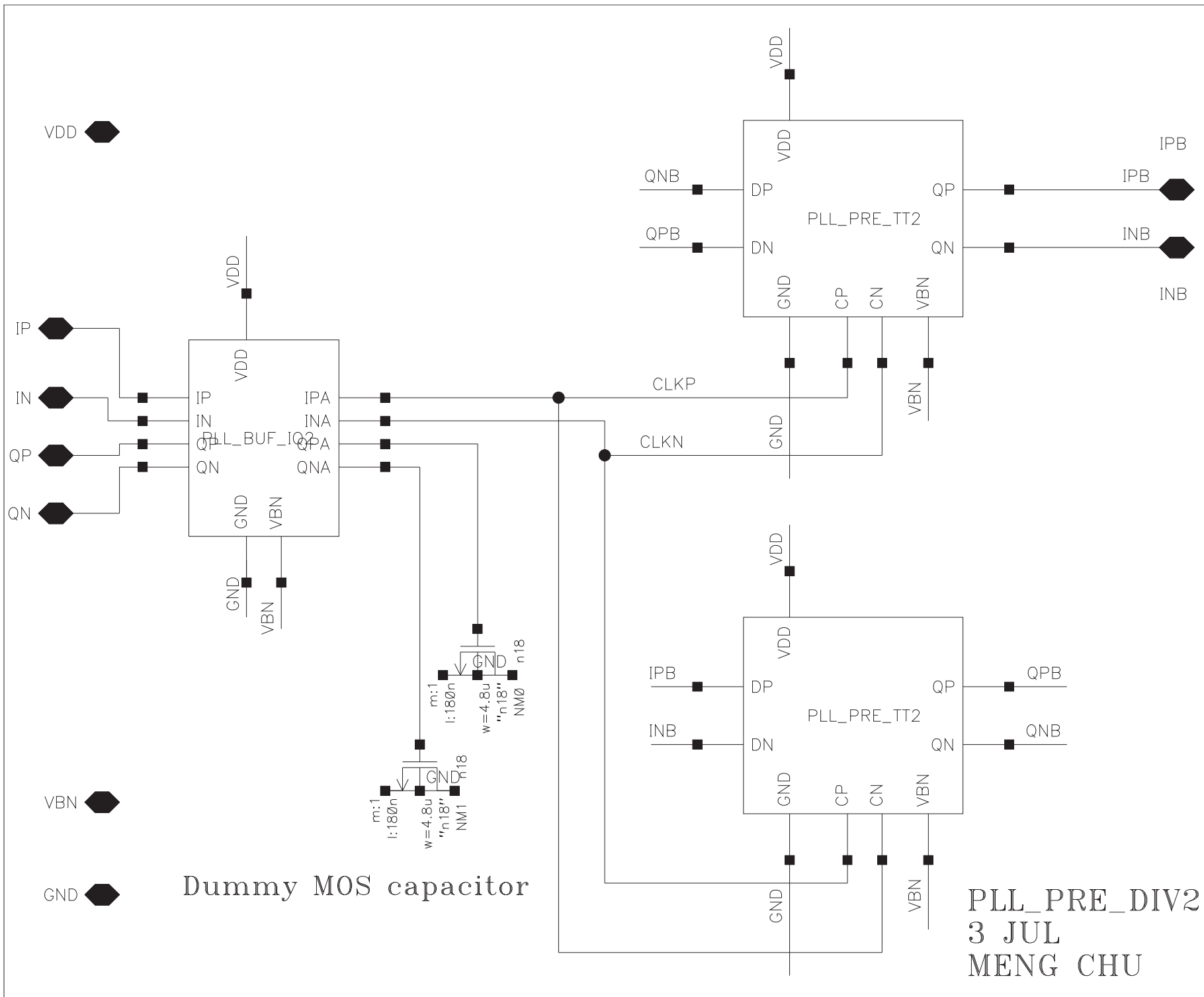






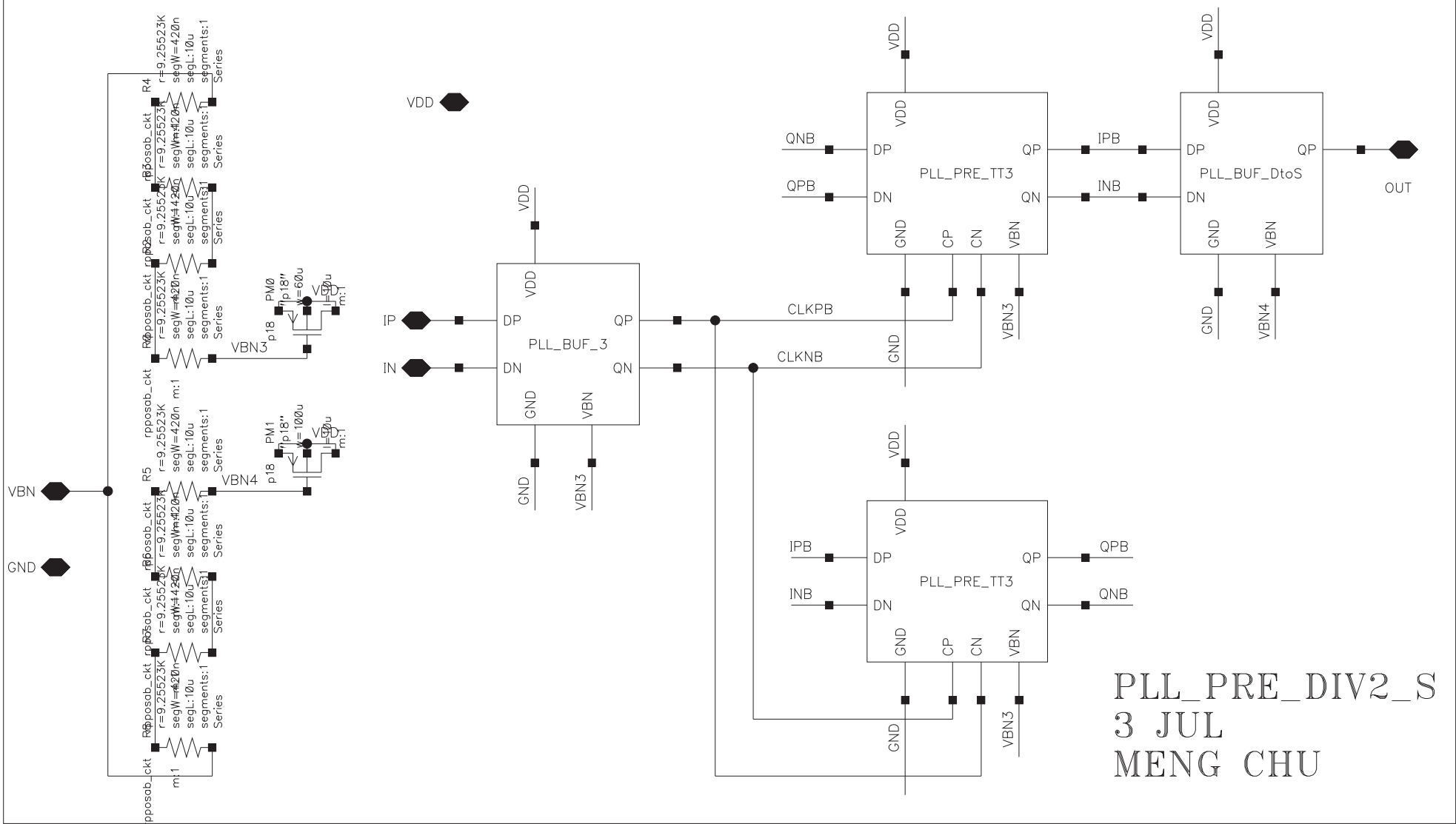


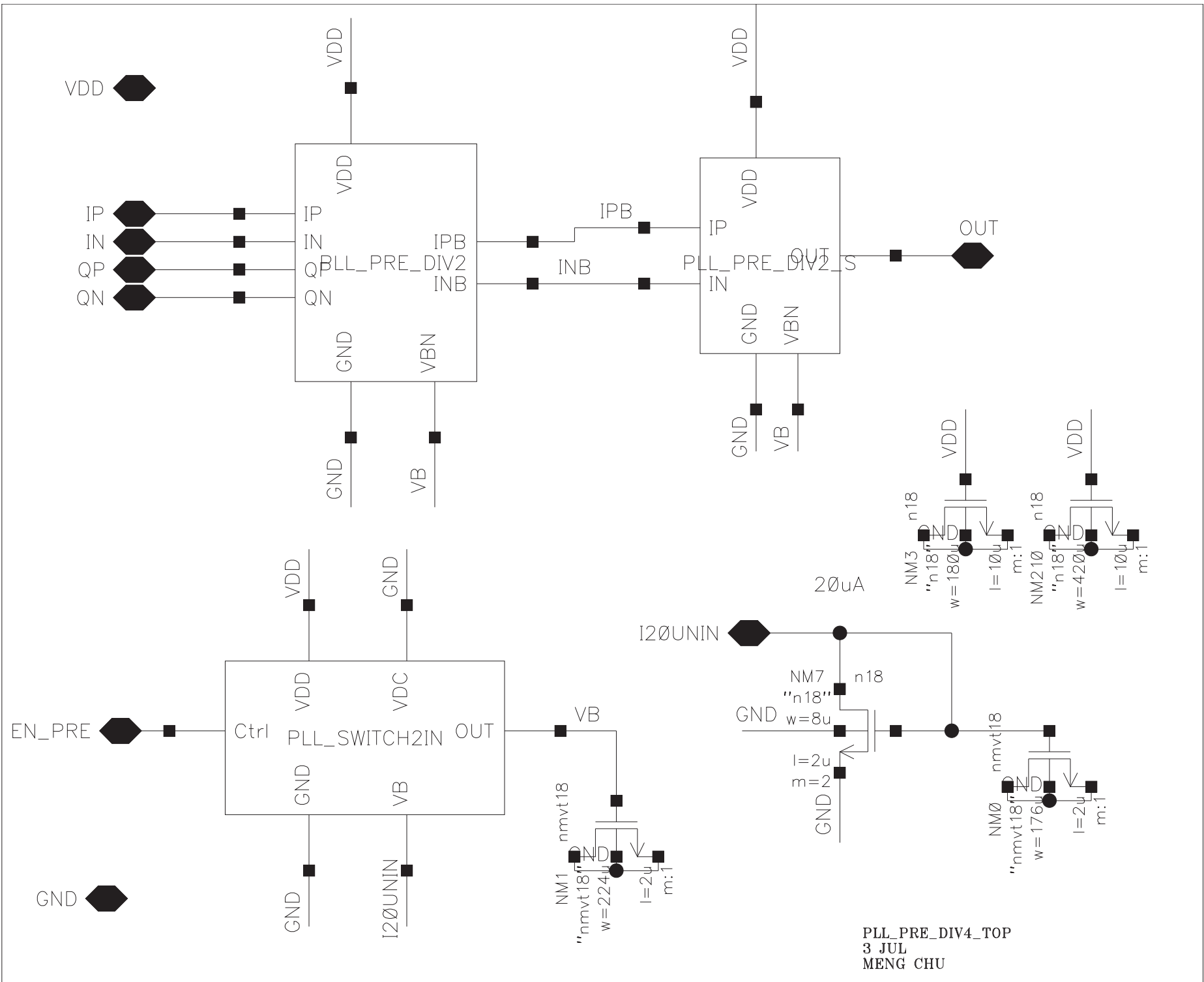
PLL\_PFD\_NAND  
 3 JUL  
 MEGN CHU



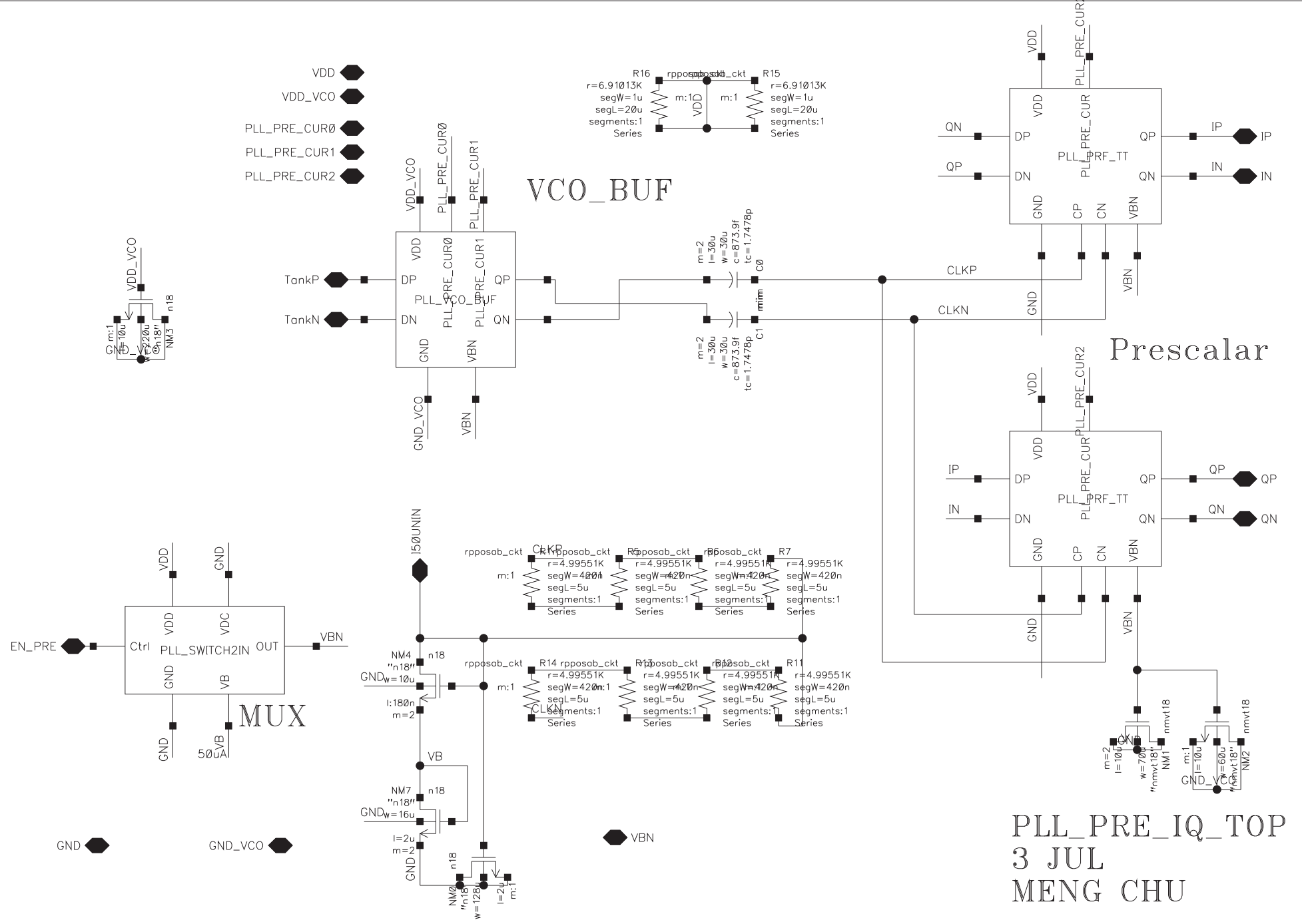
Dummy MOS capacitor

PLL\_PRE\_DIV2  
 3 JUL  
 MENG CHU



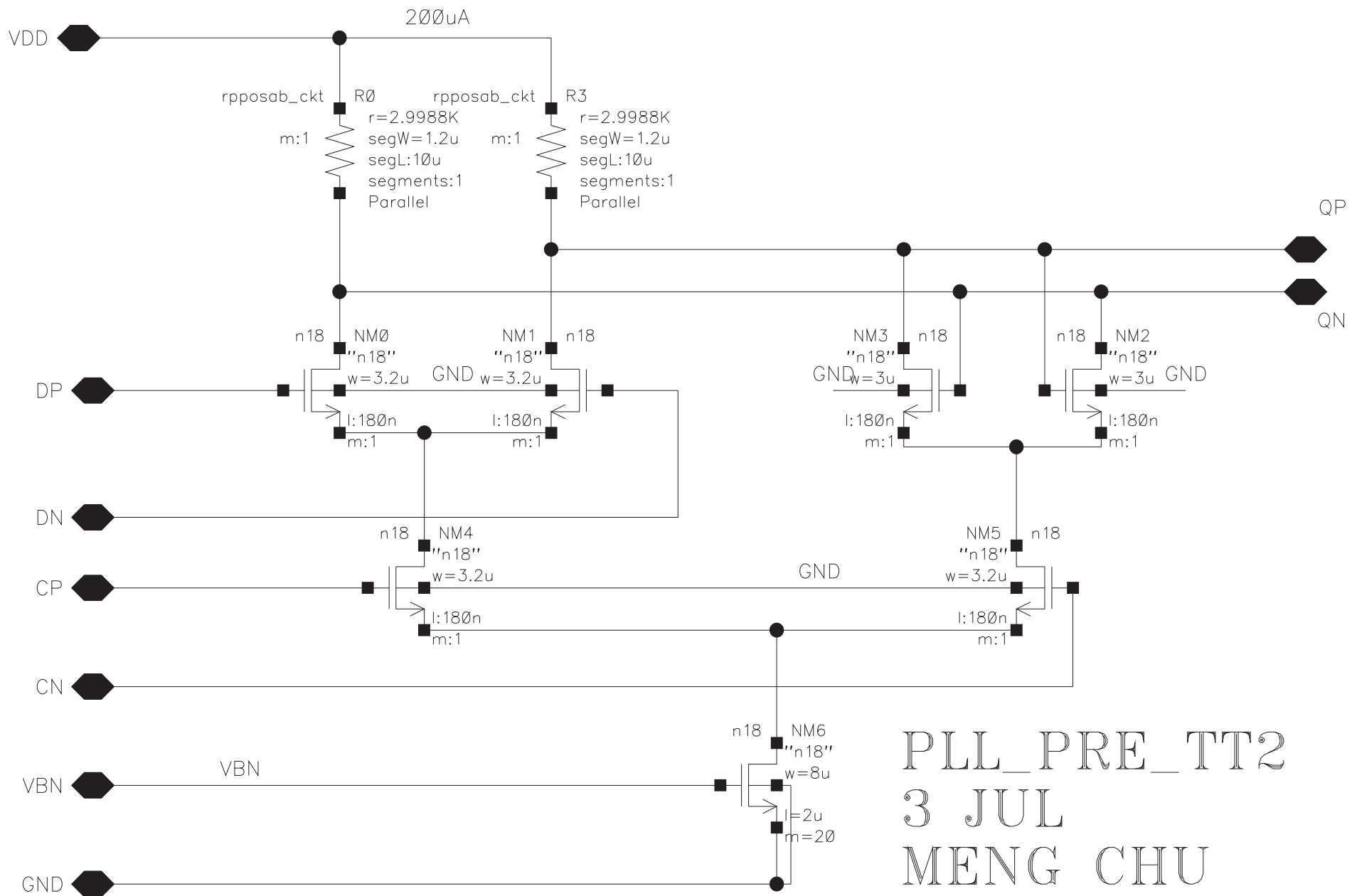


PLL\_PRE\_DIV4\_TOP  
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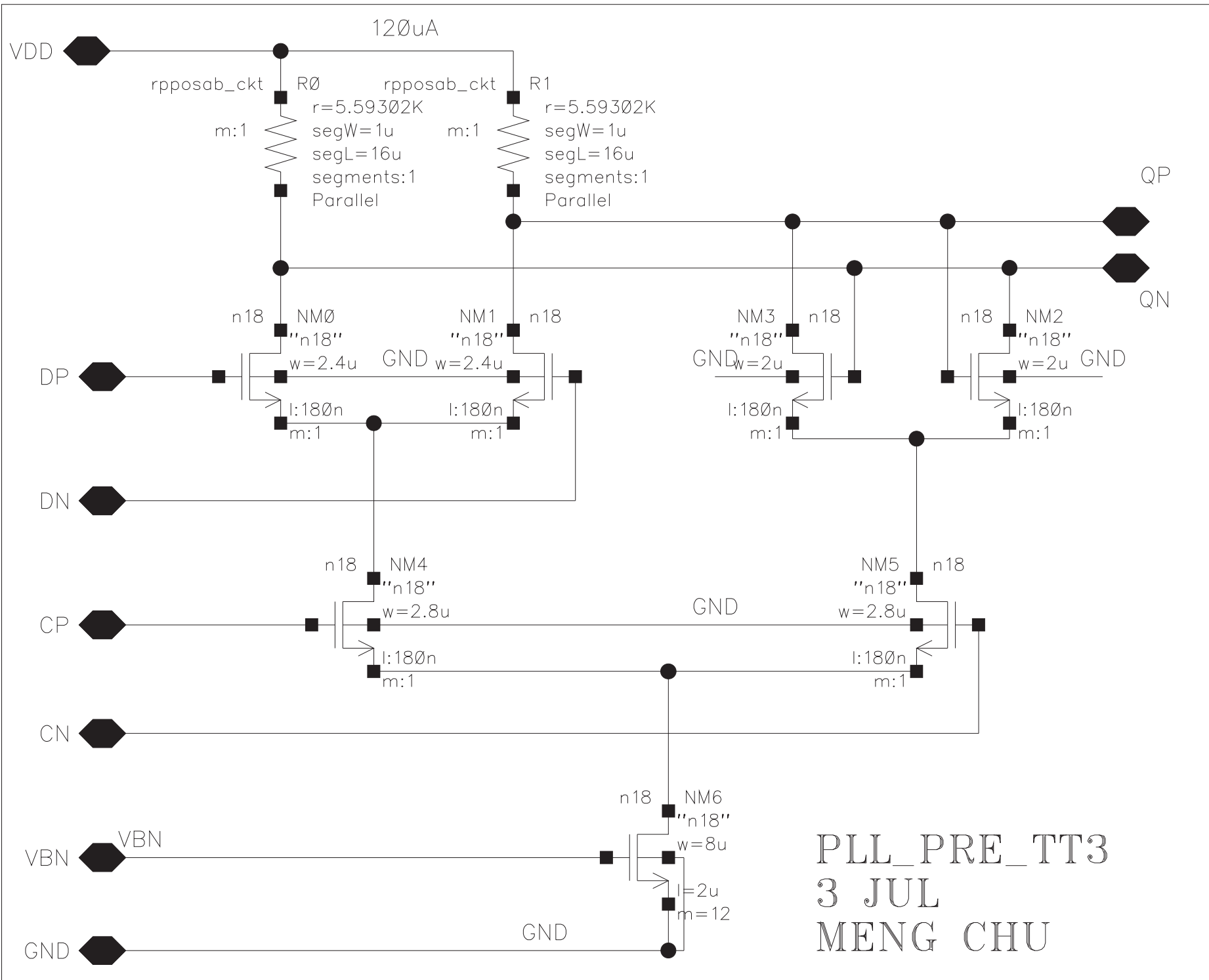


PLL\_PRE\_IQ\_TOP  
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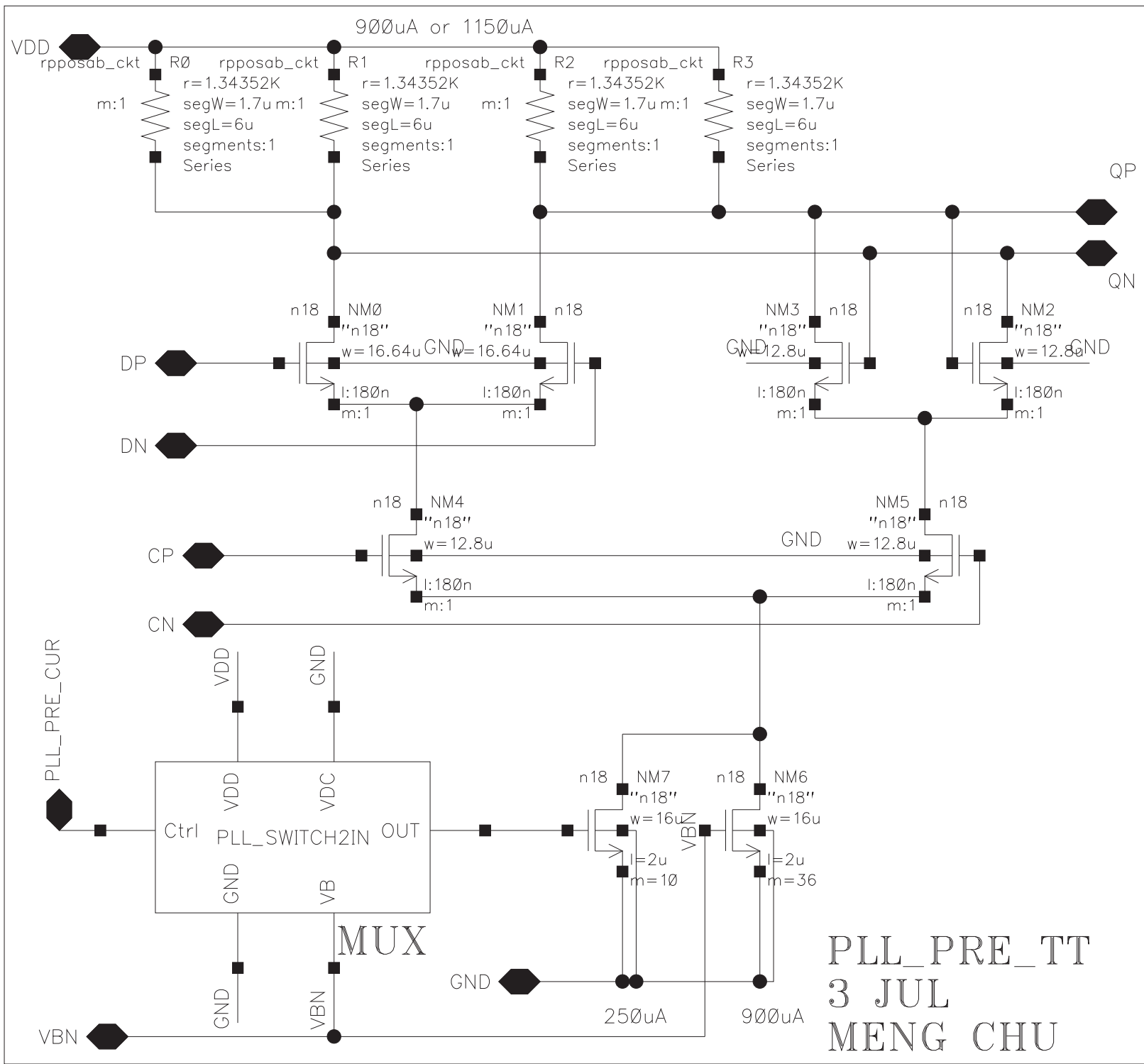




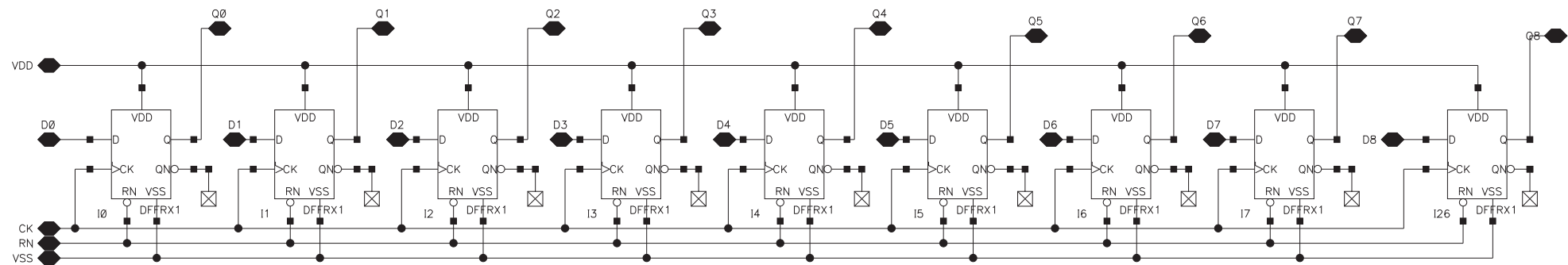
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 MENG CHU



PLL\_PRE\_TT3  
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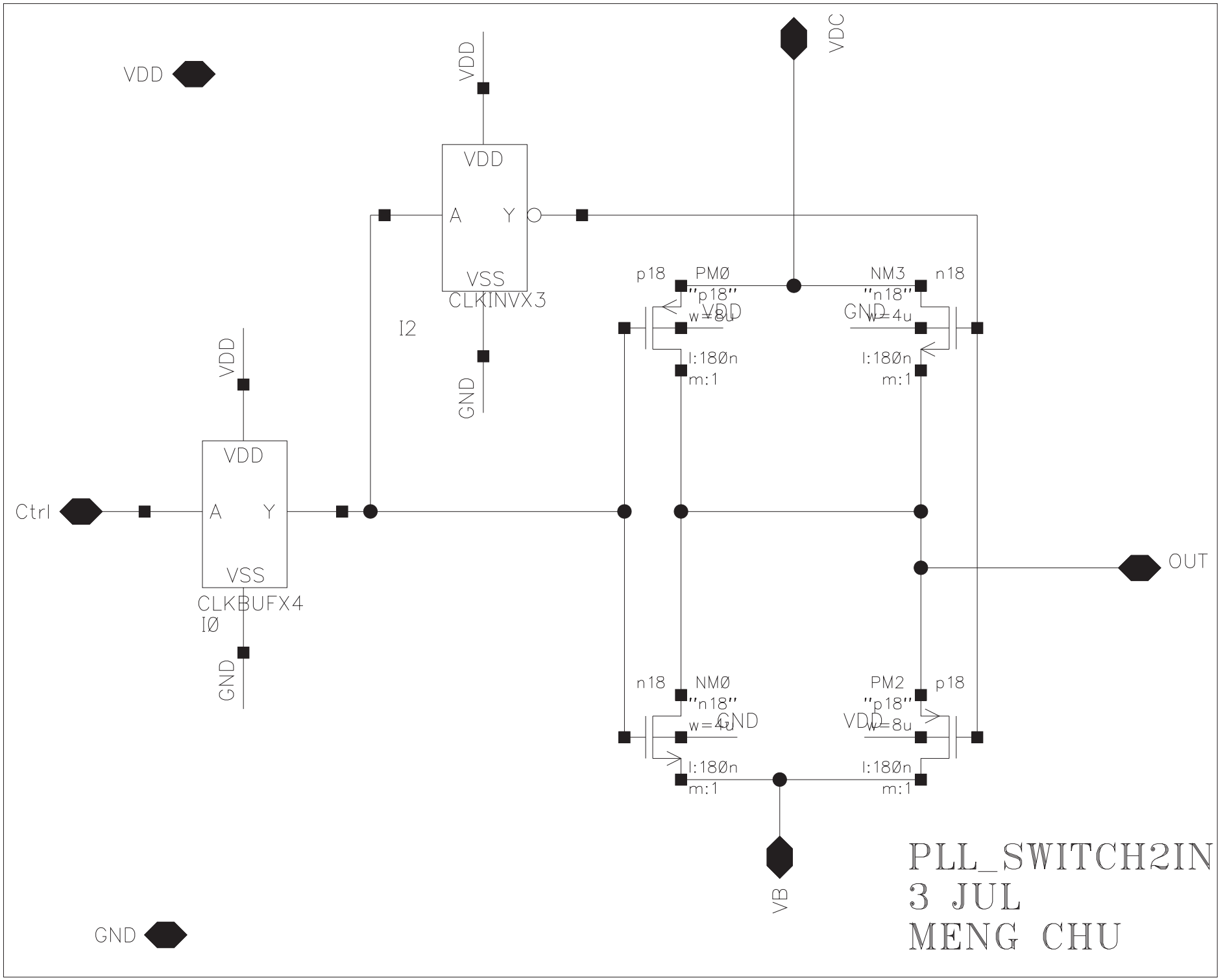
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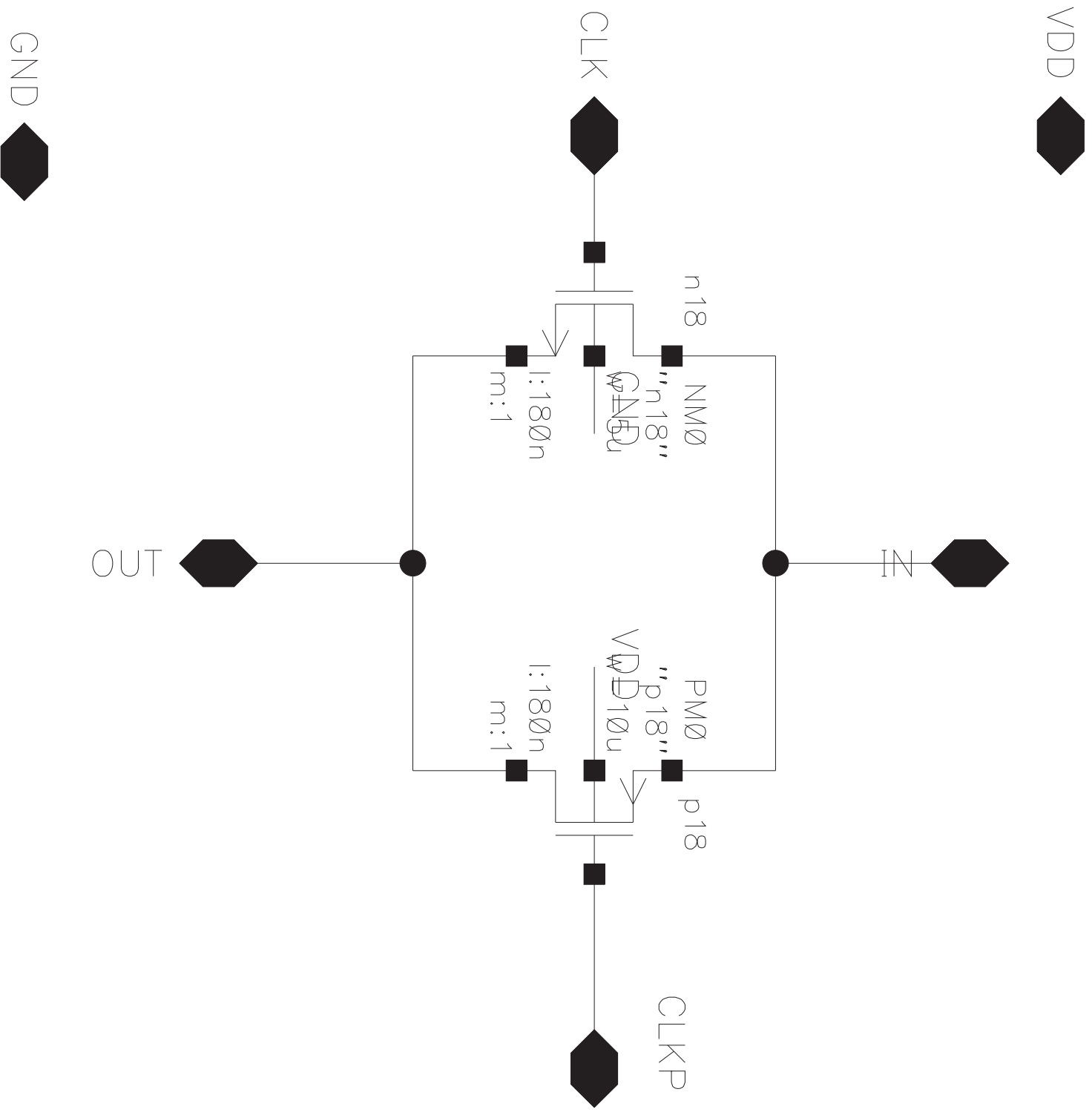
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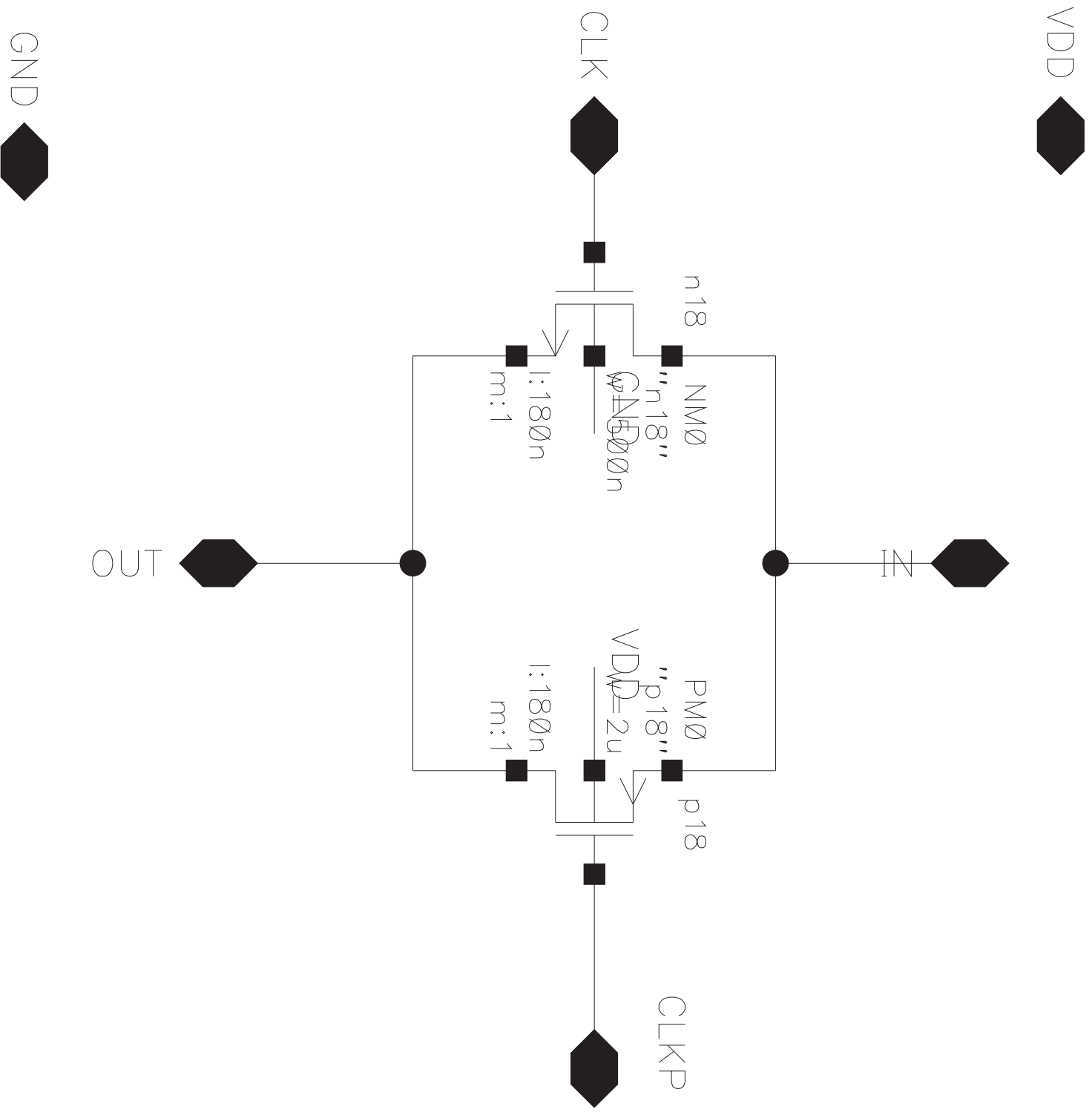
3 June 2007

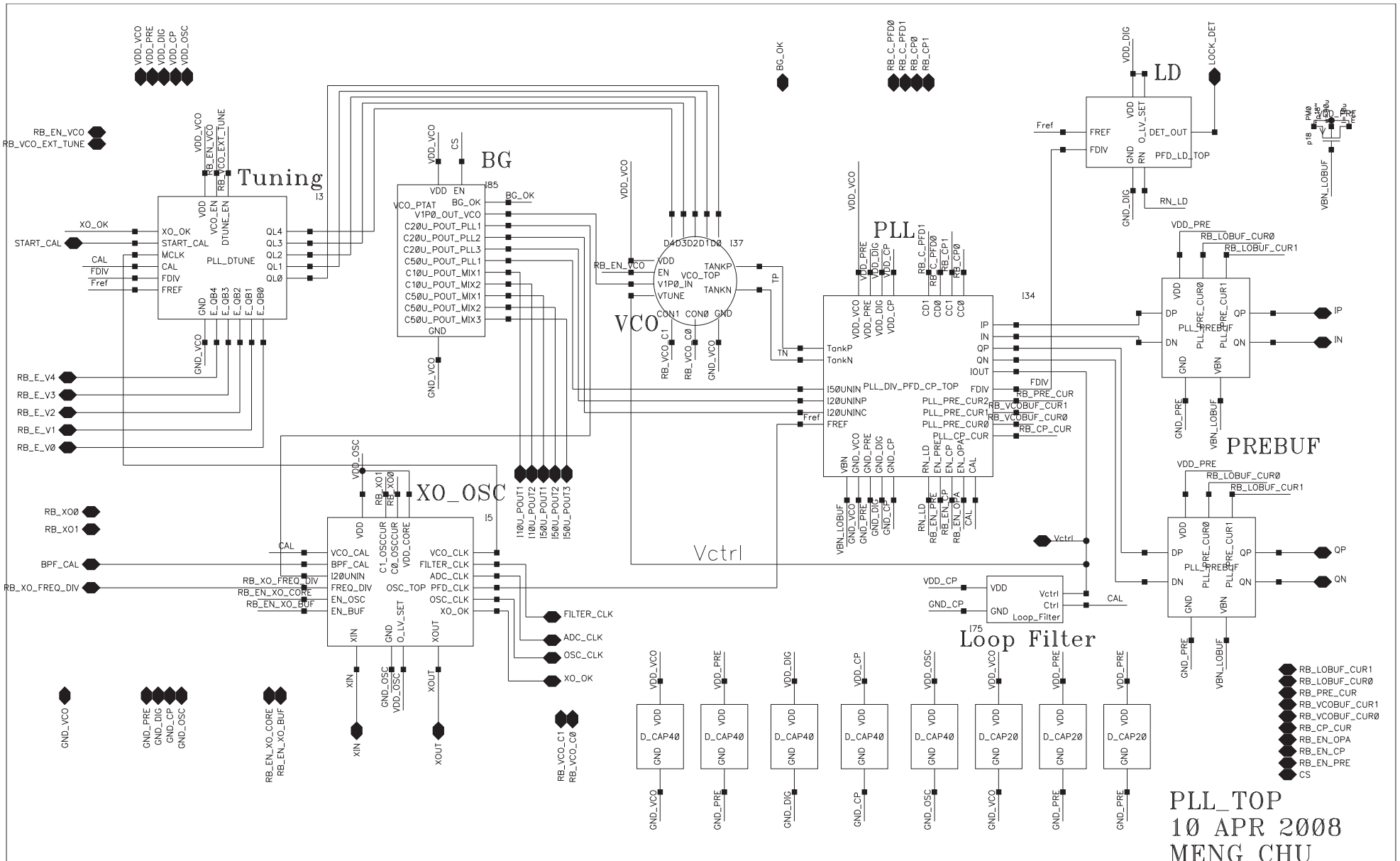
Xiaozhe Chenq



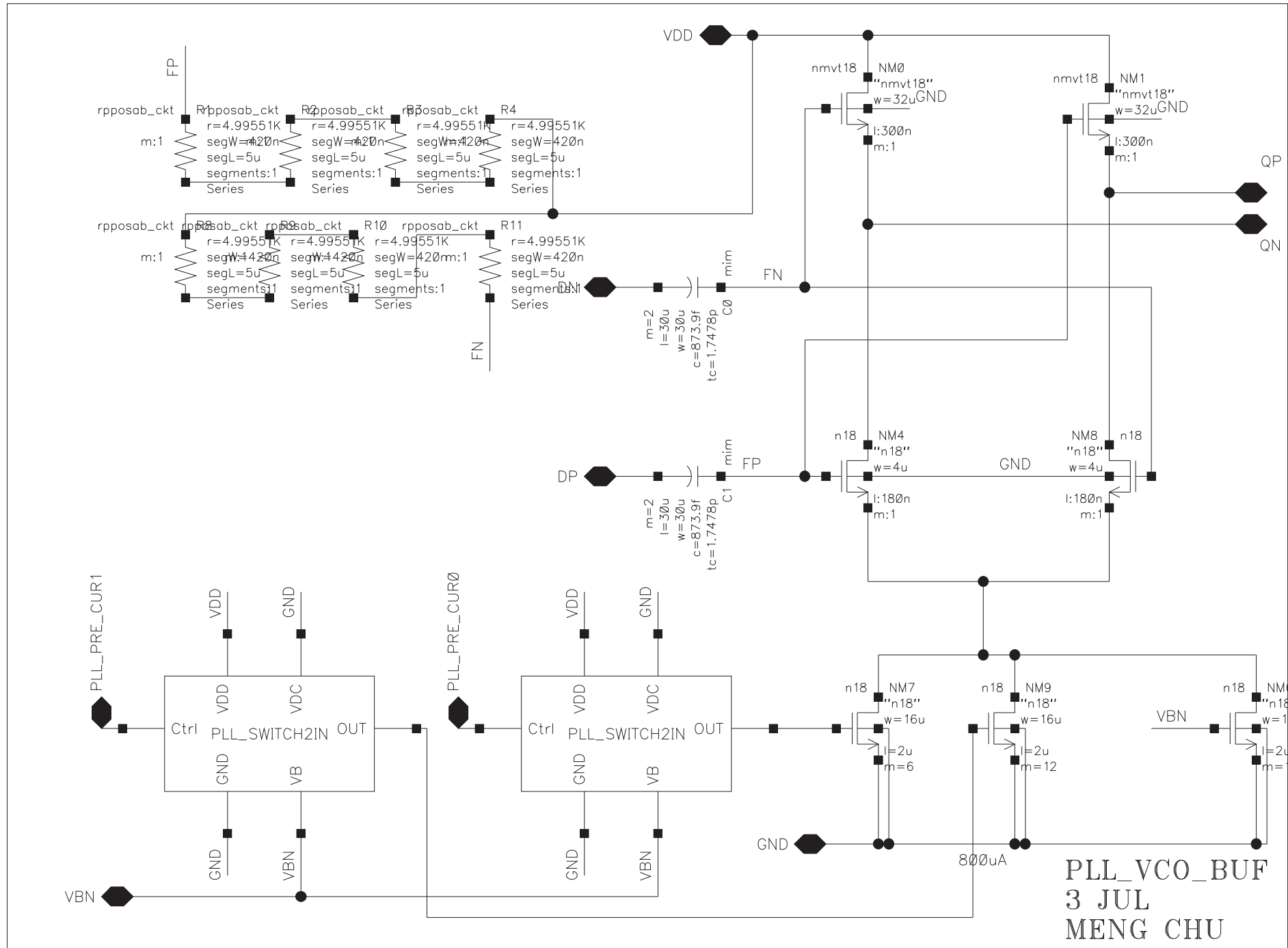
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 3 JUL  
 MENG CHU

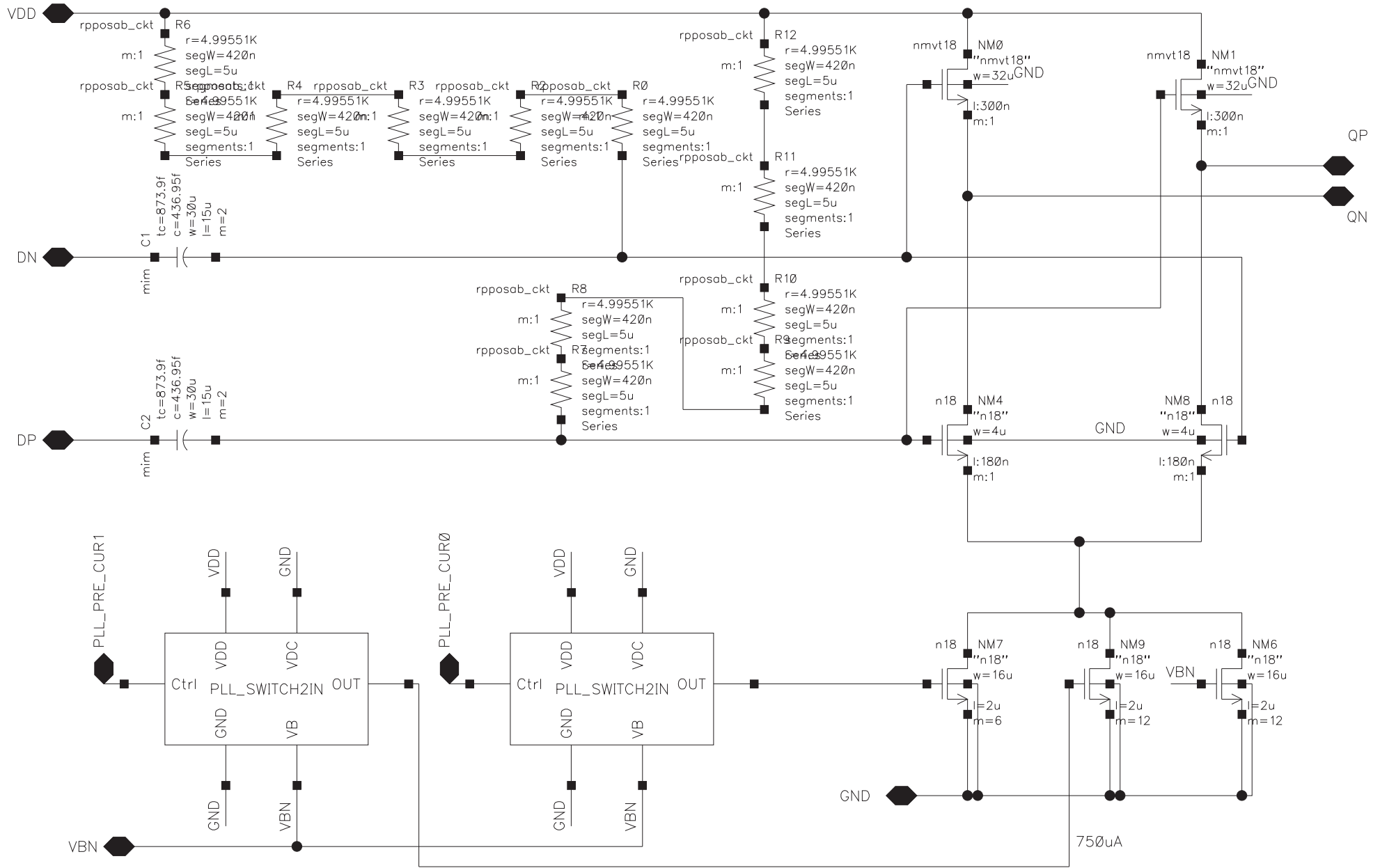


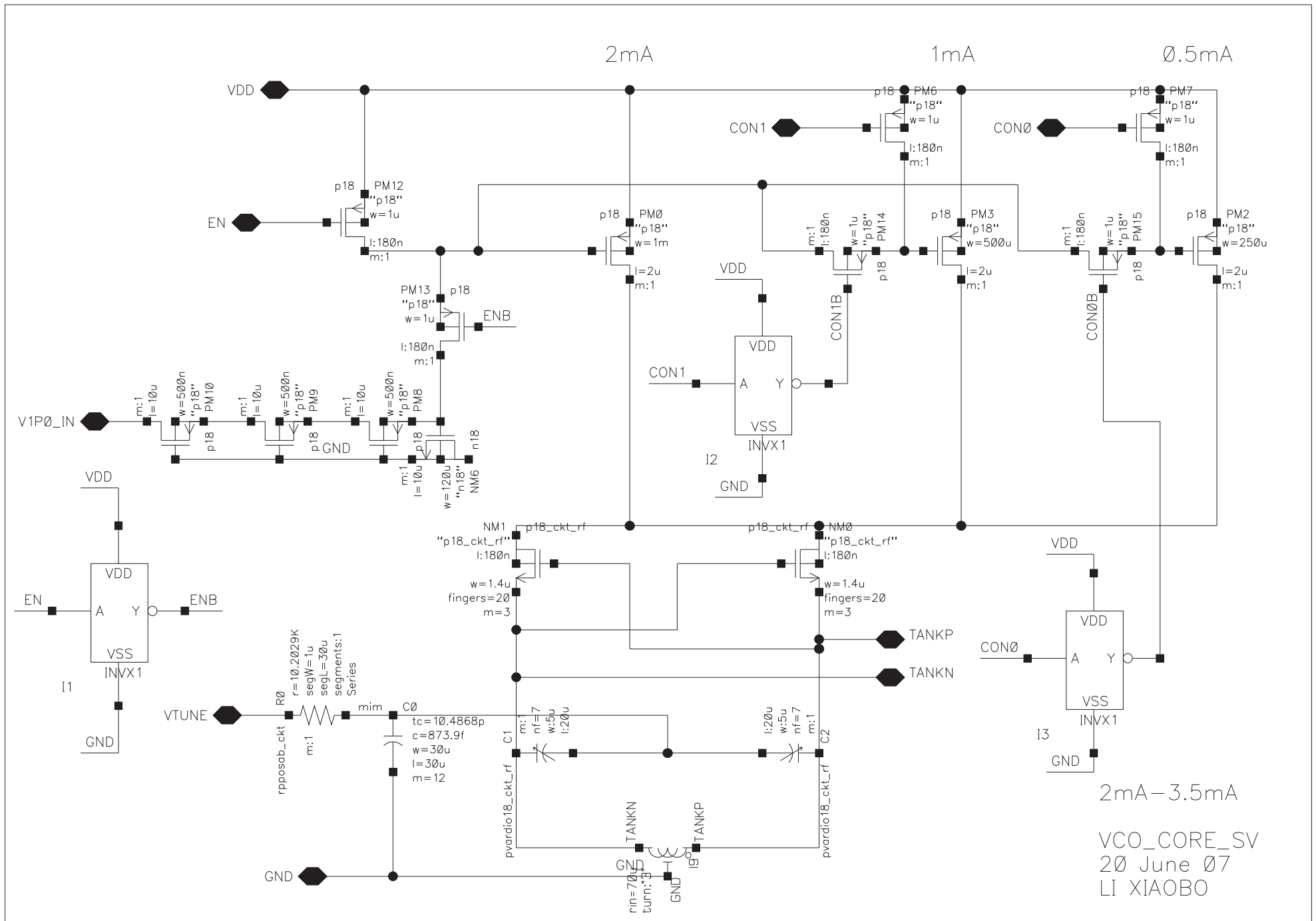


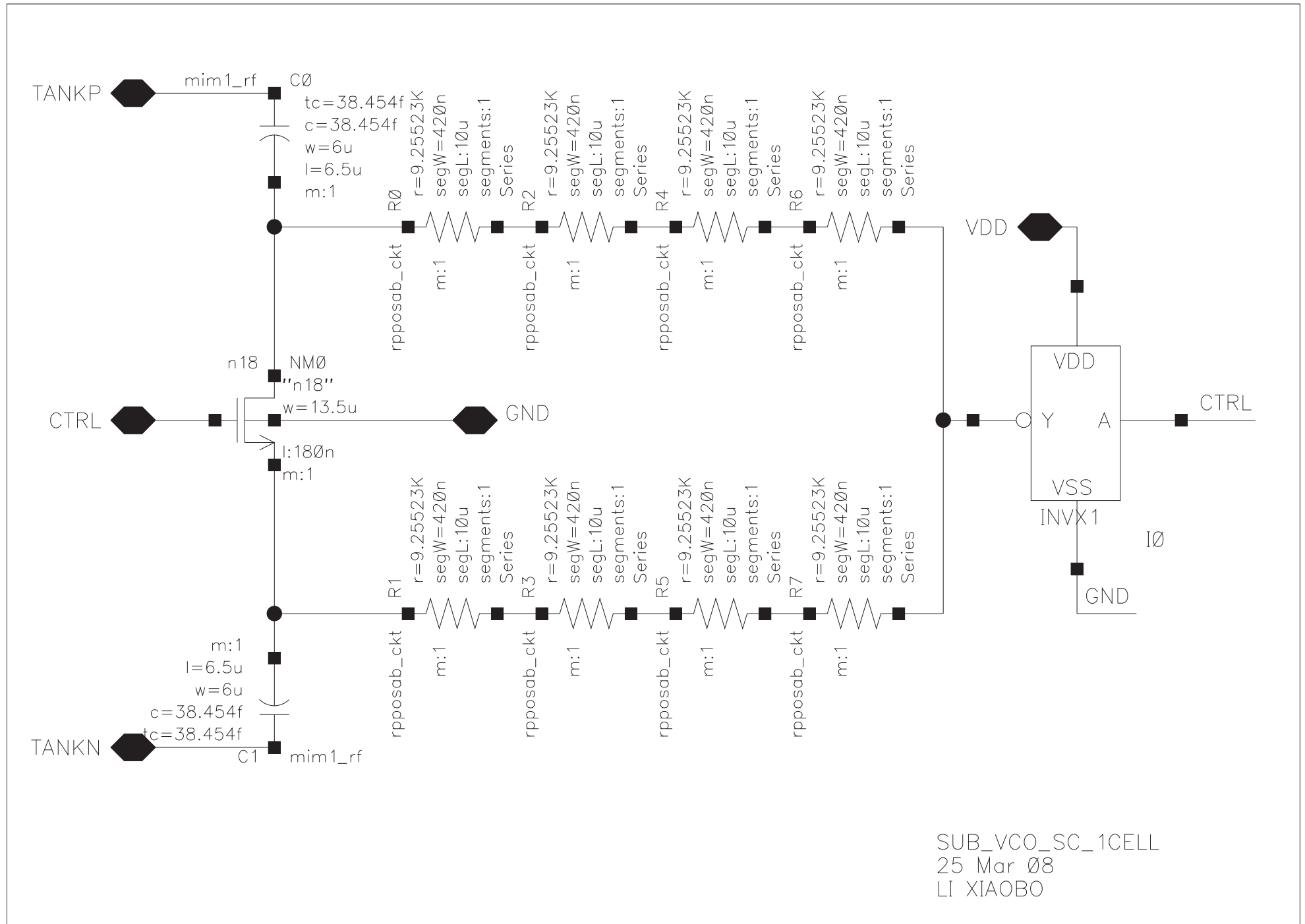






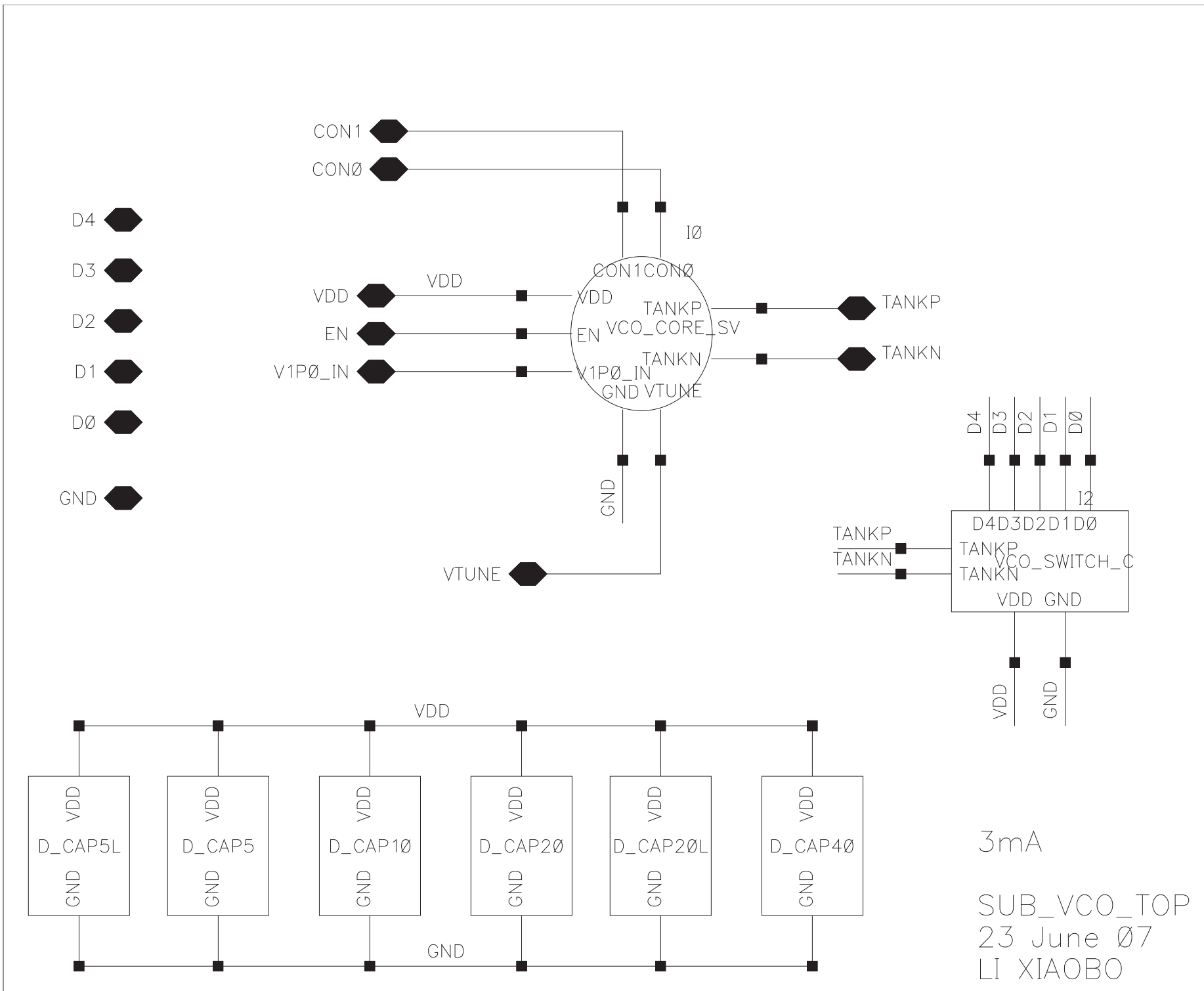








SUB\_VCO\_Switch\_C  
 25 MAR 08  
 Li Xiaobo

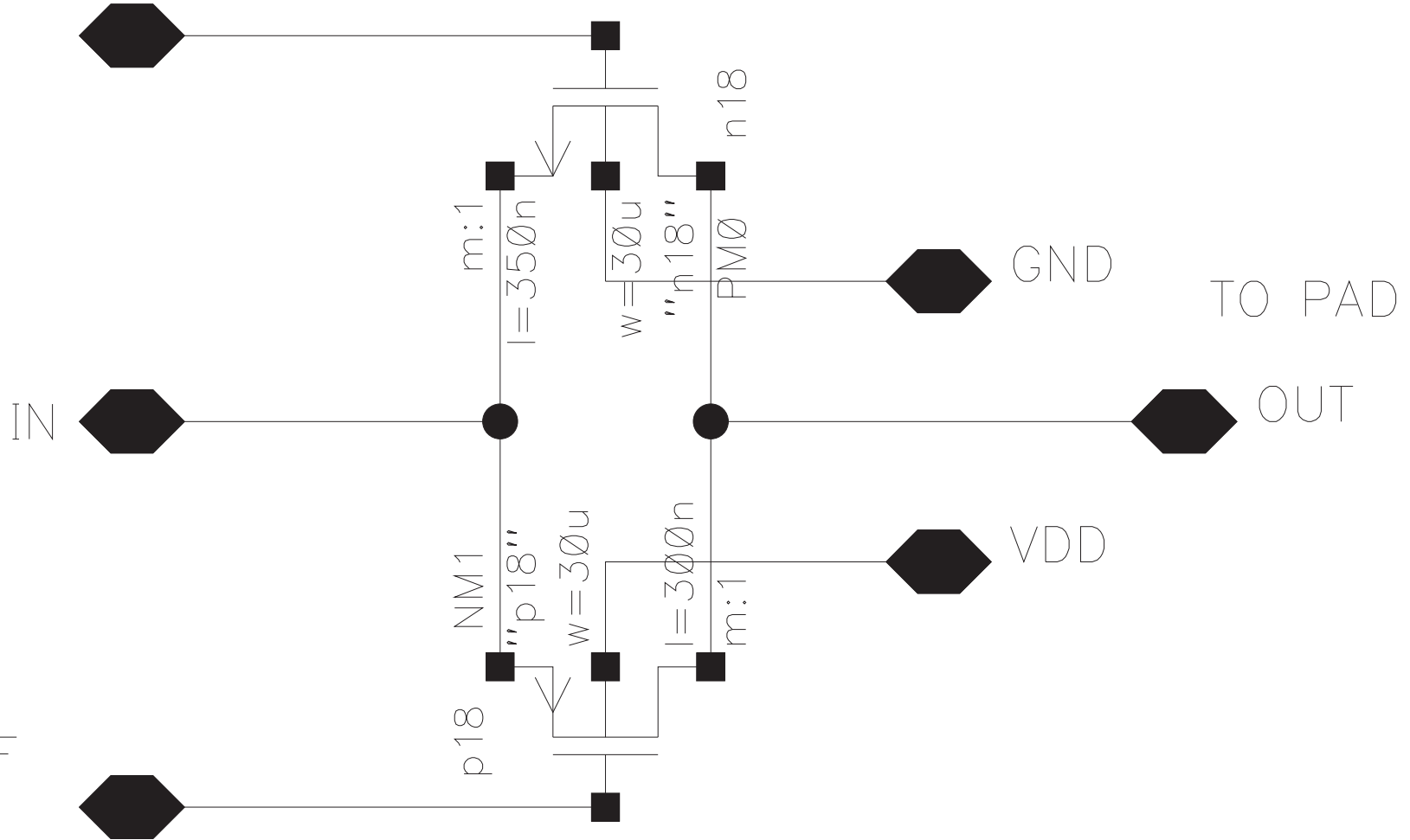


NOTE:

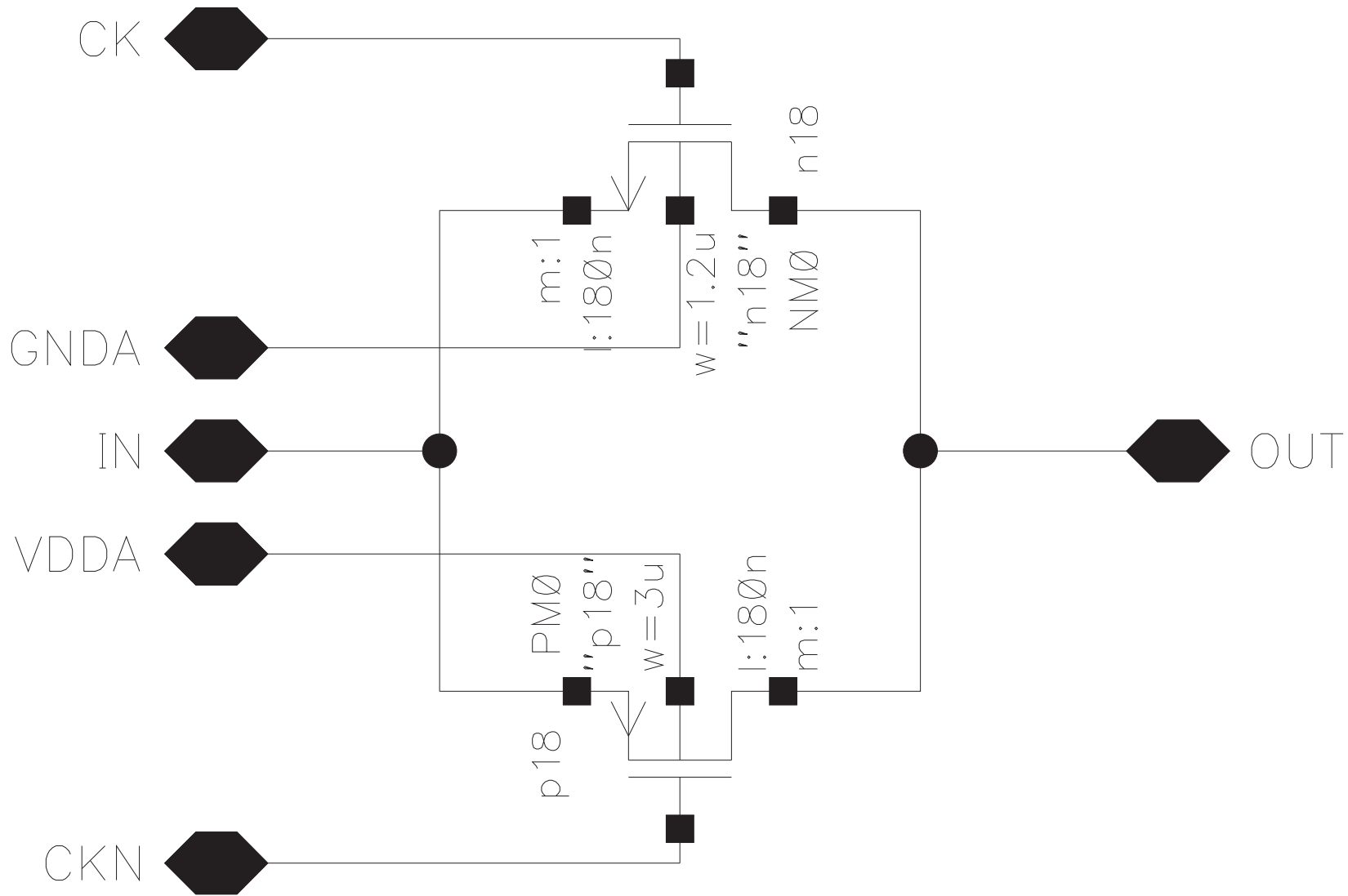
We must connect the DRAIN to the PAD.

Must layout according to ESD rule for drain.

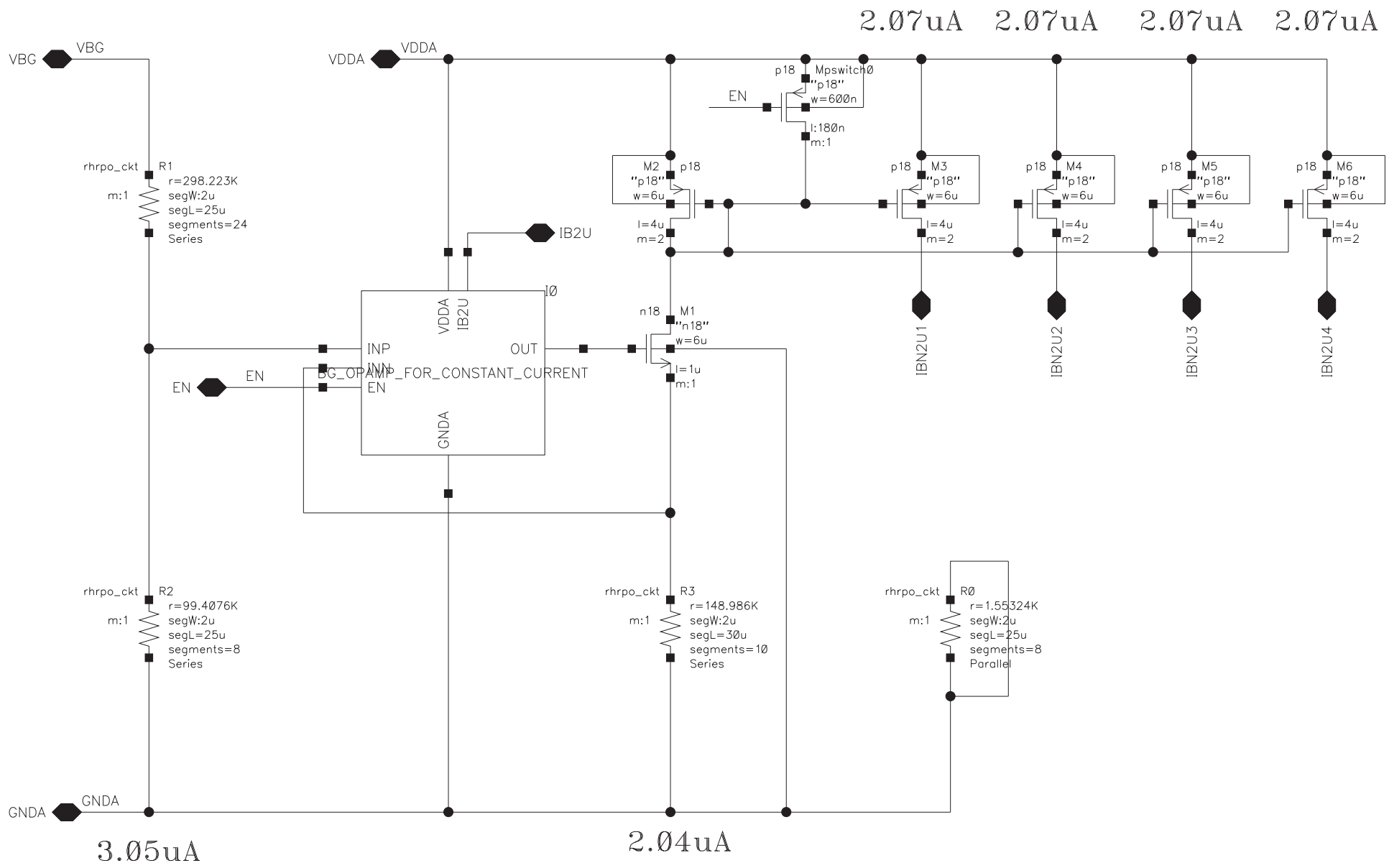
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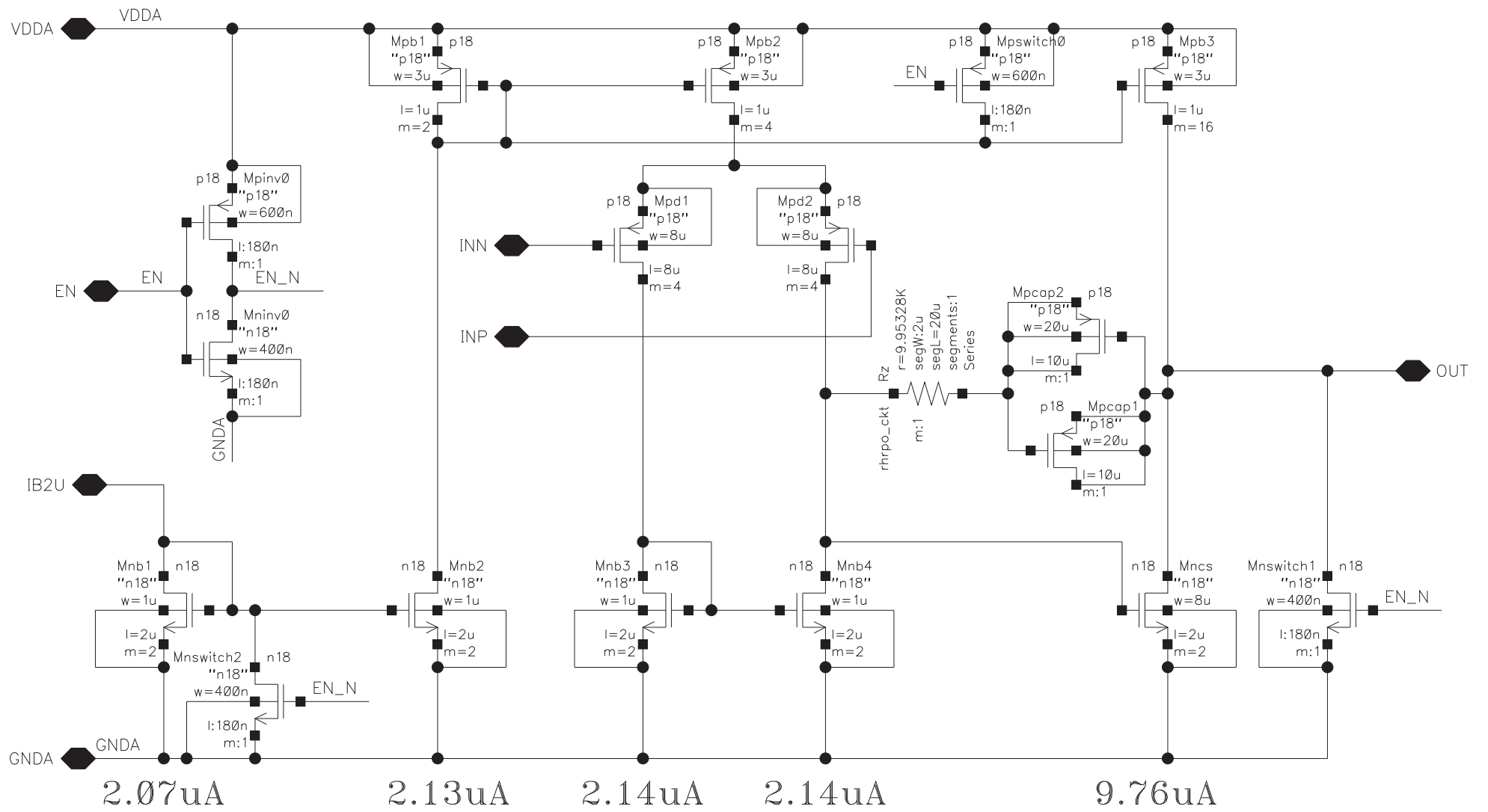


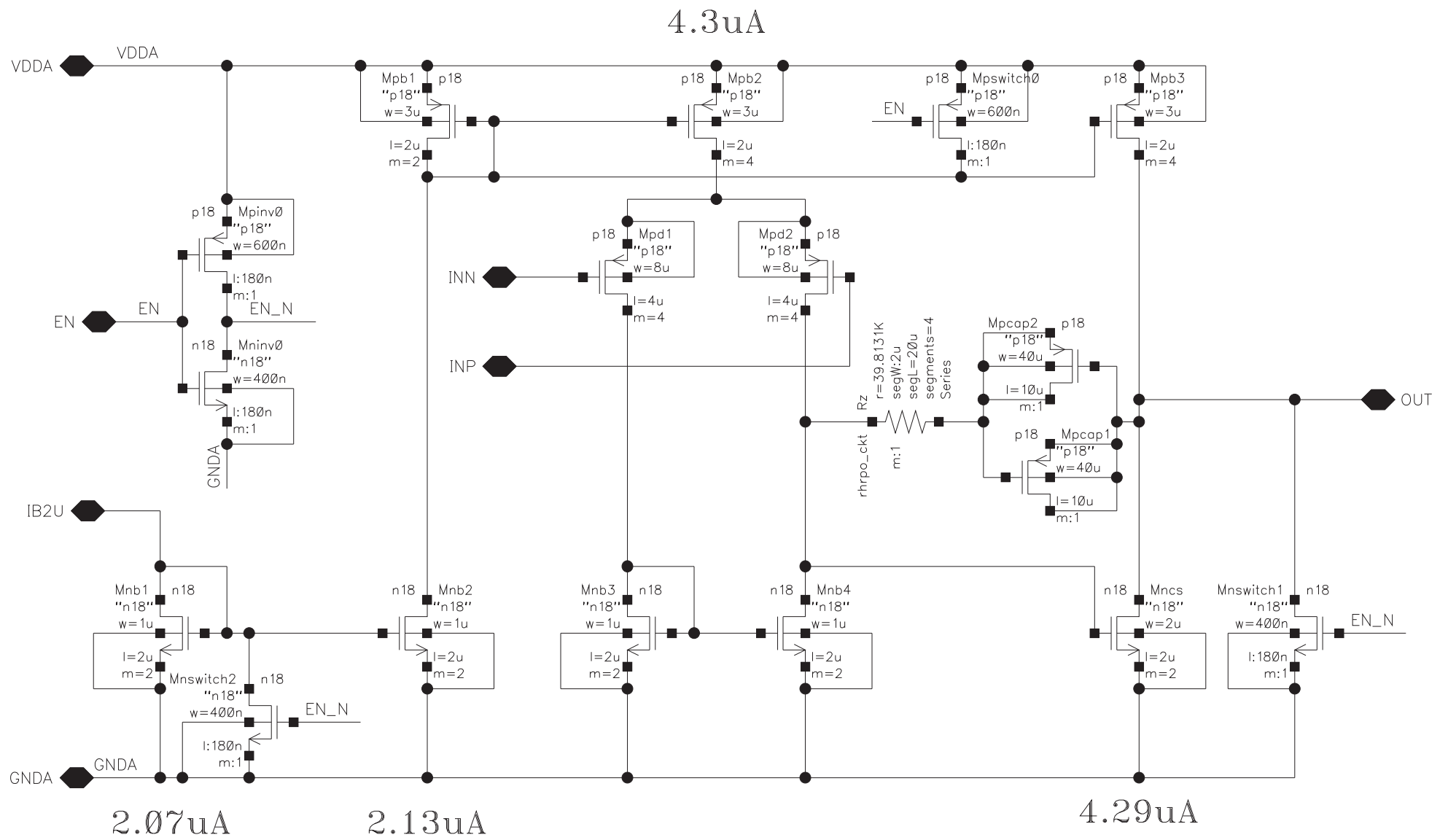
OFF



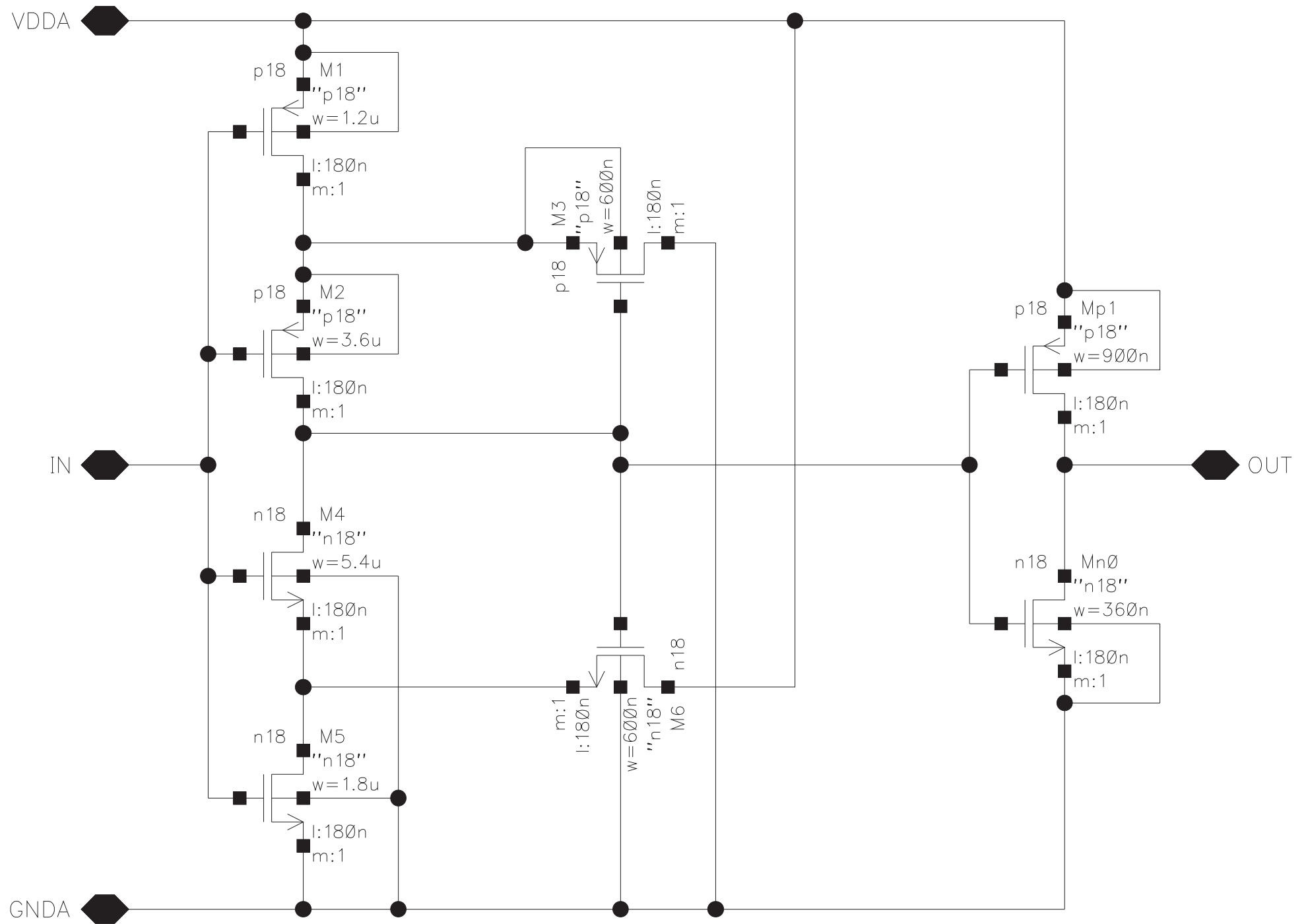


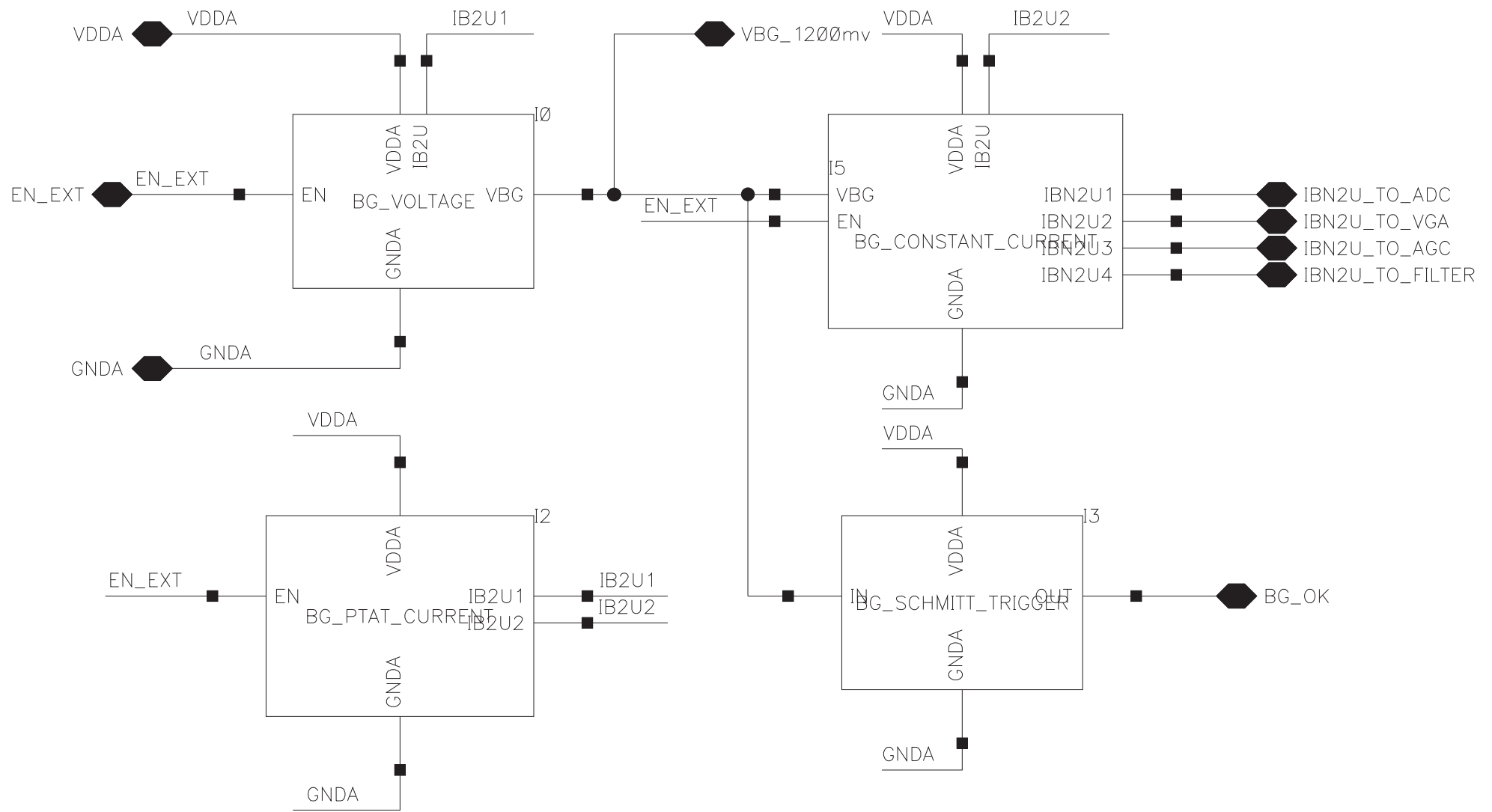


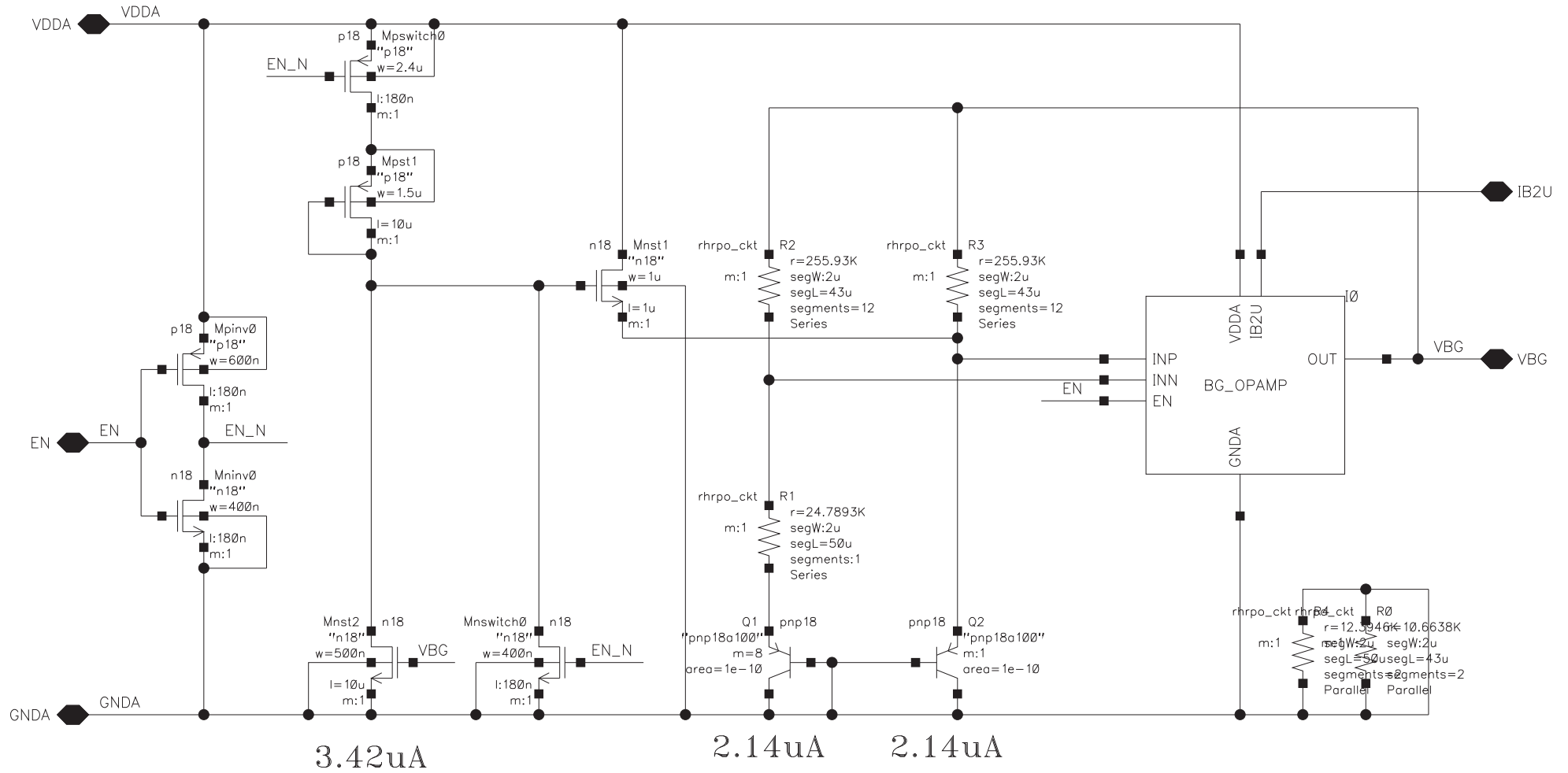


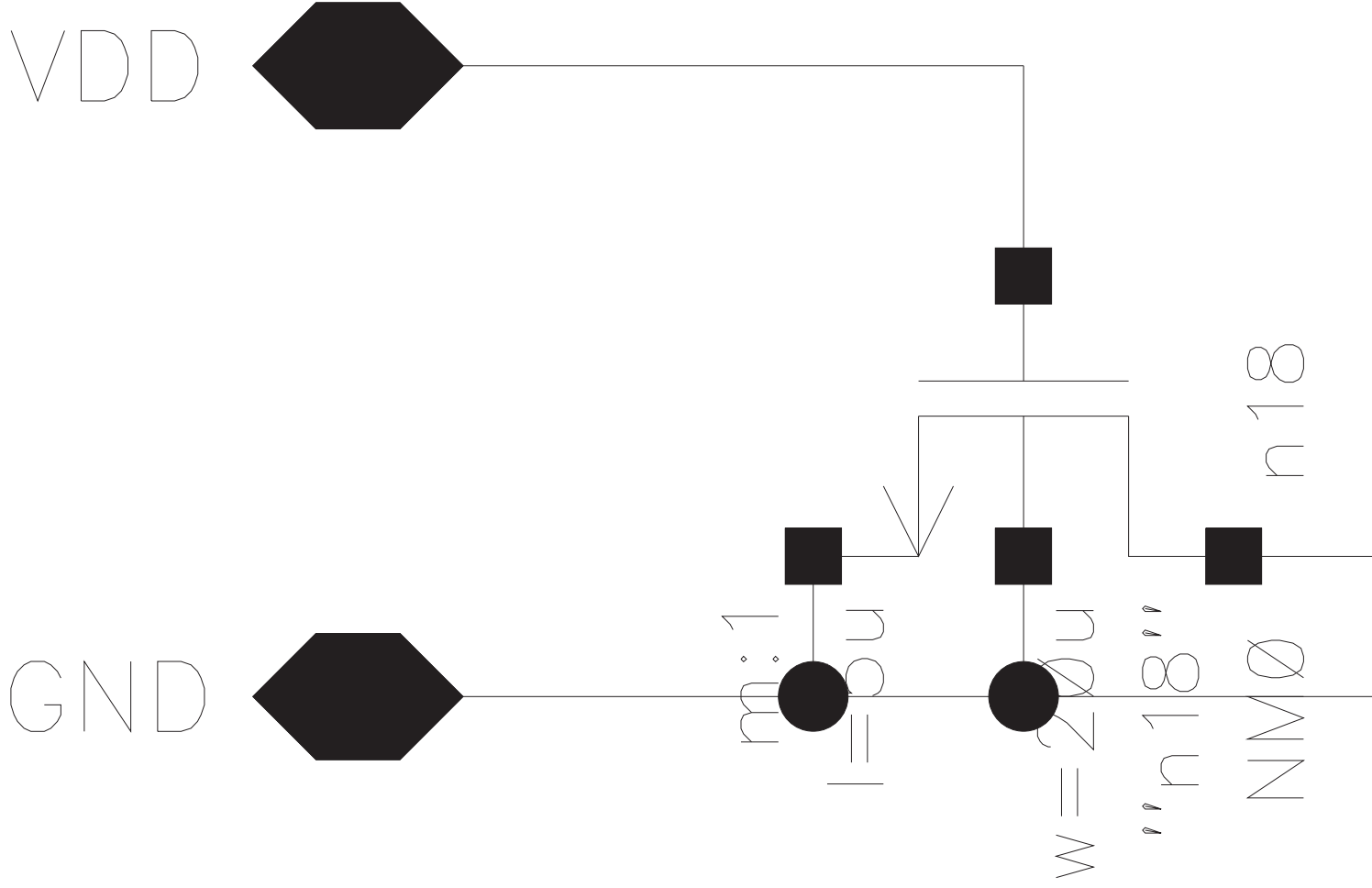




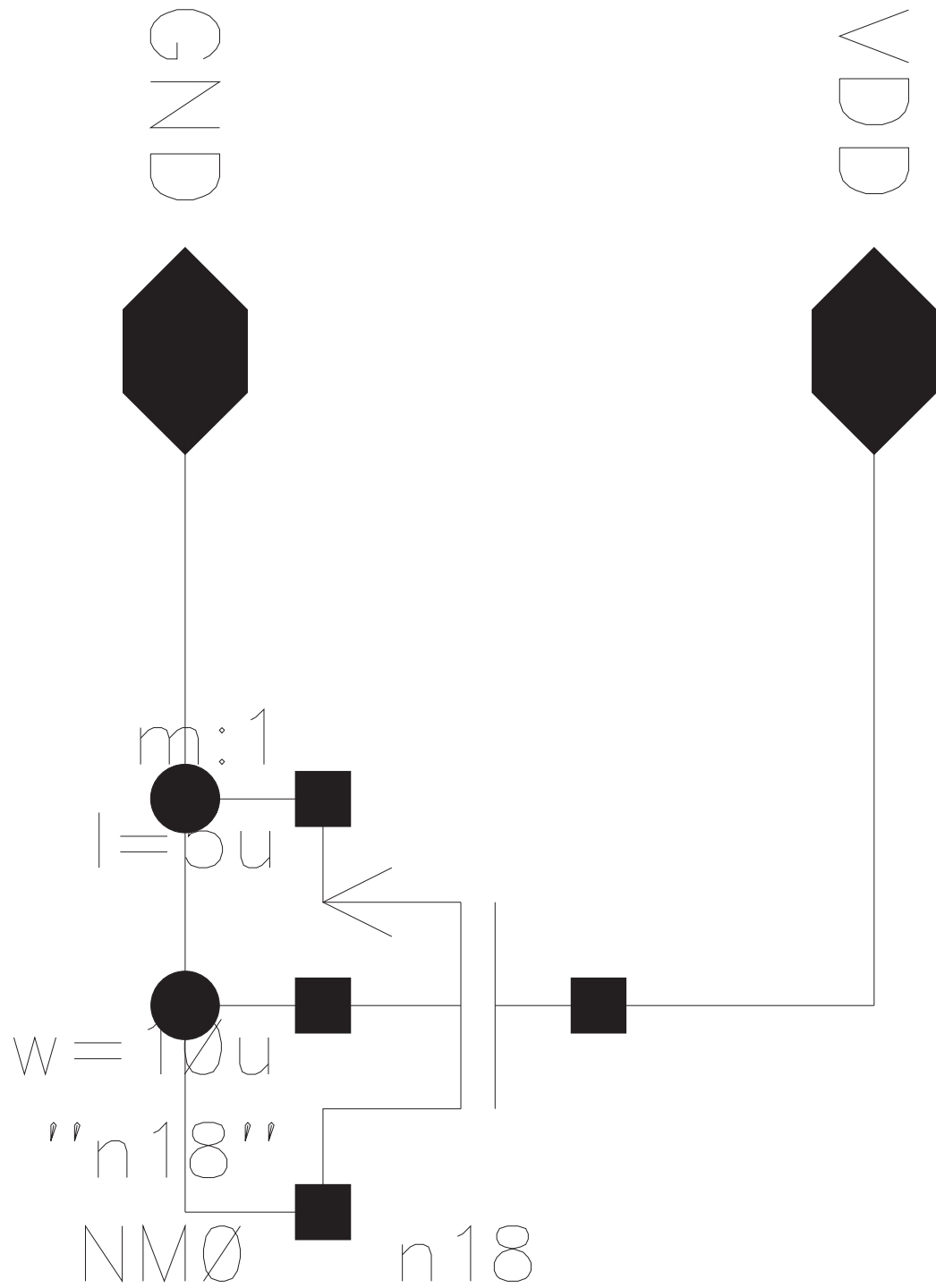


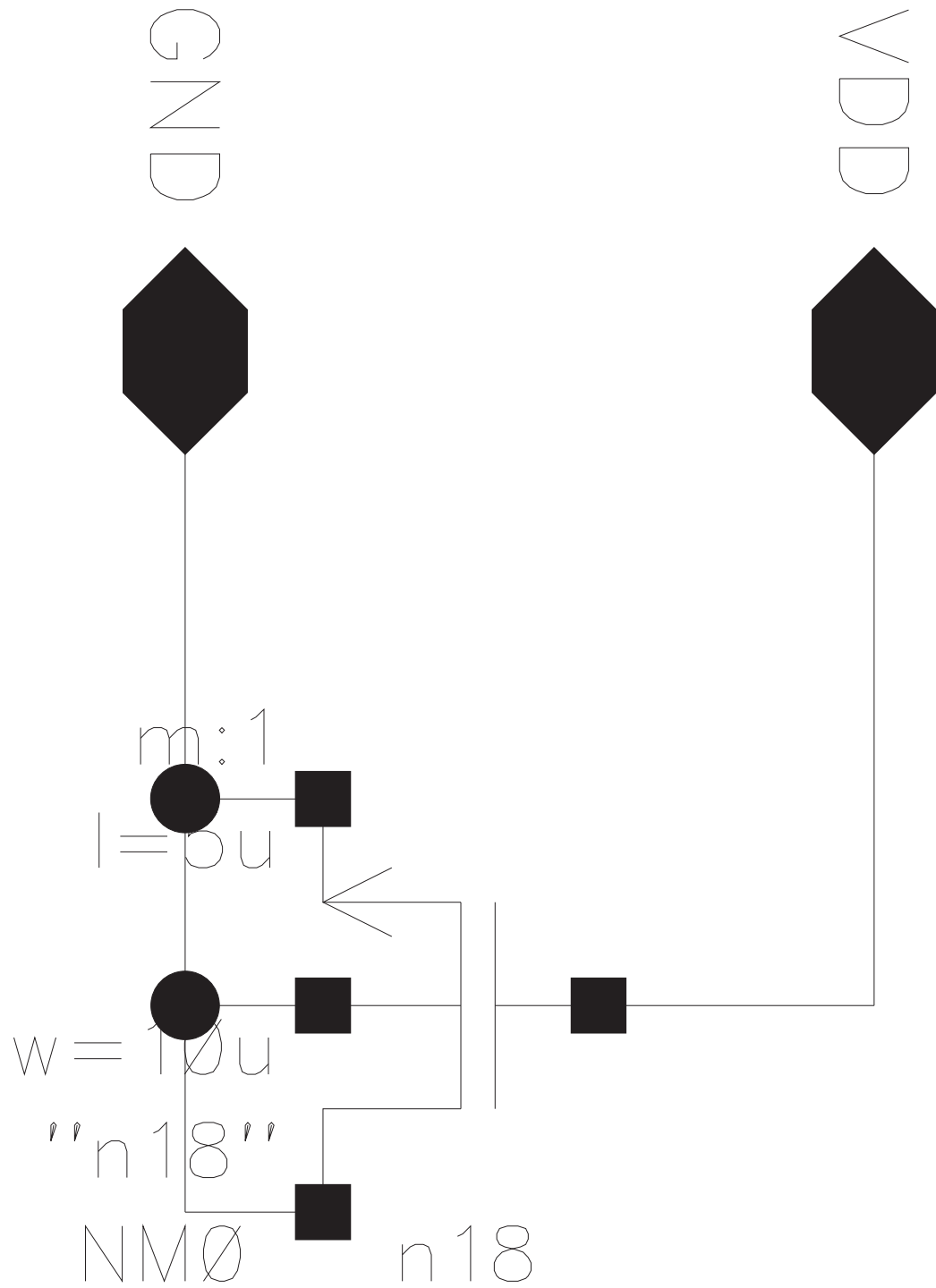


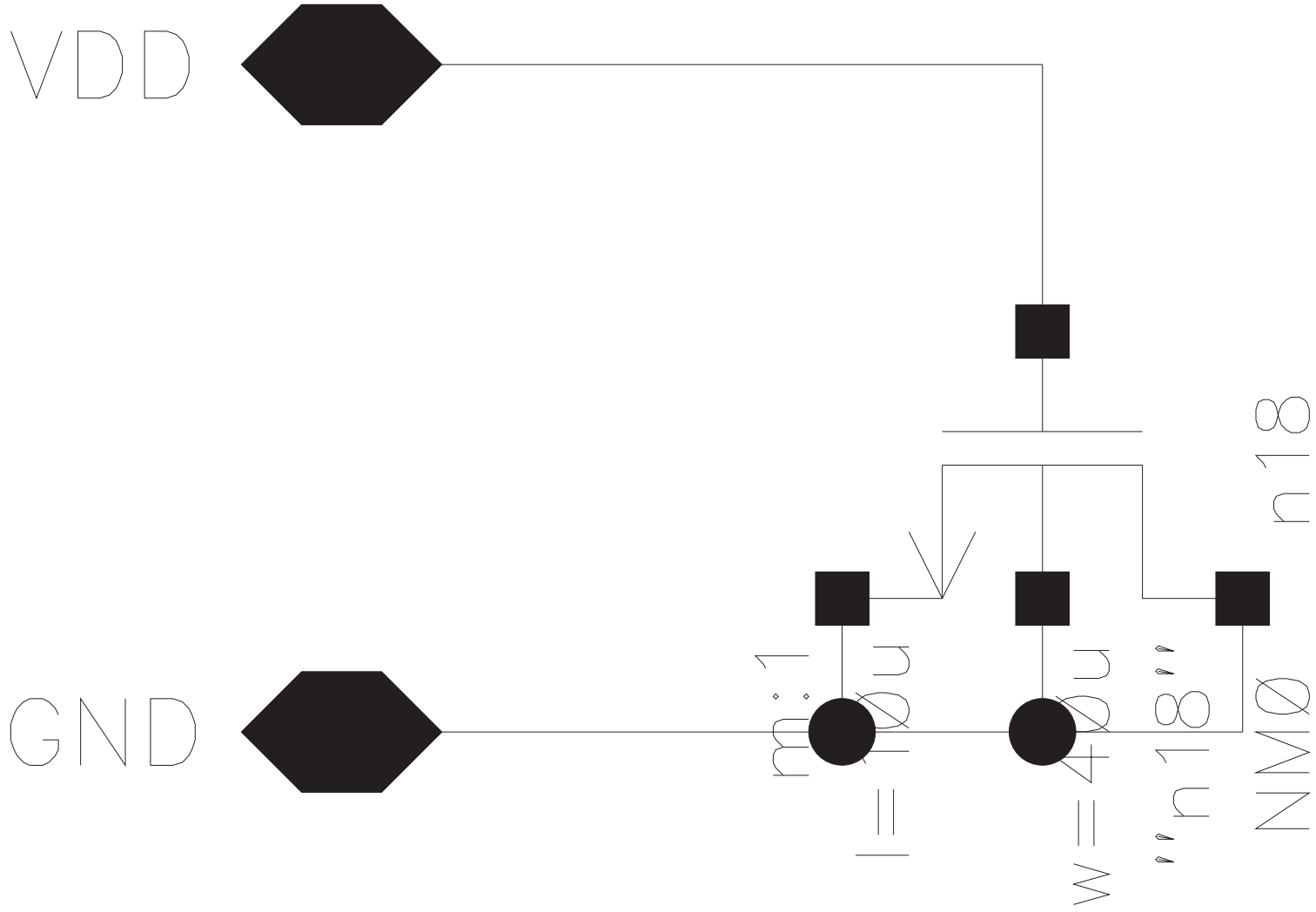


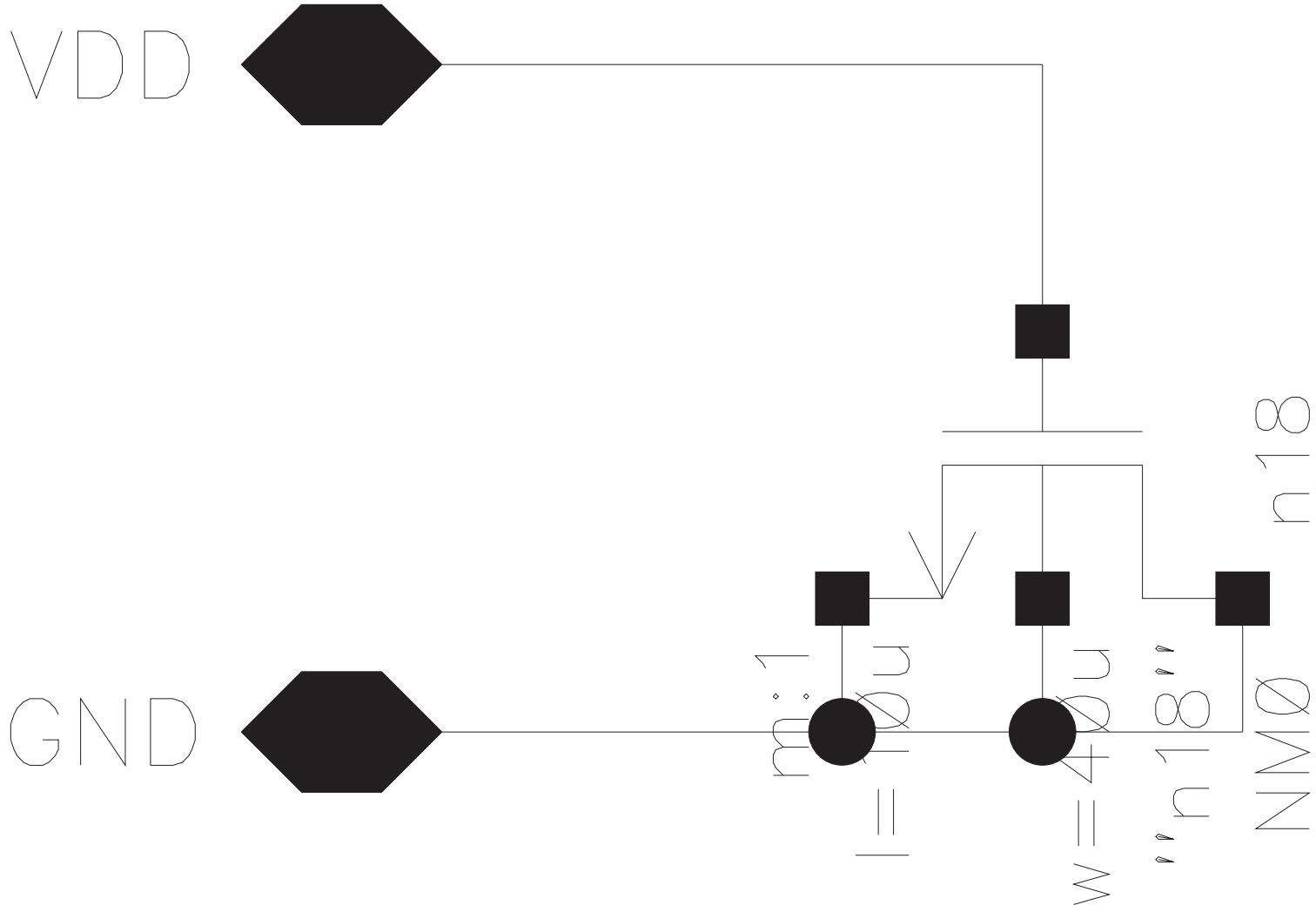


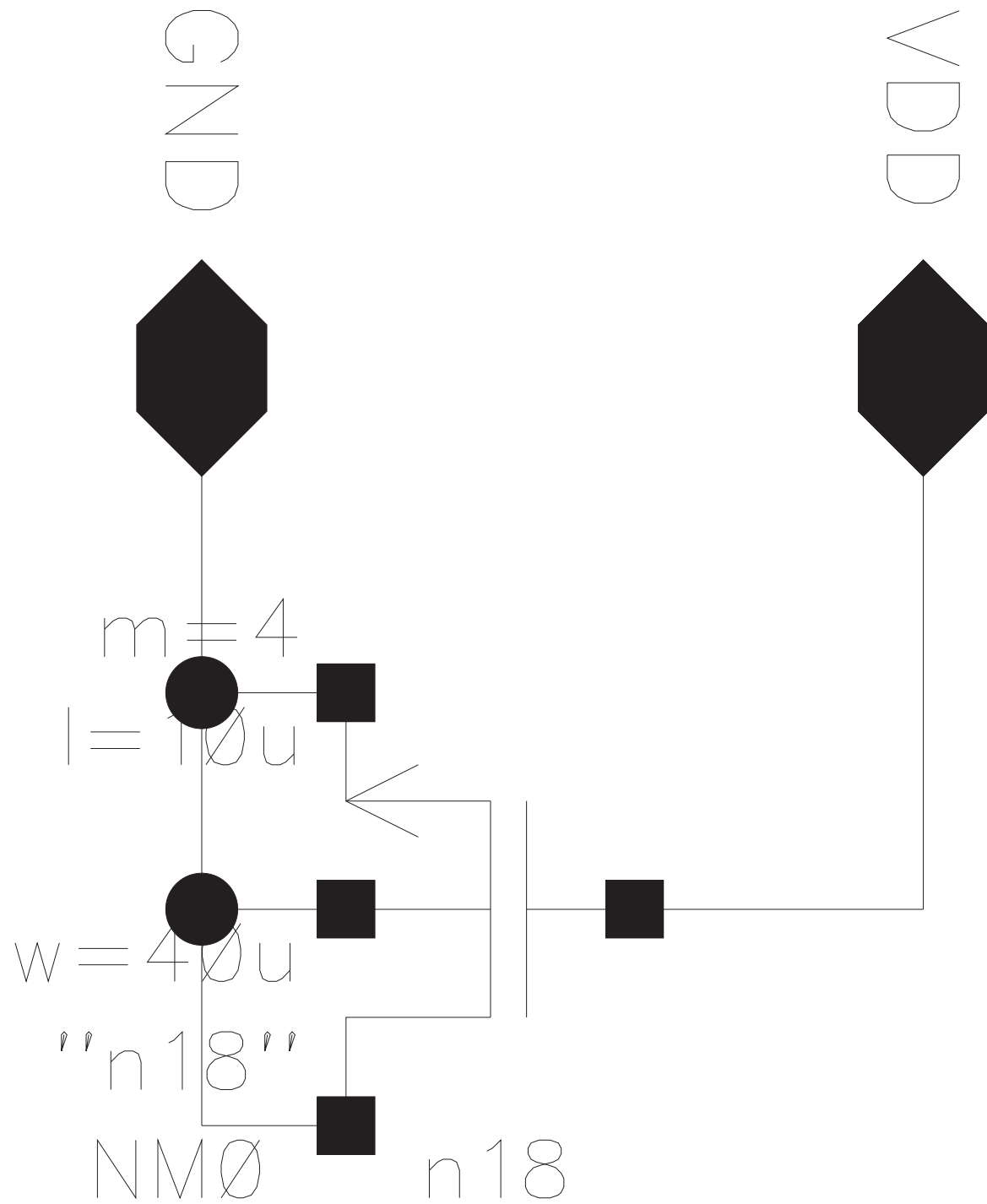


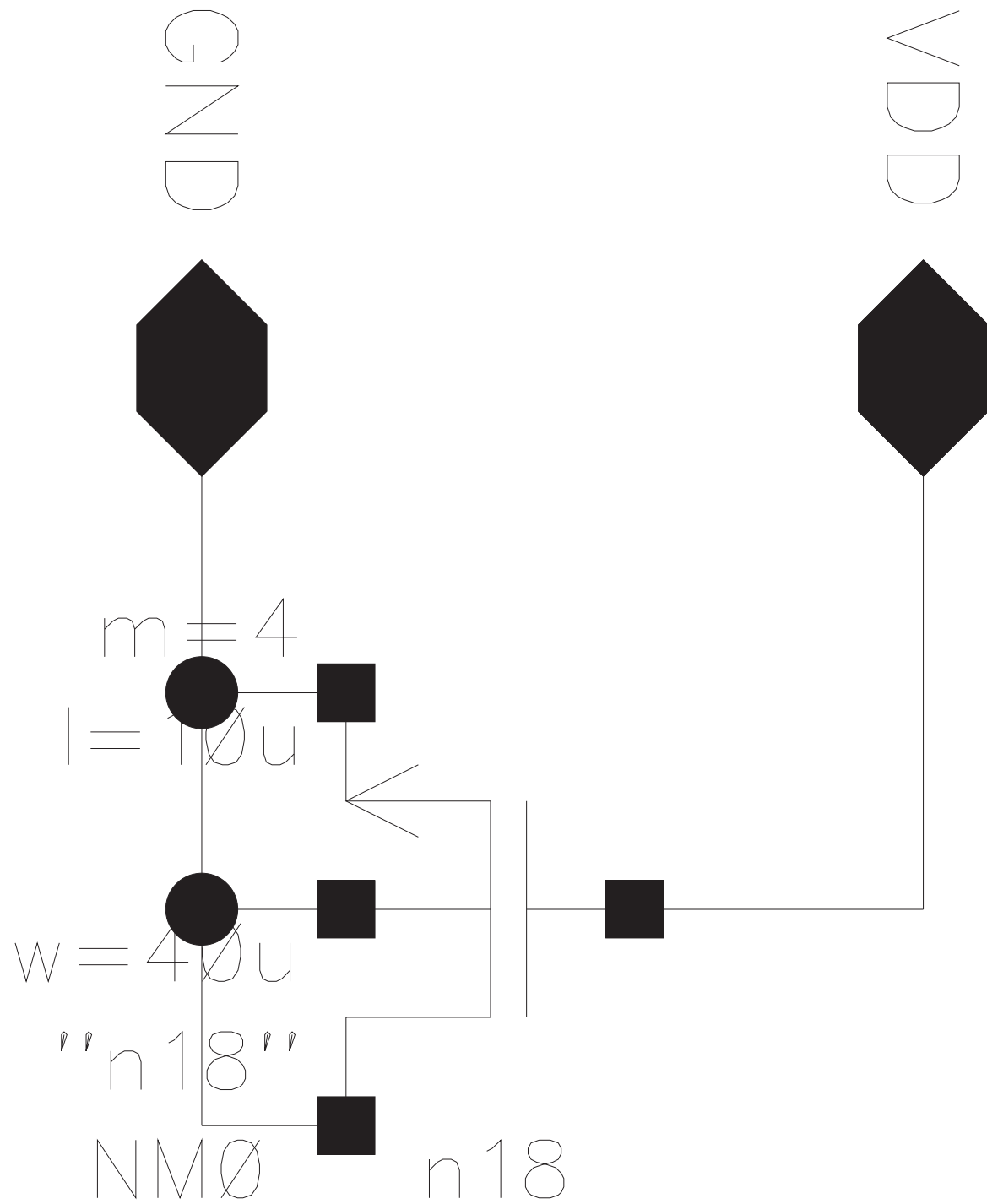




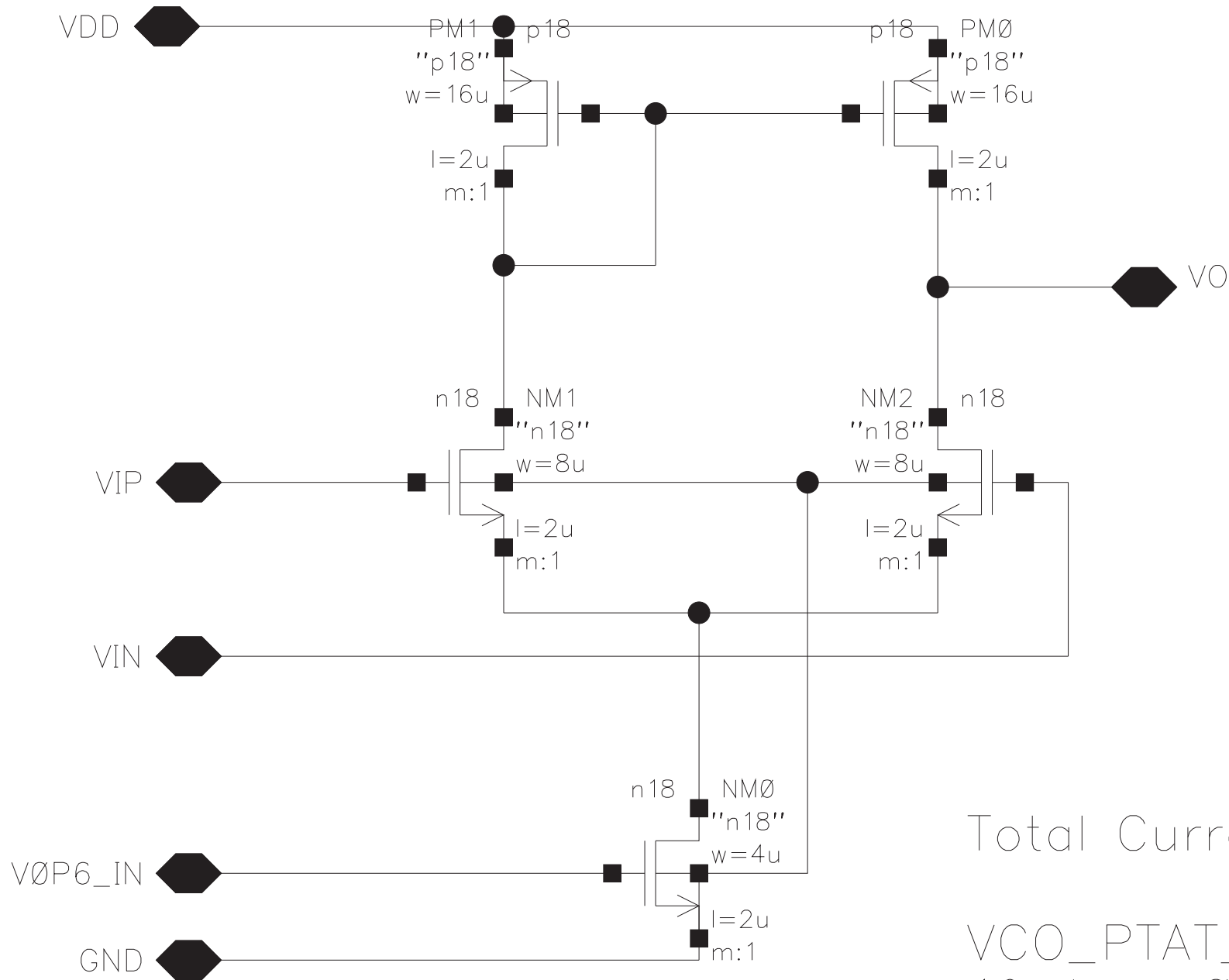












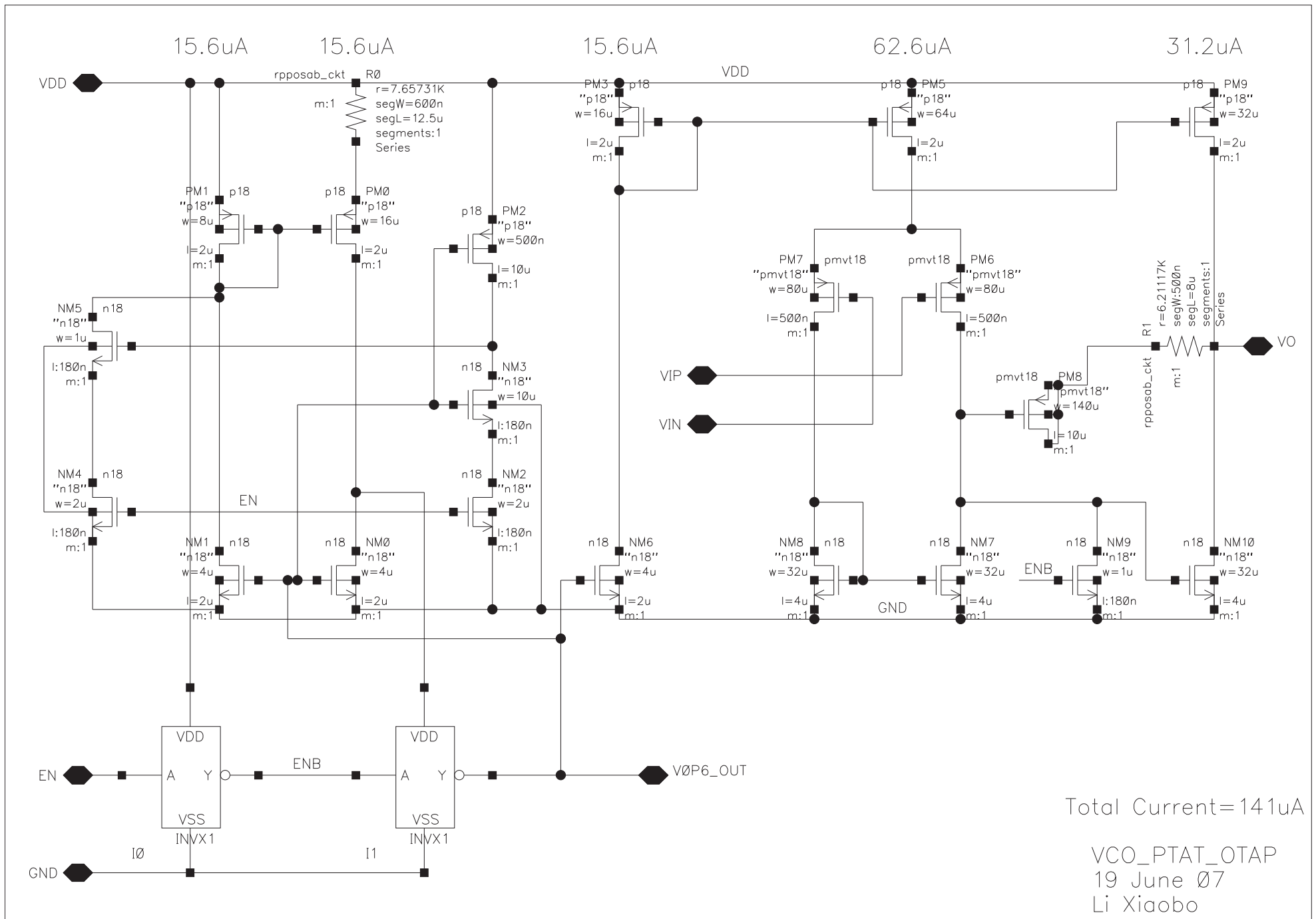
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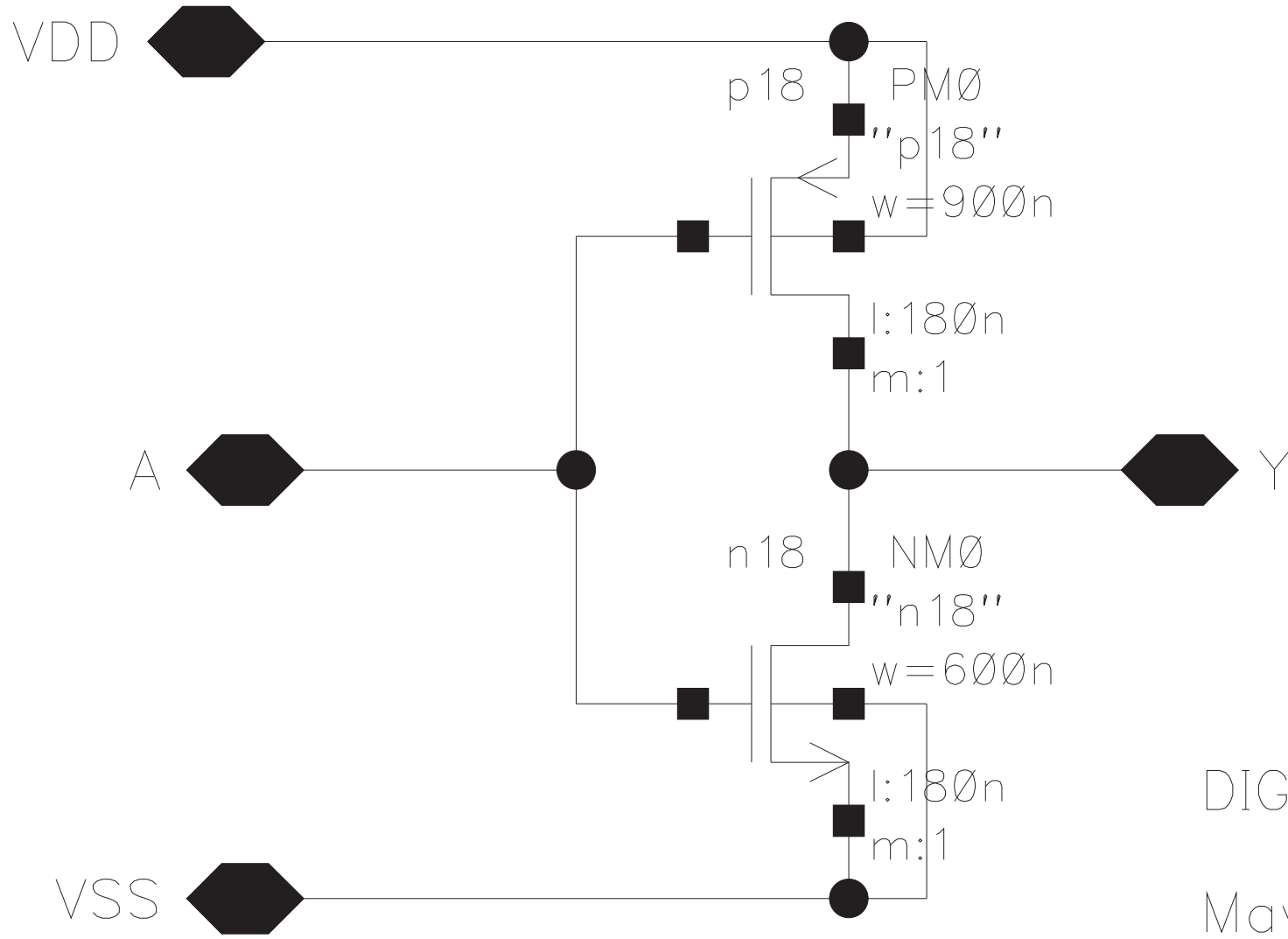
VCO\_PTAT\_OTAN

19 June 07

Li Xiaobo





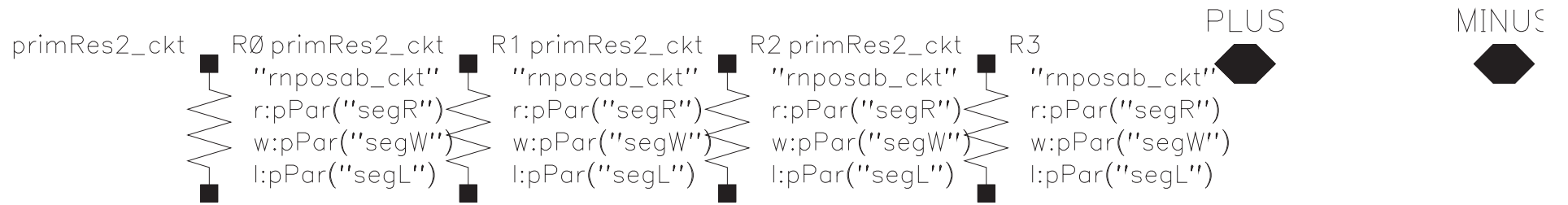


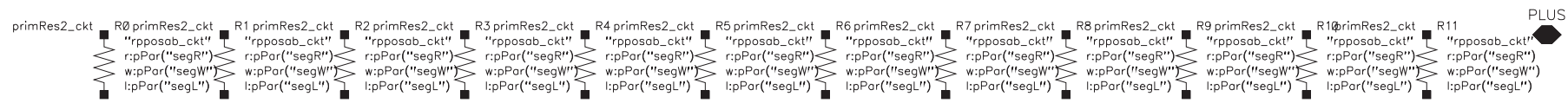
DIG\_INVX1

May 17 2007

Haibin Yang





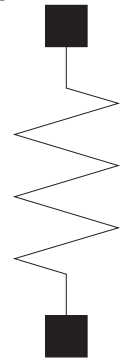


PLUS

MINUS

rfprimRes2

R0



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r:pPar("segR")  
w:pPar("segW")  
l:pPar("segL")
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PLUS



MINUS

