**Lab 1: DC Analysis of Bandgap (BG) Voltage Reference**

Background:

Voltage reference and current reference are the necessary blocks in most of the analogue IC. The circuit in Lab1 provides a constant-voltage reference and an Iptat. DC simulation will be performed to see the accuracy of voltage and current reference against PVT variation.

Objectives:

* Familiarisation with Schematic Editor: Cadence Composer
* Familiarisation with Analog Simulator: Cadence Analog Artist
* Familiarisation with DC simulation for a BG Voltage Reference Circuit

1. Invoke Cadence Design Software
   1. Click on the Terminal Window icon to get terminal window.
   2. Type **cd training** at the prompt to change the directory to training.
   3. Type **source .cshrc\_linux**
   4. Type **virtuoso&**
   5. The Command Interpreter Window (CIW) and Library Manager Window appear as shown.

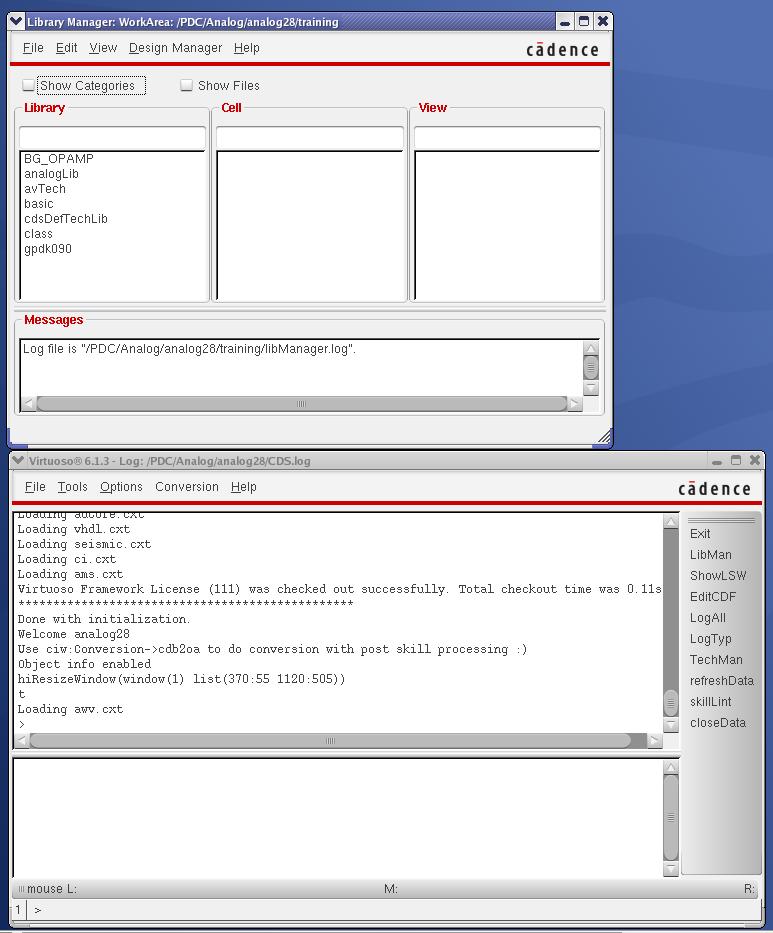


Figure 1: CIW and Library Manager Window

1. Open the schematic (test bench) of Bandgap Voltage Reference
   1. In the Library Manager, double-click on **BG\_OPAMP/BG\_test\_DC/Schematic** as shown in Figure 2.
   2. Click on symbol BG and hit the key ‘**E**’ to descent into the sub-circuit BG.
   3. You could spend some times looking at the details of the circuit.
   4. Hit the key ‘**CTRL-E**’ to go back to the top level schematic.

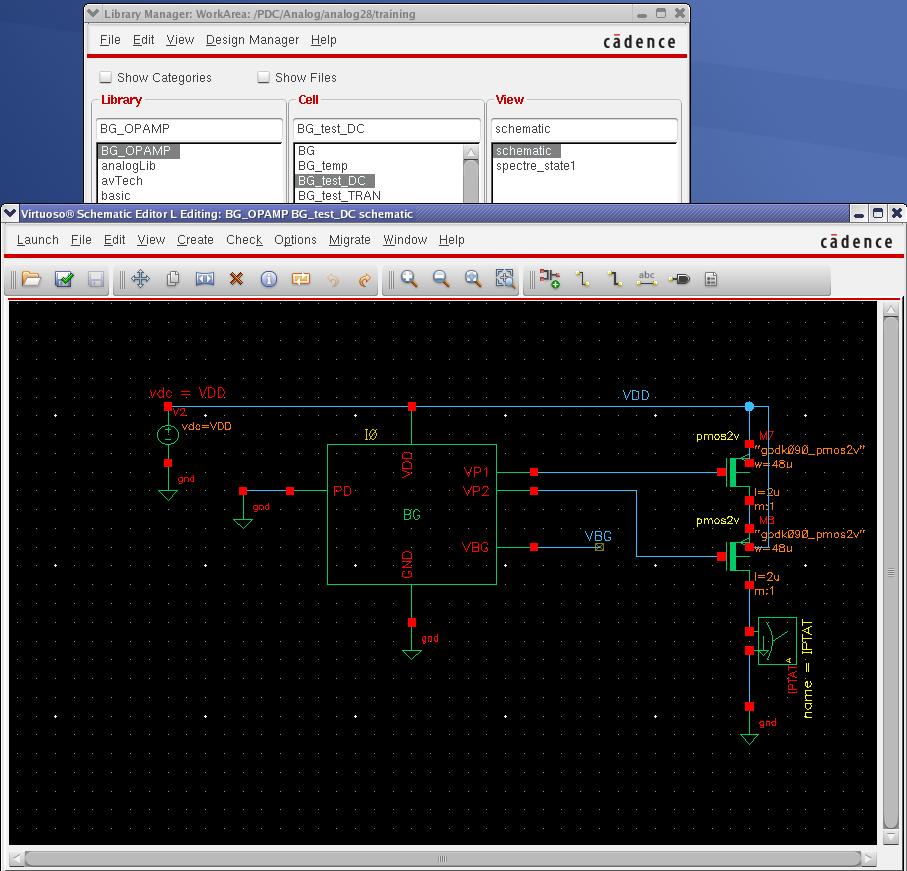


Figure 2 Test Bench of BG Voltage Reference

1. Launch the Analog Design Environment (ADE)

ADE is the interface for you to set the various parameters required for a simulation. In the Schematic Editor Window, click **Launch>ADE\_ L**. ADE is as shown in Figure 3.

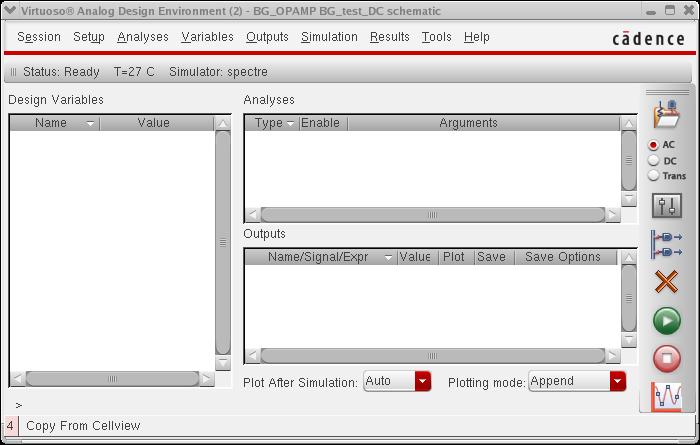


Figure 3 ADE Window

1. Setup of Simulation
   1. Click **Variable>Copy\_From\_Cellview**. Double-click on ‘VDD’. Set VDD to 2.5.
   2. Click **Analyses>Choose**. Set up the DC simulation as shown in Figure 4. Click **OK** when completed.

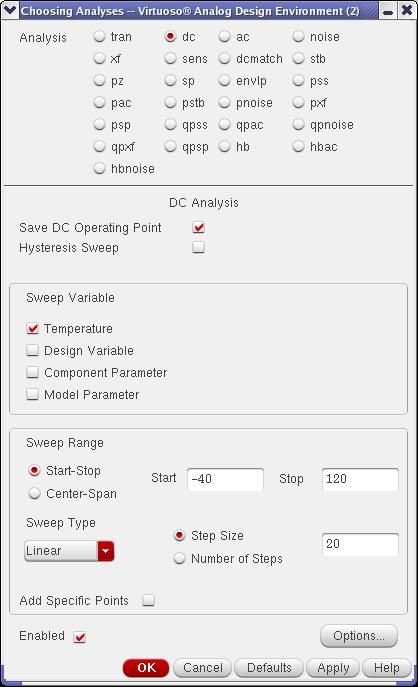


Figure 4 DC Simulation Setup

* 1. Click **Outputs>To\_Be\_Plotted>Select\_On\_Schematic**. As shown in Figure 5, click on VBG, follows by positive-terminal of IPTAT (current probe). Then hit ‘**Esc**’.

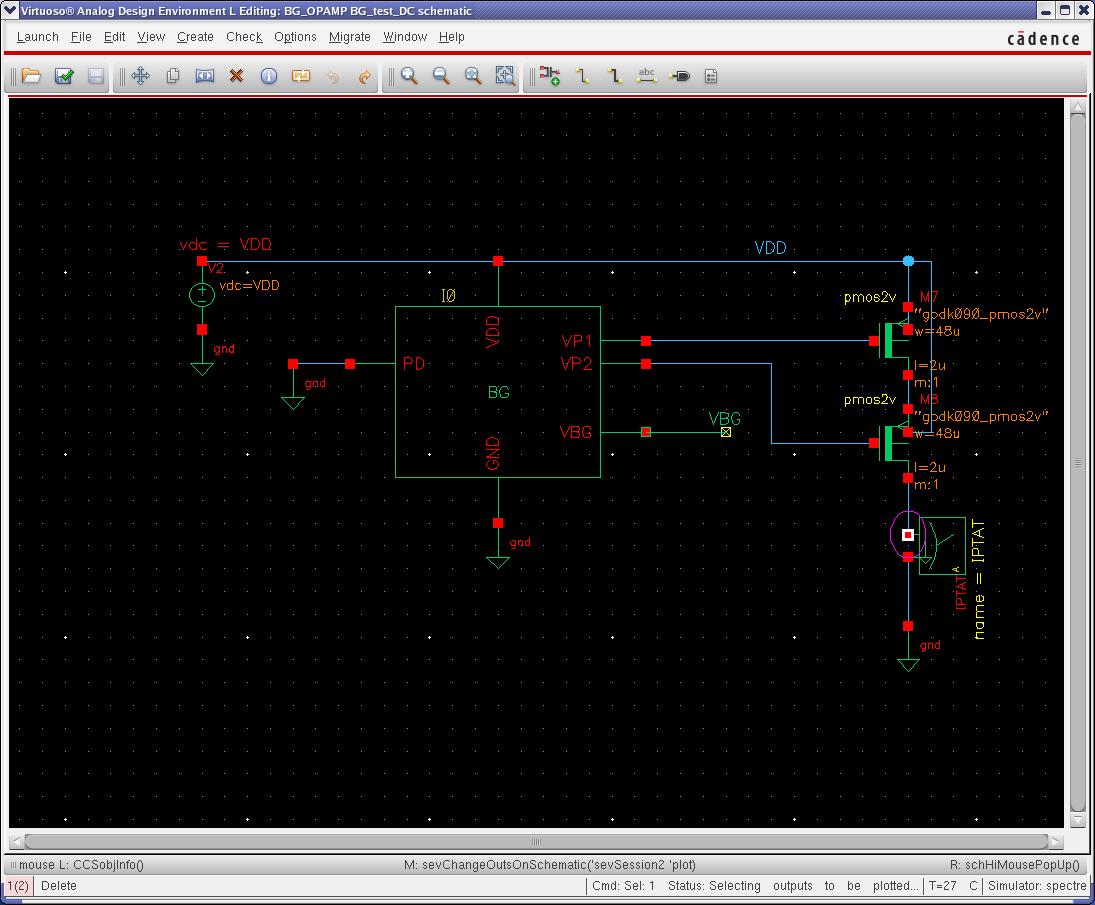


Figure 5 Selection of Net for plotting

* 1. If you have problems in set up the simulation, in ADE, click **Session>Load\_state** as shown in Figure 6. For convenience, the simulation setup (state) can be saved and recalled for future use.

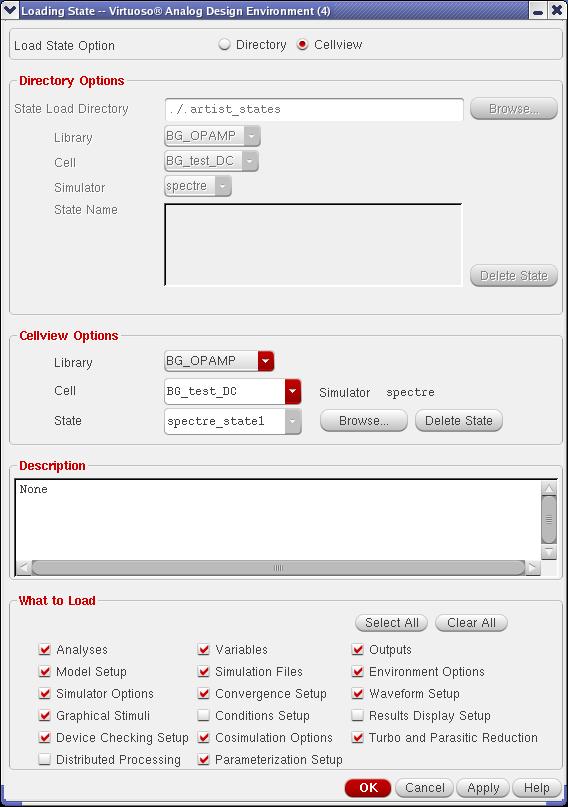


Figure 6 Load State

* 1. As shown in Figure 7, click the **green button** to netlist and simulation the circuit. The progress of the simulation will be displayed as shown on the left side of Figure 7.

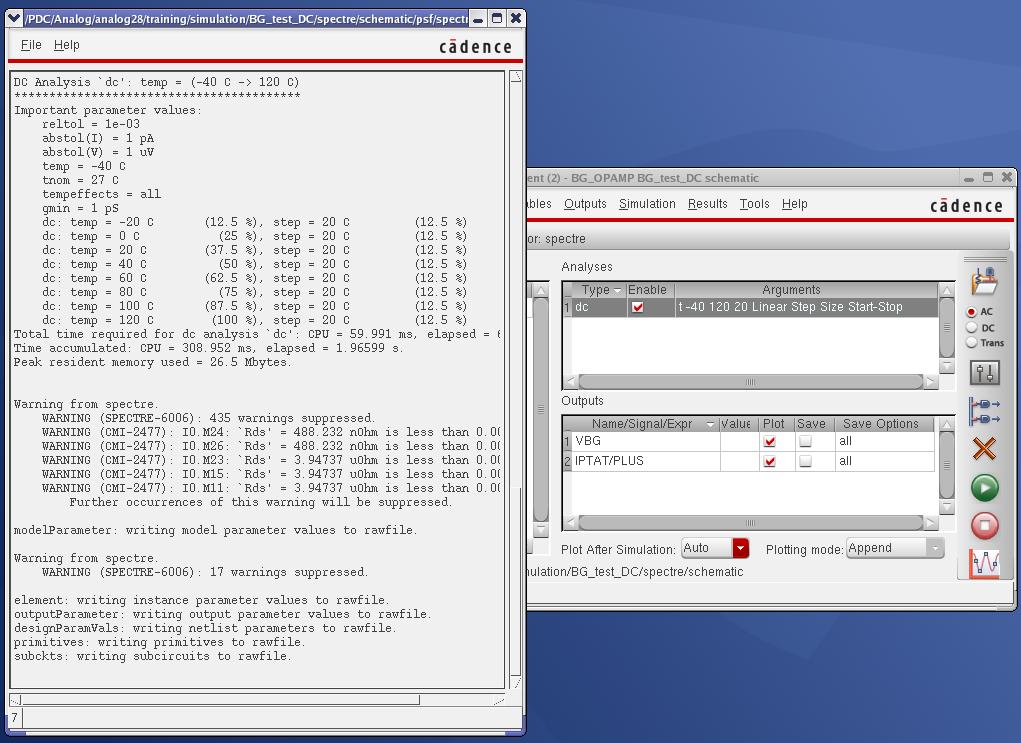


Figure 7 Netlisting and Simulation

1. Plot and Graph
   1. Click on ‘**New Subwindow’** as shown in Figure 8. A new subwindow will be created.
   2. Click on /IPTAT/PLUS and drag it to the new subwindow.



Figure 8 Result

* 1. It is shown that VBG is relatively constant with respect to the temperature. As for the IPTAT, it is proportional to absolute temperature (PTAT). Click on the cross (Figure 7) to close the window.

1. Parametric Sweep
   1. In ADE, click **Tools>Parametric\_Analysis**. Set up the parametric sweep as shown in Figure 9. Click **Analysis>Start** to launch the simulation.

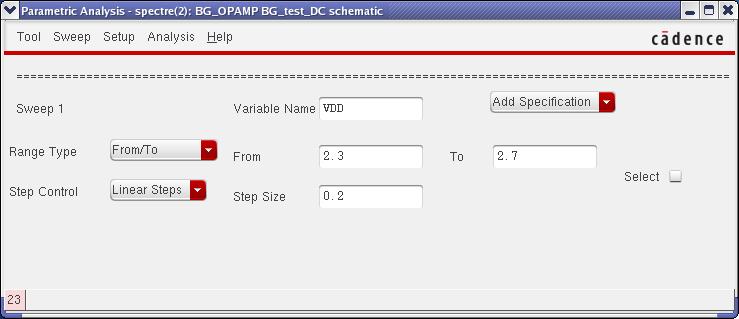


Figure 9 Setup of parametric sweep

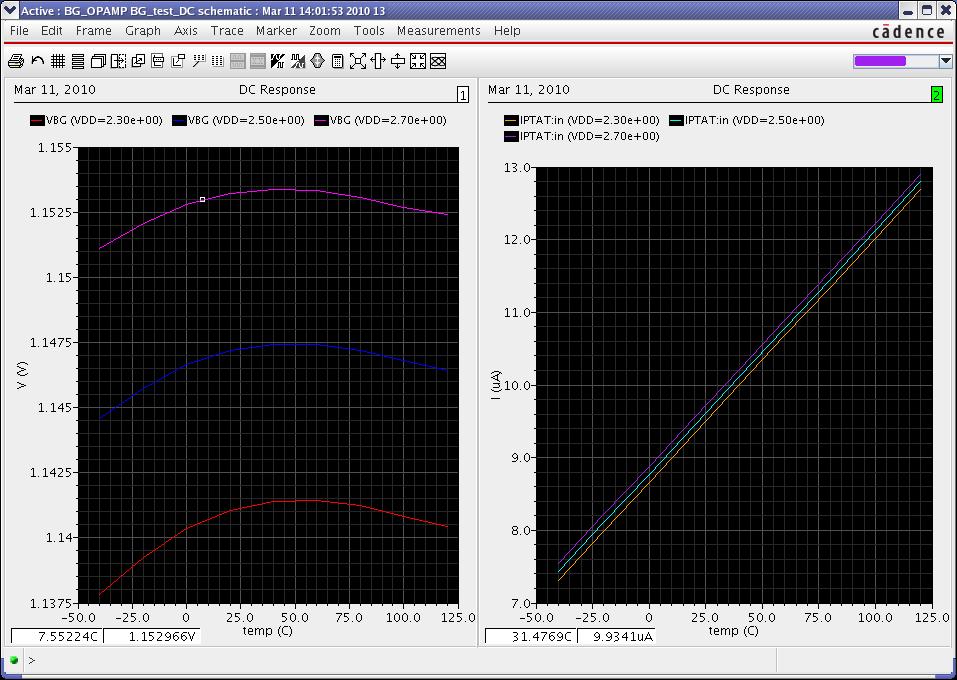


Figure 10 Result after parametric sweep

* 1. Create a new subwindow and drag all the current waveform to it. As shown in Figure 10, VBG and IPTAT vary with VDD. This implies there is some finite amount of PSRR.

1. Process Corner
   1. In ADE, click **Setup>Model\_Libraries**. Click on ‘**NN**’ of Section (Figure 11). ‘NN’ stand for nominal PMOS and nominal NMOS. Select ‘**SS**’ and click **OK**.
   2. In Parametric Analysis Window (Figure 9), click **Analysis>Start** to launch simulation.
   3. It can be observed that different process corner of components will give you different result (Figure 12).

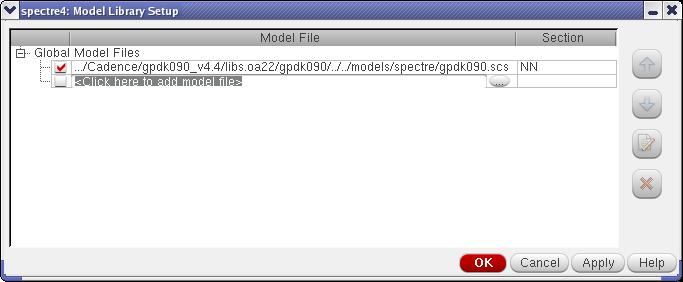


Figure 11 Setup of simulation model

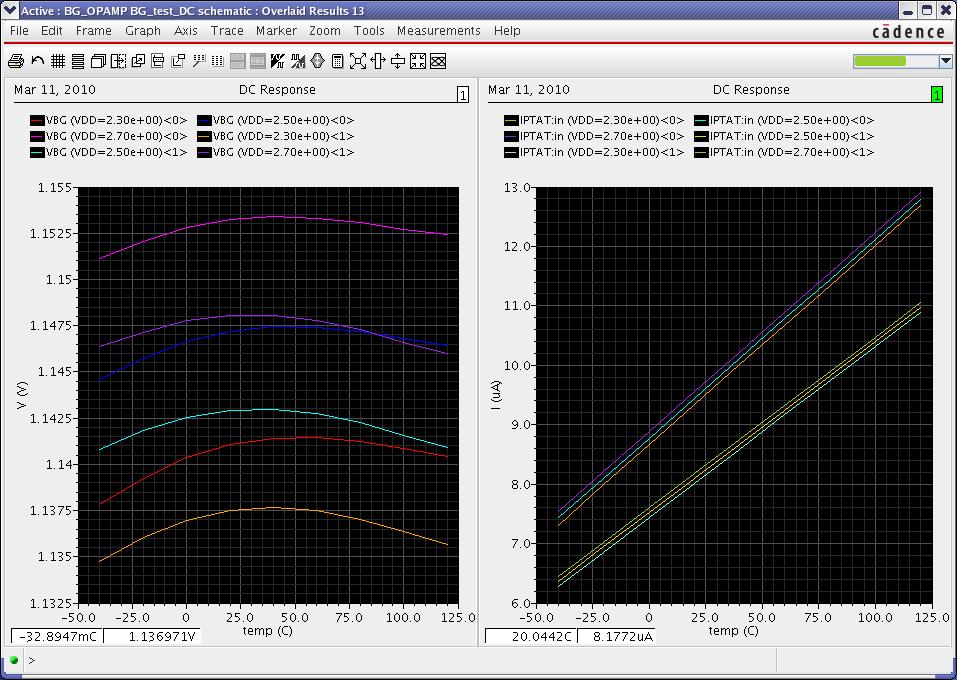


Figure 12 Result for different process corner