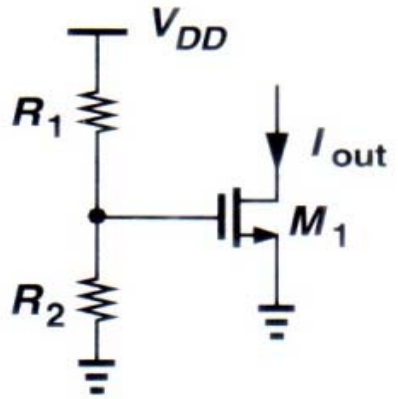
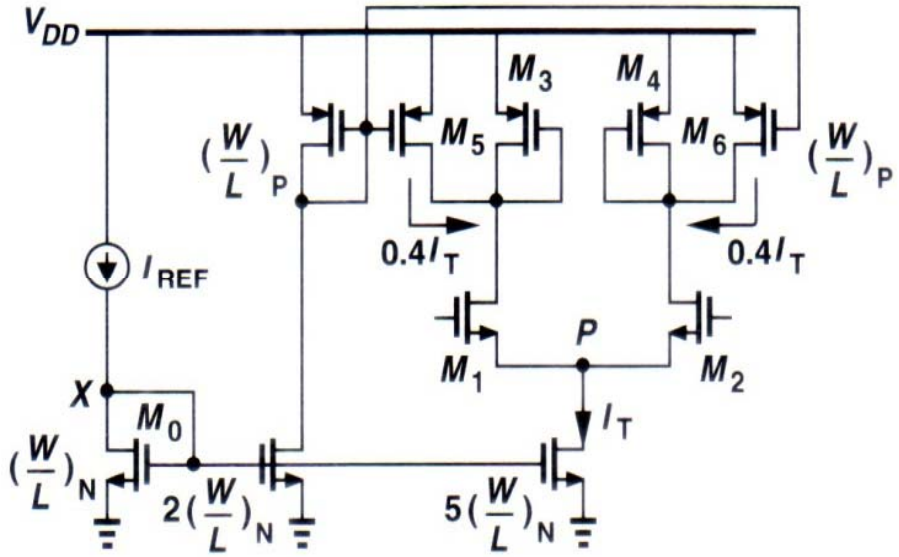
Simple Resistive Biasing:



$$I_{out} \approx \frac{1}{2}\mu_o C_{ox}\frac{W}{L}\left(\frac{R_1}{R_1+R_2}V_{DD}-V_{TH}\right)^2$$

- I_{out} is not accurate as it depends on process, V_{DD} and temperature
- V_{TH} can varies 100mV from wafer to wafer.
- More severe if the overdrive voltage is lesser in order to consume less headroom. E.g., $V_{GS}=V_{OV}+V_{TH}=200mV+(400mV\pm50mV)$.

Usage of Current Mirrors:

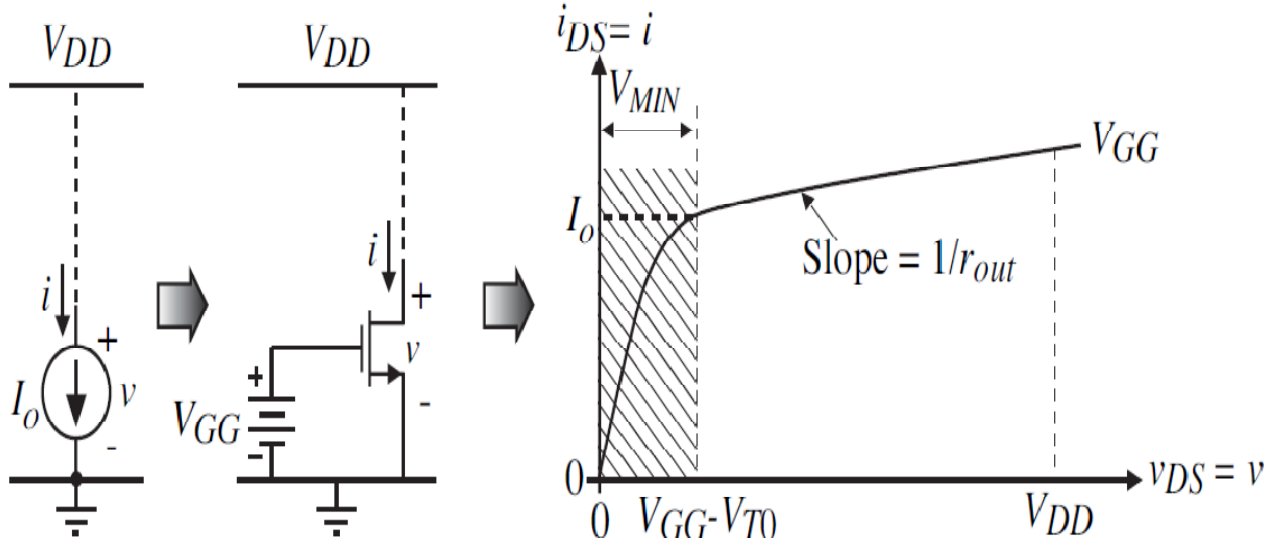


Current mirrors usually employ the same length for all the transistors so as to minimize errors due to side-diffusion of the source and drain area.

$L_{effective} = L_{drawn} - L_{diffusion}$

If L_{drawn} is doubled, $L_{effective}$ is not as $L_{diffusion}$ is relatively constant.

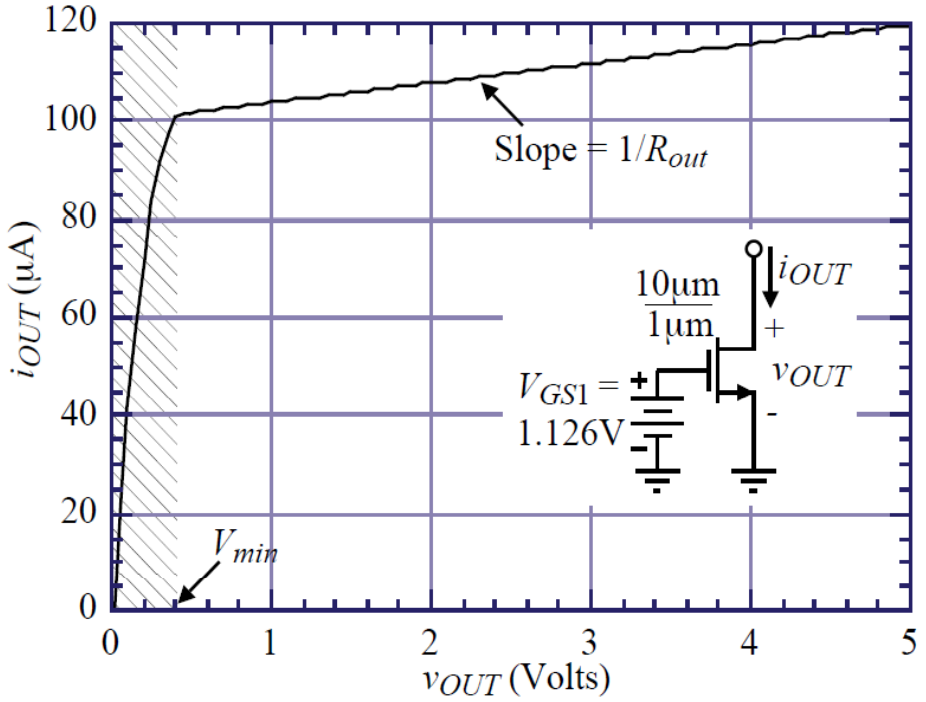
MOS as Current Source:



2 important quantities:

- R_{out} → 'flatness' of the current sink/source (ideally independent of voltage).
- V_{MIN} →The minimum output voltage when the current is more constant.

Example of a MOS Current Sink:



K_N=110uA/V^2, V_{TH}=0.7, λ=0.04V^{-1}

$$r_{ds} = \frac{1}{\lambda I_D} = 250K\Omega$$

$$I_D = \frac{1}{2} K_N \frac{W}{L} (V_{GS} - V_{TH})^2 = 100uA$$

$$g_m = K_N \frac{W}{L} (V_{GS} - V_{TH}) = 110u.10(1.126 - 0.7) = 469uS$$

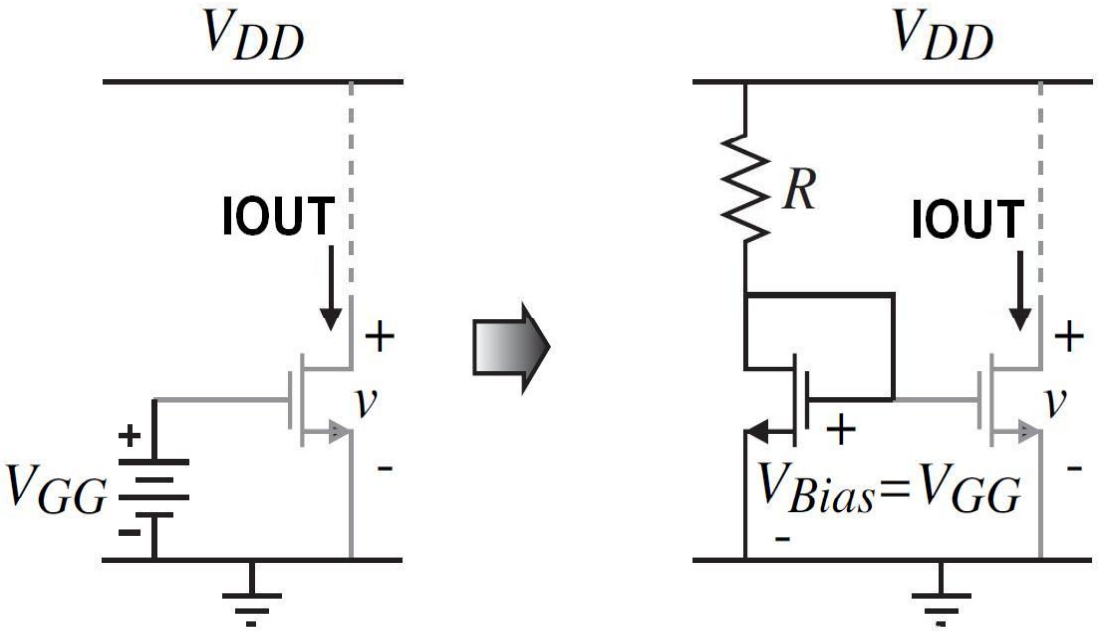
Improve rout and VMIN:

$$V_{MIN} = V_{OV} = \sqrt{\frac{2I_D}{K_N \frac{W}{L}}} = \sqrt{\frac{2.100u}{100u.10}} = 0.426$$

V_{MIN}=0.1V if W/L=182

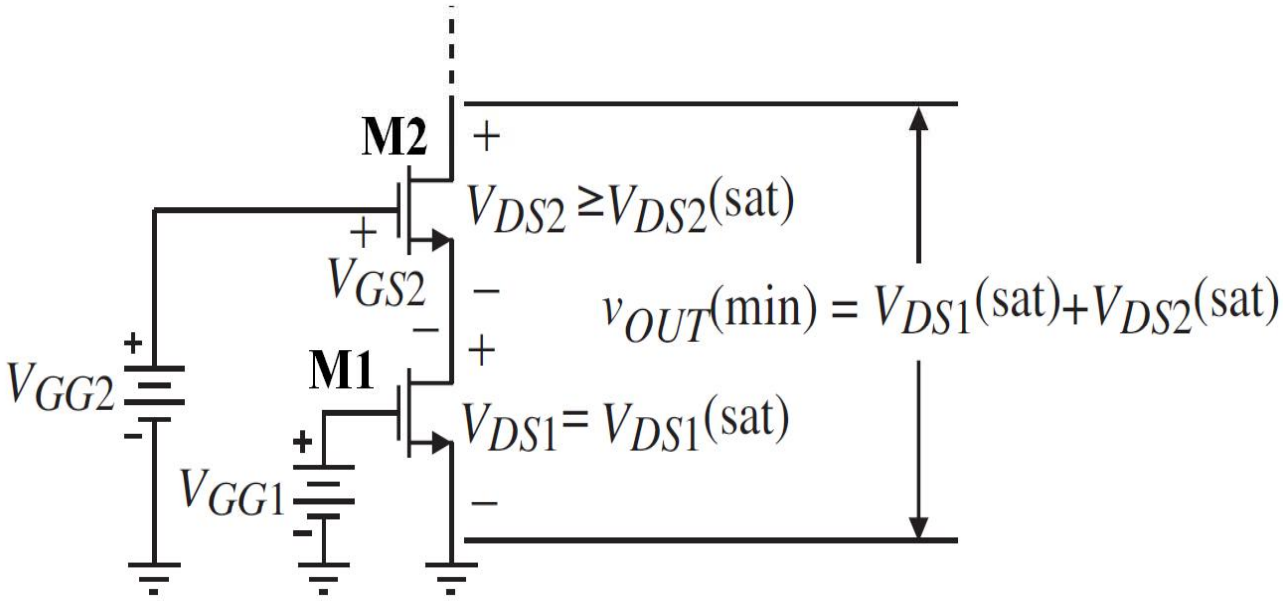
Rout can be improved through source-degeneration (cascode configuration)

A Simple Current Sink:



Accuracy of V_{DD}, R, V_{TH} affect I_{OUT}.

Cascode Current Sink:



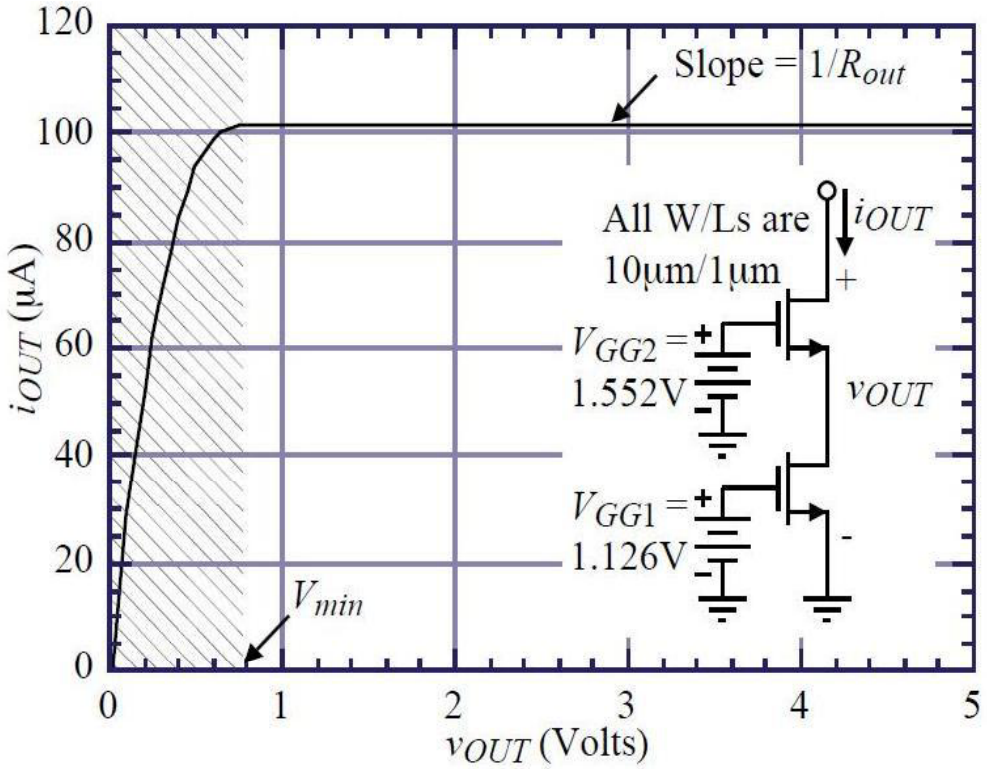
V_{GG1} is to bias M1 for the desired current. M1 must be in saturation.

V_{GG2} is to keep V_{DS1} as small as possible and still in saturation.

$V_{GG2} = V_{DS1,sat} + V_{GS2} = V_{DS1,sat} + V_{TH} + V_{DS2,sat}$ or two V_{ov} + one V_{TH}.

For the previous NMOS current sink, V_{GG2} should be V_{GG2}=2(0.426)+0.7=1.552V.

Example of Cascode Current Sink:

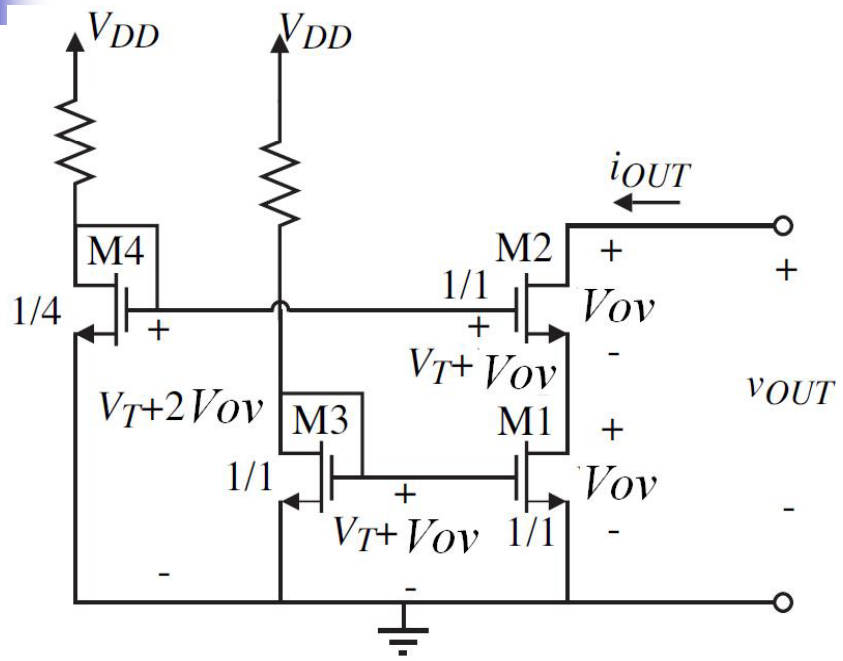


Using the previous parameter (ignore the bulk effect):

$V_{MIN}=2\ V_{DS,sat}=2(0.426)=0.852$

$R_{out}=g_m*r_{ds}*r_{ds}=469u.250K.250K=29.3M\Omega$

High-Swing Cascode Current Sink:



$V_{OV} = \sqrt{\frac{2I_D}{K_N \frac{W}{L}}}$, if W/L increases 4X, V_{ov} reduces by 2X.

In order to get $V_{min}=2V_{ov}=2*0.5V=1V$ and $I_D=100uA$, $\frac{W}{L} = \frac{2I_{OUT}}{K_N (V_{OV})^2} = \frac{2.100u}{110u.0.25} = 7.27$

For M_4, $2V_{ov}$ is needed, hence the size of $W_4/L_4=7.27/4=1.82$

V_{DS} of M3 and M1 are not equal, Iout≠Iref or there is mirroring error.

Voltage and Current Reference:

Independent voltage or current source that has a high degree of precision and stability. They should be independent of PVT.

Since most process parameters vary with temperature, if a reference is temperature-independent, then it is usually process independent as well.

The characteristics of bipolar transistors have proven to be the most reproducible and well-defined quantities that can provide positive and negative TC (temperature coefficient).

Negative-TC voltage [3]:

$I_C = I_S e^{V_{BE}/V_T}$, where $V_T = \frac{KT}{q}$

$I_S \propto \mu K T n_i^2$, where μ denotes the mobility of minority carriers and n_i is the intrinsic minority carrier concentration of silicon.

$\mu \propto \mu_o T^m$, where m≈-3/2

$n_i^2 \propto T^3 e^{-\frac{Eg}{KT}}$, where Eg≈1.12 eV is the bandgap energy of silicon.

Thus, $I_S = bT^{4+m} e^{-\frac{Eg}{KT}}$, where b is a proportionality factor.

$$V_{BE} = V_T ln\left(\frac{I_C}{I_S}\right)$$

$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} ln\left(\frac{I_C}{I_S}\right) - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T}$, assuming I_C is constant wrt T.

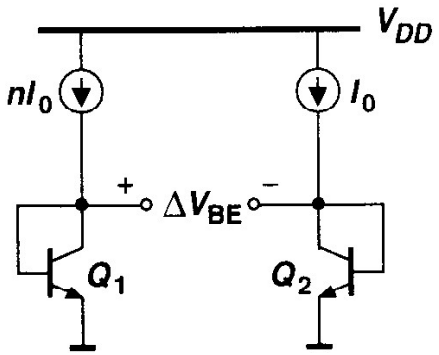
$$\frac{\partial I_S}{\partial T} = b(4+m)T^{3+m} e^{-\frac{Eg}{KT}} + bT^{4+m}\left(e^{-\frac{Eg}{KT}}\right)\left(\frac{Eg}{KT^2}\right)$$

Then, $\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - Eg/q}{T}$

TC of VBE is a function of T. With VBE≈750mV and T=300°K, $\frac{\partial V_{BE}}{\partial T} \approx -1.5 mV/°K$

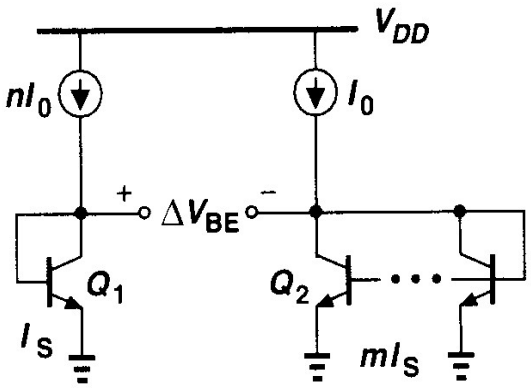
Positive-TC Voltage:

Difference between two V_{BE} = PTAT (proportional to absolute temperature).



Neglecting base current,

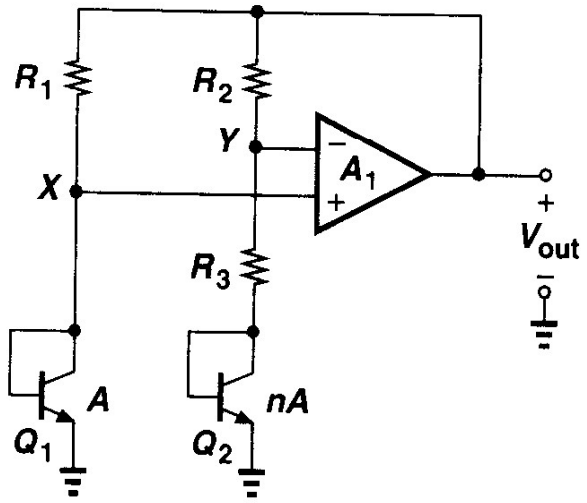
$$\Delta V_{BE} = V_{BE1} - V_{BE2}$$
$$= V_T ln \frac{nI_o}{I_S} - V_T ln \frac{I_o}{I_S} = V_T ln(n)$$
$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{K}{q} ln(n)$$



$$\Delta V_{BE} = V_T ln(nm)$$
$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{K}{q} ln(nm)$$

The ratio can be controlled through current ratio of size ratio.

Bandgap Reference:



Bandgap reference is derived from V_{BE} (CTAT) and ΔV_{BE} (PTAT).

$$V_{REF} \approx \alpha_1 V_{BE} + \alpha_2 V_T ln(n)$$

At room temperature, $\frac{\partial V_{BE}}{\partial T}$=-1.5mV/°K and $\frac{\partial V_T}{\partial T}$=+0.087mV/°K.

$$V_{REF} \approx V_{BE} + 17.2 V_T \approx 1.25V$$

Opamp ensures V_X=V_Y. ΔV_{BE} drops across R3. I_{PTAT} flows into Q1 and Q2.

$$V_{OUT} = V_{BE2} + \frac{V_T ln(n)}{R_3}(R_3 + R_2) = V_{BE2} + V_T ln(n)\left(1 + \frac{R_2}{R_3}\right)$$

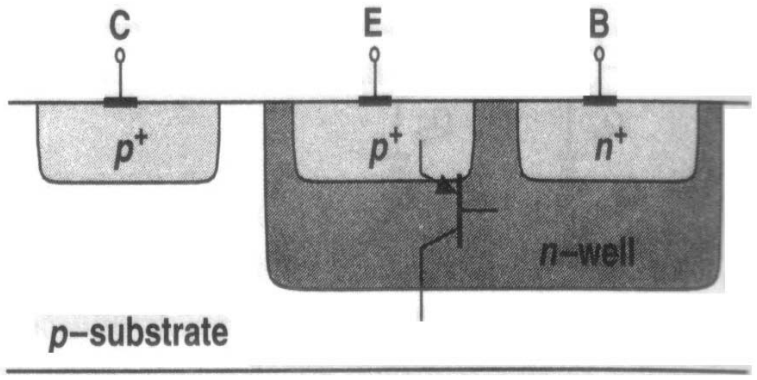
We could choose n=31 and R_2/R_3=4.

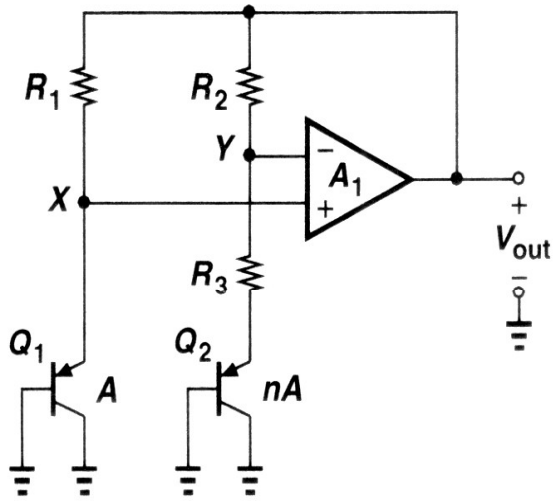
TC of resistors will not affect V_{OUT} since ratio is used in the equation.

Bandgap Reference: Collector Current Variation

- I_{PTAT} flows into Q1 and Q2 (previous slide). However, we assume IC is constant when we derived $\frac{\partial V_{BE}}{\partial T}$.
  The effect is $\frac{\partial V_{BE}}{\partial T}$ is slightly less negative than -1.5mV/°K.
- R typically has positive-TC.
- In practice, accurate simulations (+ accurate models) are necessary to predict the temperature coefficient.

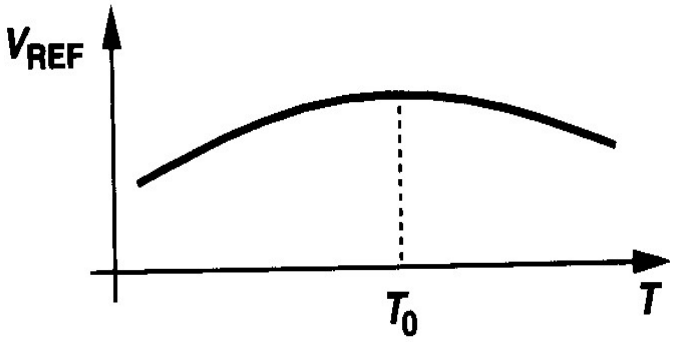
Bandgap Reference: Vertical Parasitic pnp BJT

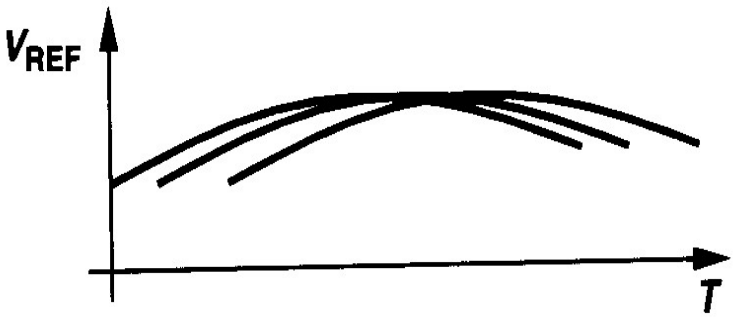




Without additional mask, vertical parasitic pnp BJT is available in CMOS process.

Bandgap Reference: Curvature Correction



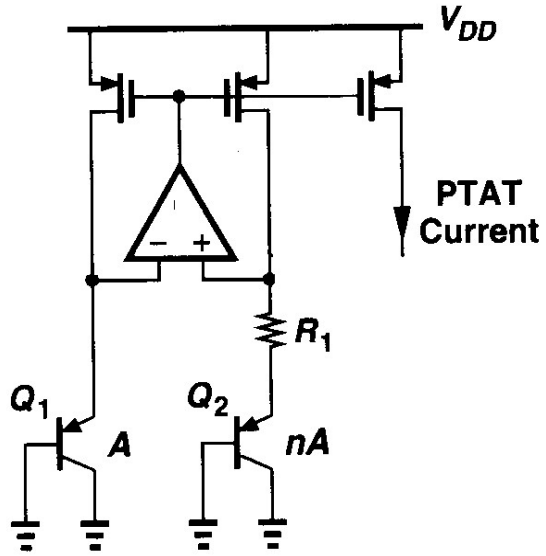


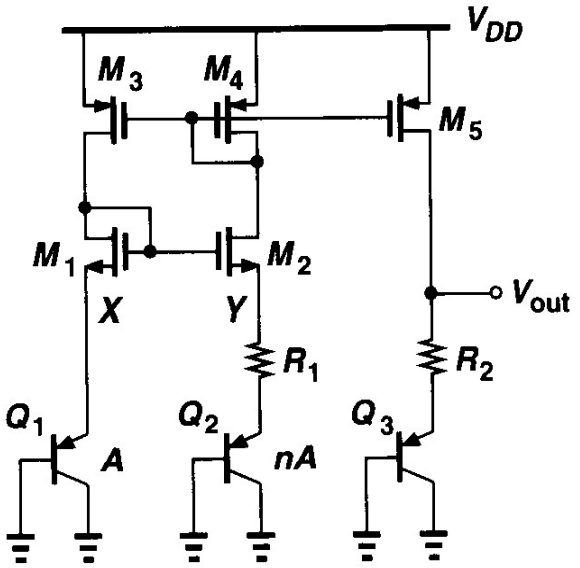
Bandgap voltage exhibits a finite curvature. The TC is typically zero at only one temperature.

Some techniques have been devised to suppress the variation of VREF – curvature correction technique.

Likely result of Bandgap Voltage is shown. At certain temperature, VREF is Gaussian distributed.

PTAT Current:





I_{PTAT}=ΔV_{BE} drop across R1

Typically g_m↓as Temp↑, increasing current (I_{PTAT}) help to compensate the drop of g_m.

$$V_{bandgap} = V_{CTAT} + I_{PTAT} R_2 = V_{CTAT} + \Delta V_{BE} \frac{R_2}{R_1}$$