Introduction to CMOS Analog Integrated Circuit Design

Course Title : **Introduction to CMOS Analog Integrated Circuit Design**

Organising Group : **ICDC**

Date : **27 Sept 2010**

Course Objective(s)

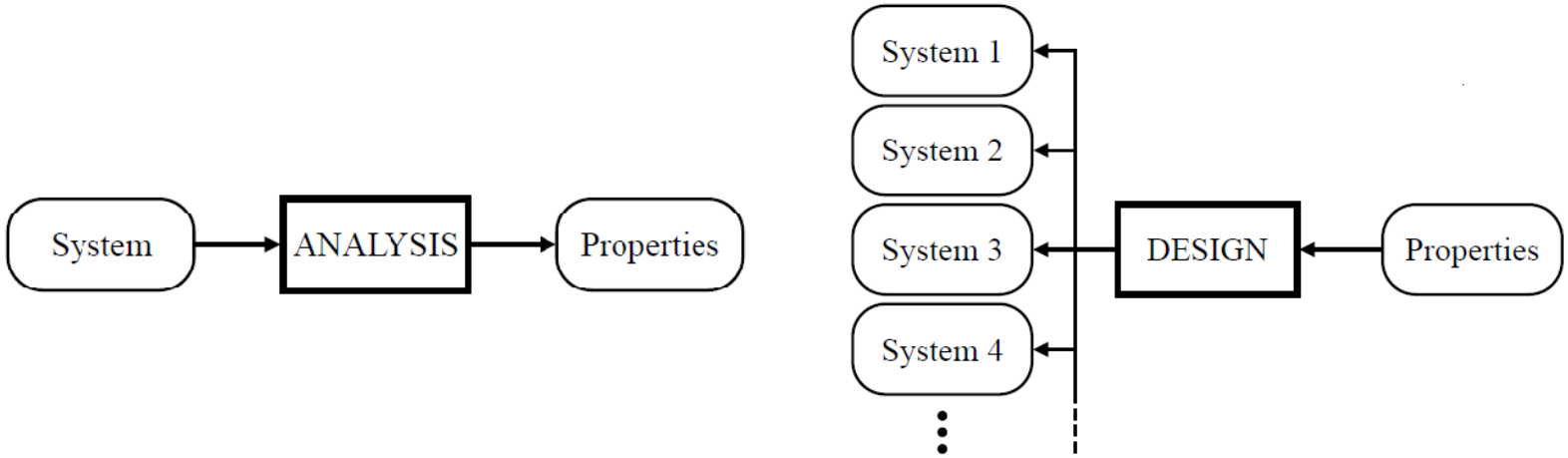
: This course is aimed to introduce the participants to CMOS Analog IC Design. Building blocks circuits such as current mirror, voltage and current reference, differential amplifier and operational amplifier and their applications will be discussed. Electronic Design Automation tools will be use to simulate on some circuits in order to enhance the understanding of key parameters that determines the performance of the circuits.

Content:

AM Tan See Teck	PM Teo Chee Keong
- Introduction - CMOS Transistor - CMOS Reference	- Differential Amplifier - Operational Amplifier - Opamp Applications - Opamp Design Considerations
Lab1 & 2	Lab 3

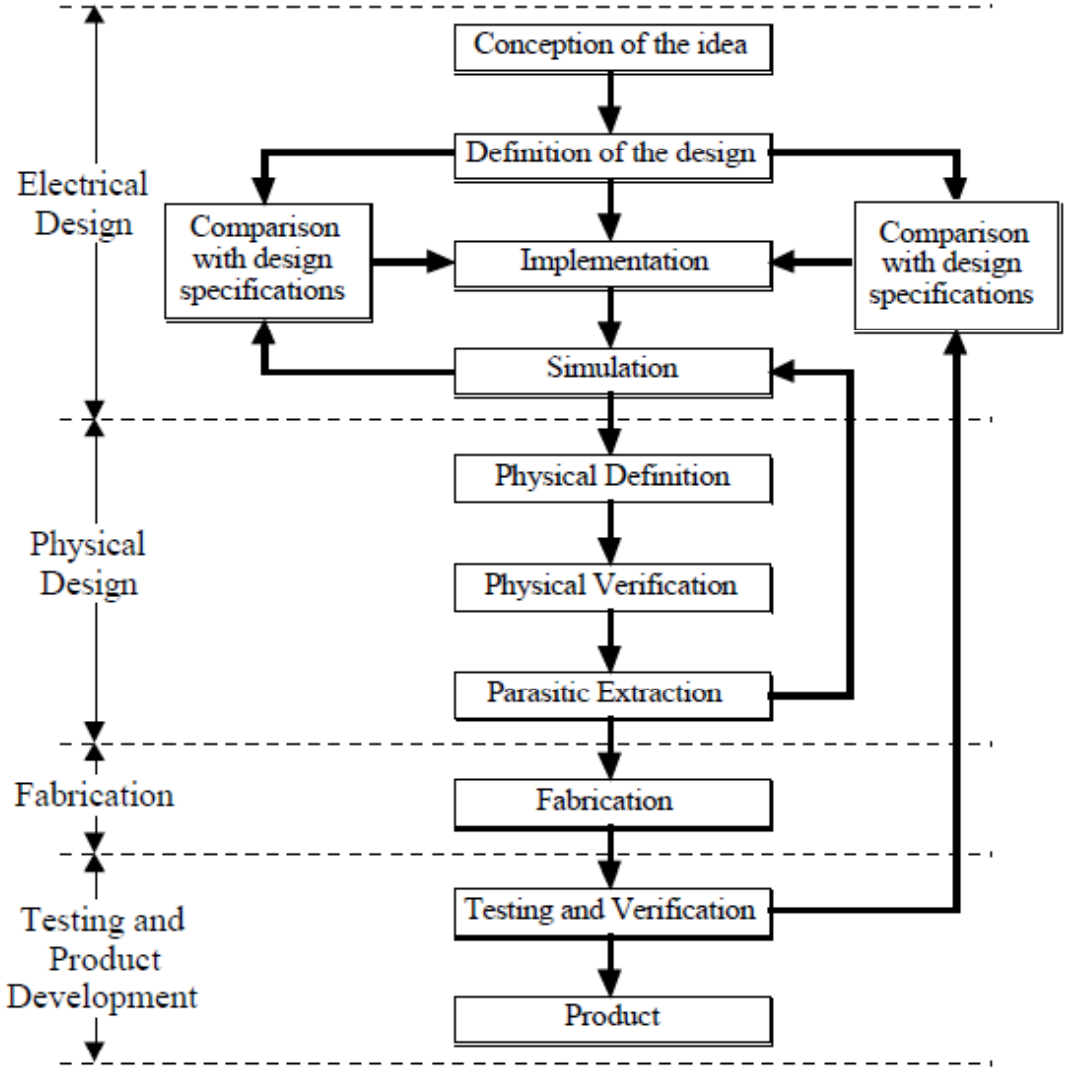
Analysis and Synthesis (design):

Difference between Analysis and Synthesis (design)

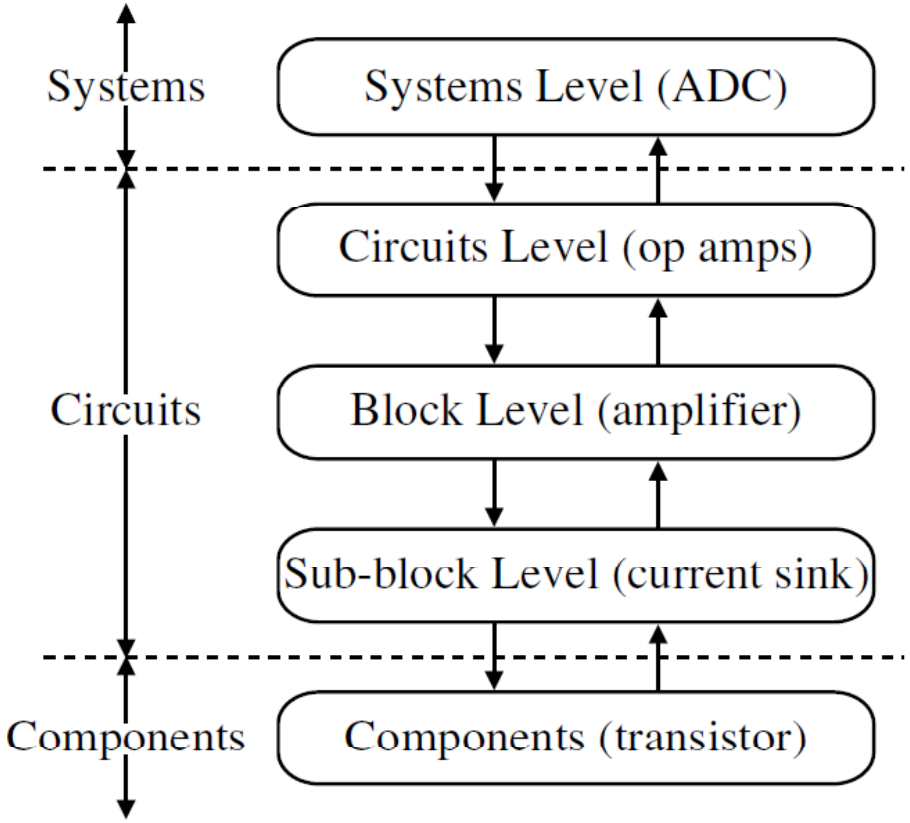


Analysis	**Design**
Given a system, find its properties.	Given a set of properties or specifications, find a system that meet the specifications.
The solution is unique.	No unique solution. Innovation in play.
More like science.	More like art.

Analog IC Design Flow:



Complexity of Analog Design:



- System Design is Top-down.
- Circuit Design is Bottom-up.
- There are less repeated blocks in analog design.

Level of Hierarchy or Abstraction:

Hierarchy	Design	Physical	Model
System or architectural	System specifications	Floor plan, pad arrangement.	Behavioral model
Circuits	Circuit specifications	Circuit Layout	Macromodels
Devices	Device specifications	Geometrical description, P-cell, layout rules	Device models

Devices →Handled by foundry. Process Design Kit (PDK) is the interface between foundry and circuit designer.

Systems → Handled by system designer. Application or product level knowledge is required. Usually, system designer are also experienced circuit designer.

Circuits → Domain of circuit designer.

System Level: Design

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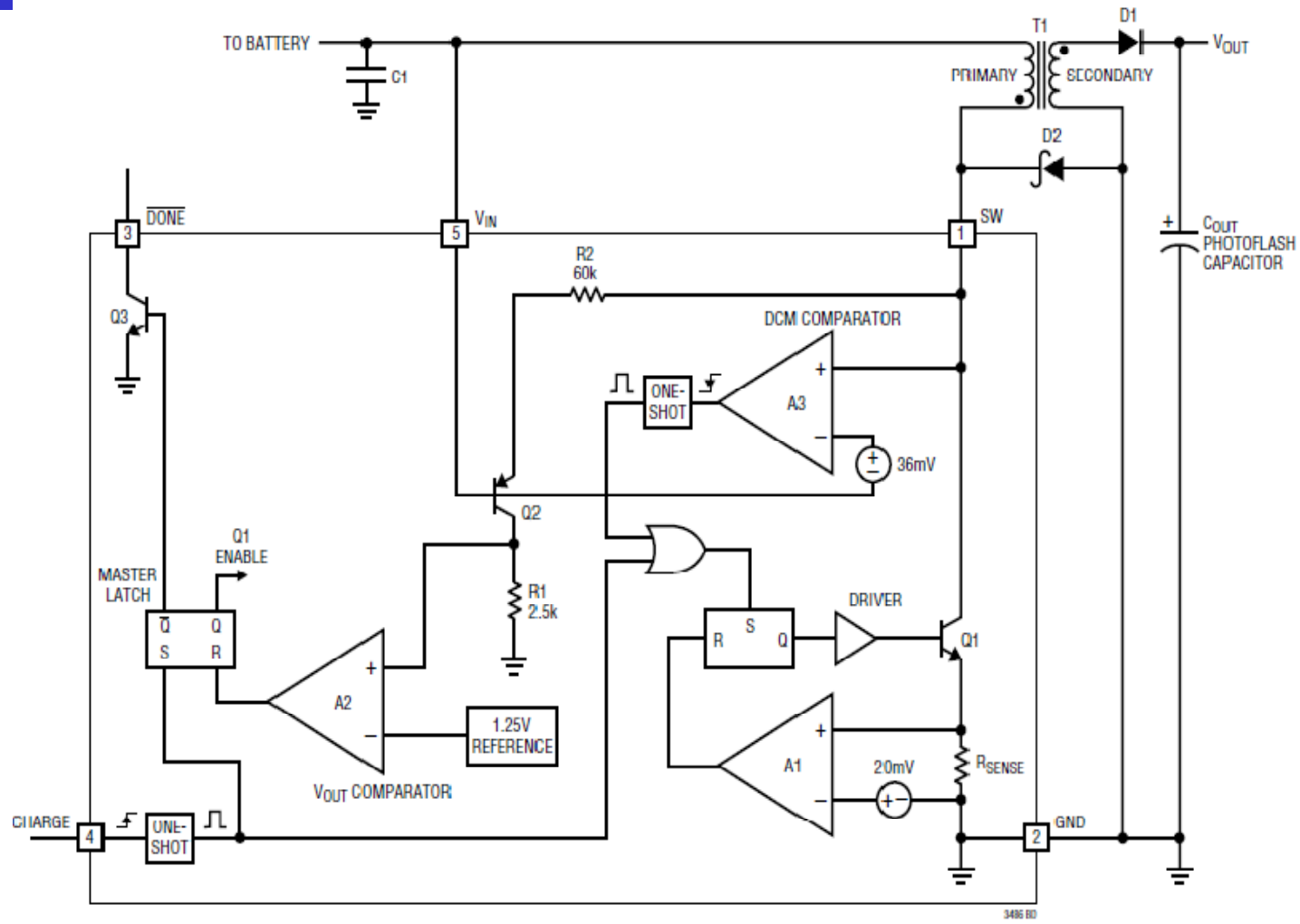
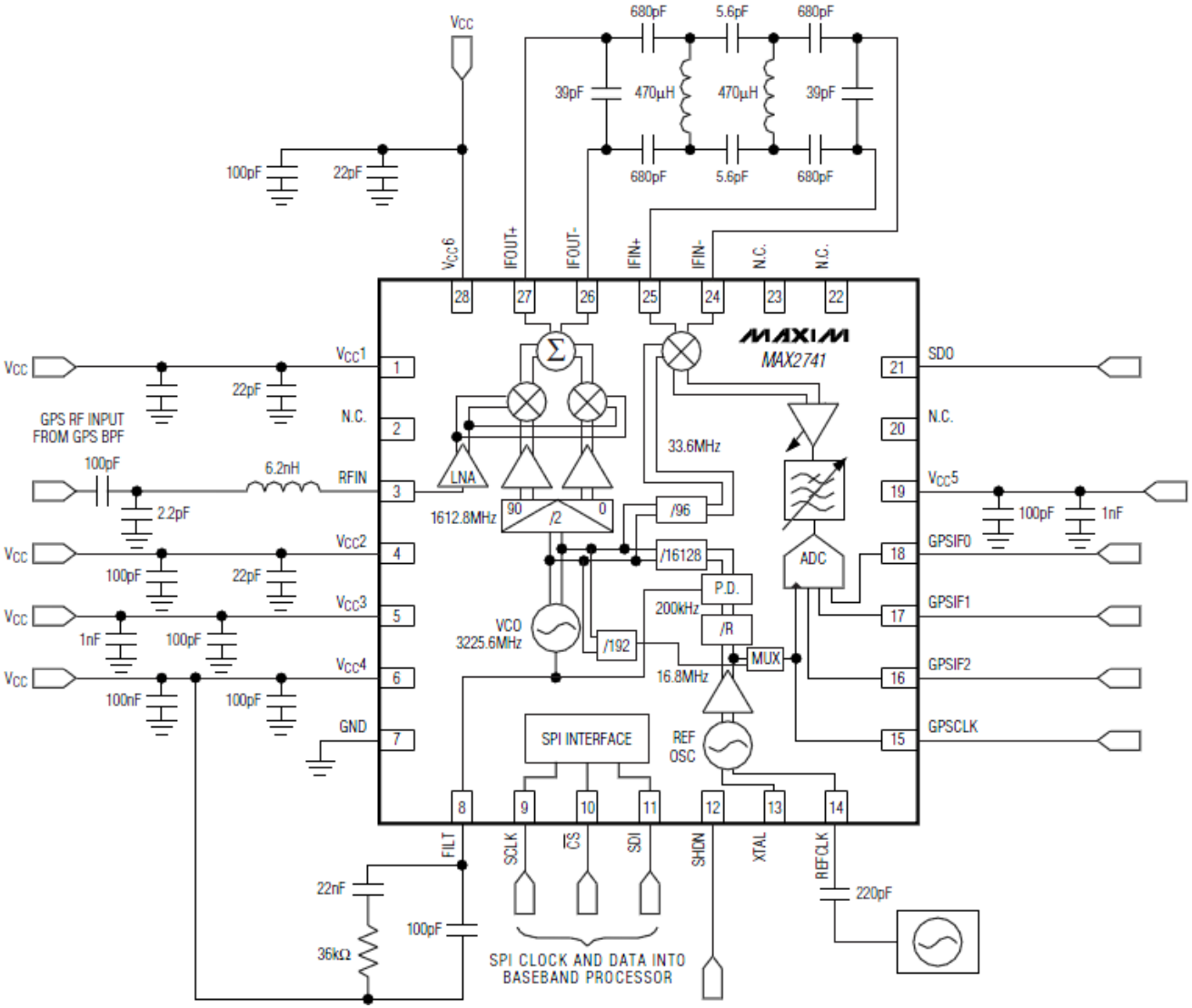


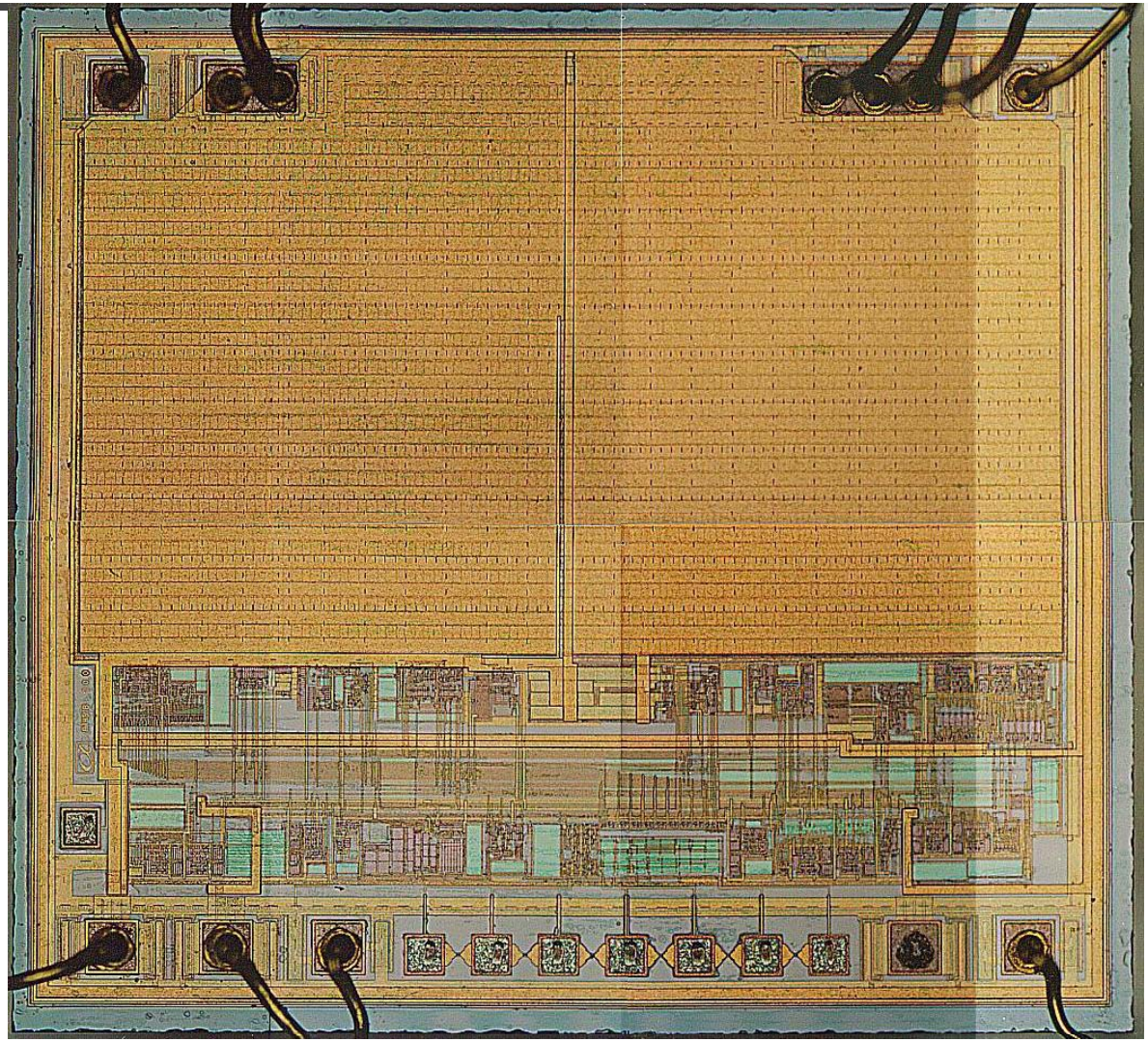
System Level: Design

- System Design is top-down.
- Get input from customer (through application/Product/Marketing engineer/manager).
- Study datasheets of competitors.
- Come out specifications of various circuits for circuit designer to work on.
- System level simulation at SPICE level or behavior level.
- Complete versus partial system simulation?
- External component (model available?) to be included in the simulation?

System Level: Design



System Level: Layout



System Level: Layout

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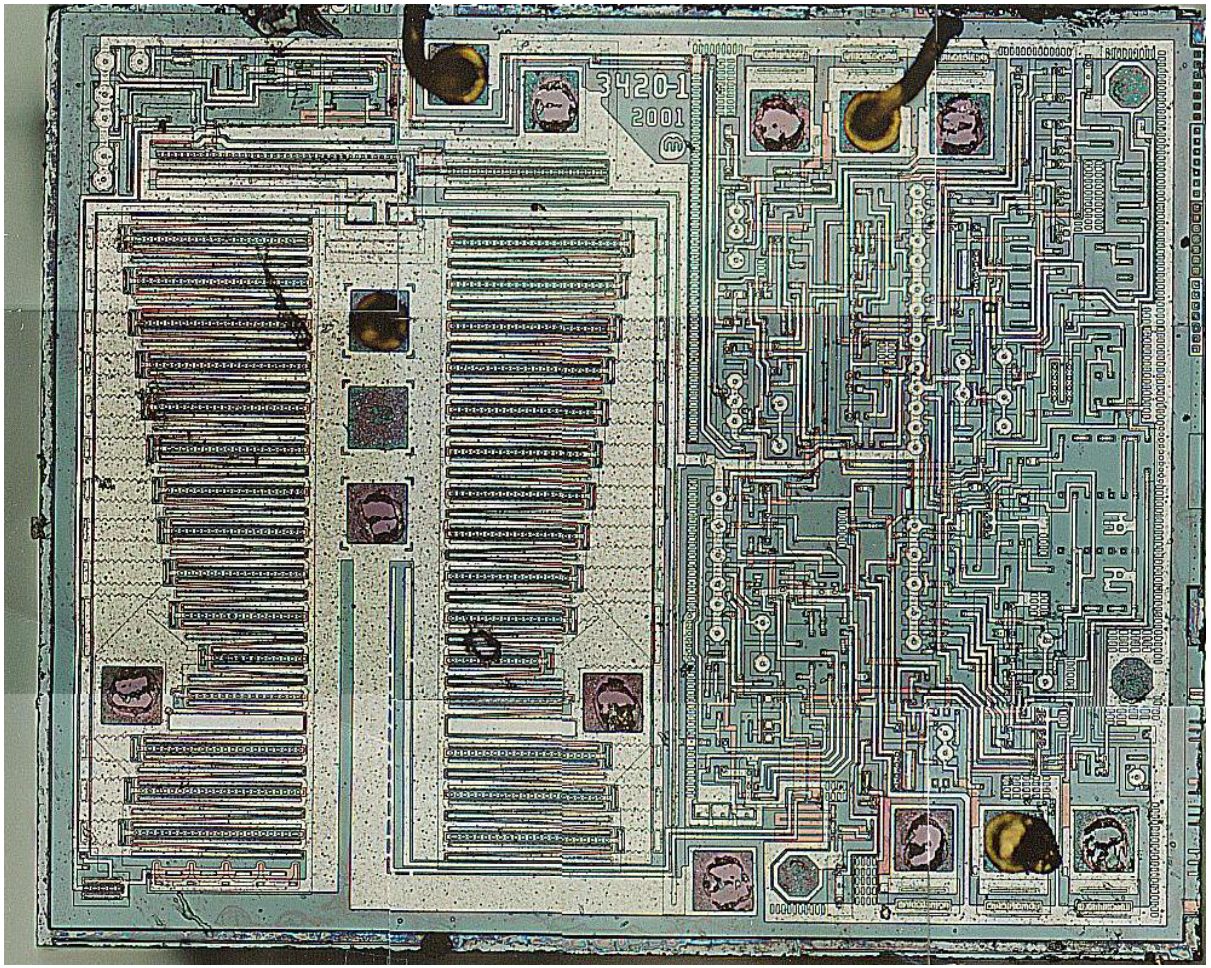
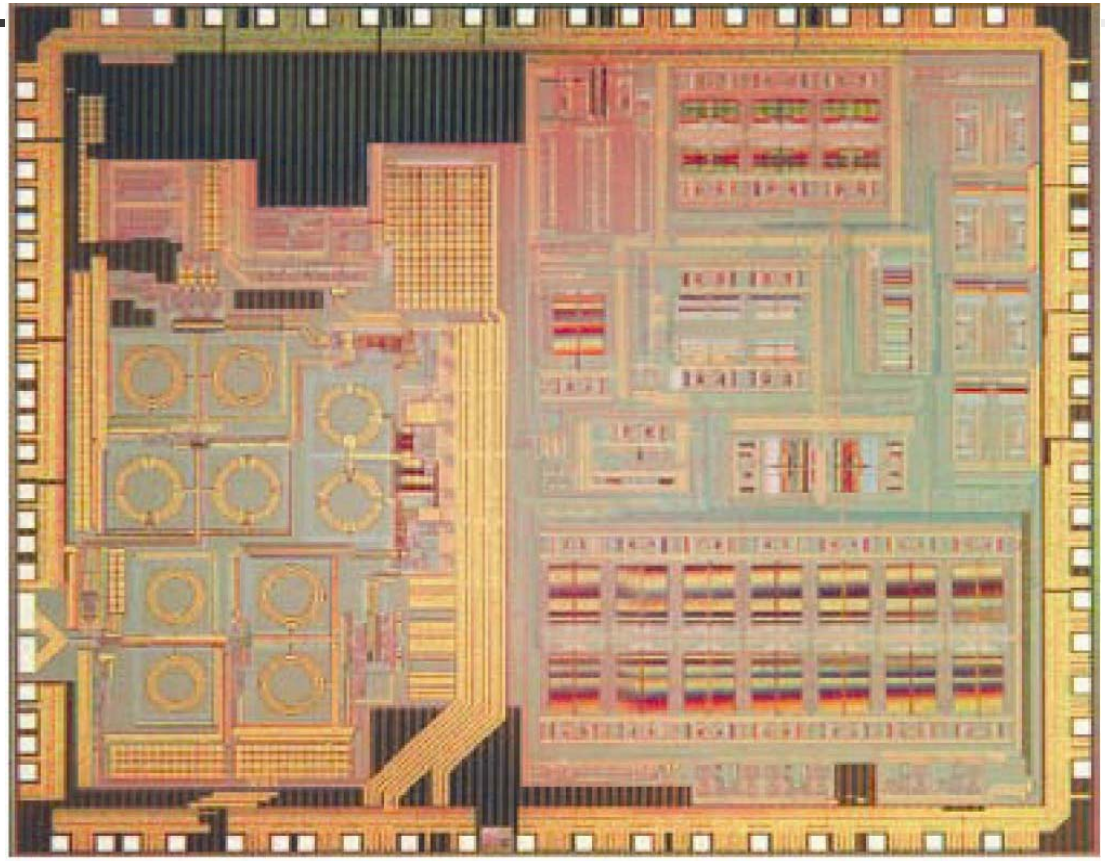


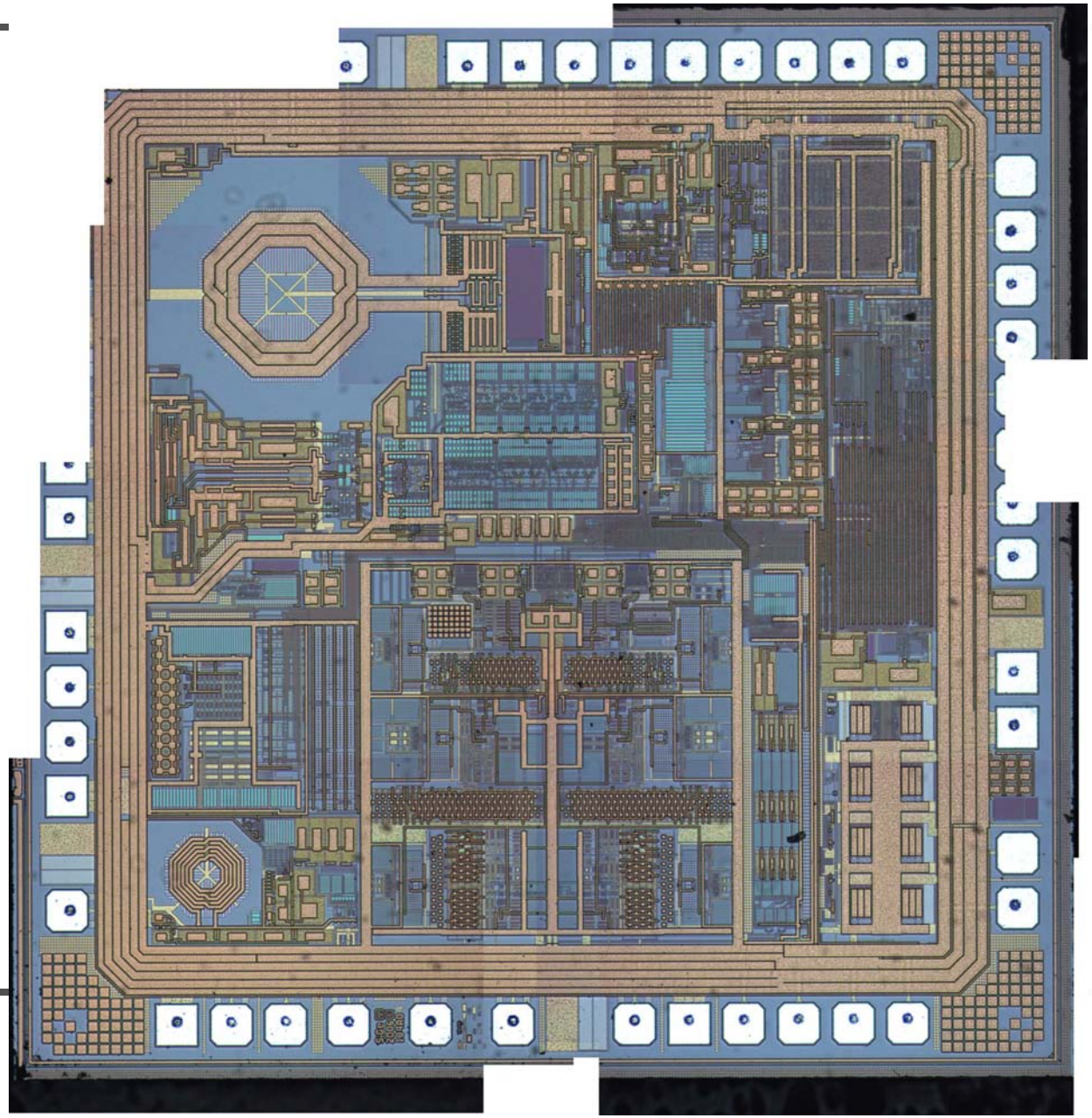
- As long as it works, funny pad arrangement is acceptable.

System Level: RFIC (Bluetooth Transceiver)



- L takes up area (cost).
- Meeting performance without using L?
- Burning more power against using L?

System Level: RFIC (GPS Receiver)



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Process, Voltage and Temperature (PVT):

- The system or circuits need to meet the specification under PVT variation.

- Process → Various corner simulation to cater for process variation.

- Voltage → Example, 1.6 to 2.0V for 0.18um technology, 1.1 to 1.3V for 0.13um technology.

- Temperature → Junction temperature. Depending on application. Such as -40ºC to 120ºC. What is the ambient temperature? What is the power dissipation and packaging adopted?

Process, Voltage and Temperature (PVT):

MAX2741

ABSOLUTE MAXIMUM RATINGS

V_{CC} Pins to GND .....-0.3V to +3.3V
V_{CC} Pins to Each Other .....-0.3V to +0.3V
FILT to GND.....-0.3V to (V_{CC} + 0.3V)
CMOS Inputs to GND (SHDN, SCLK, $\overline{CS}$, SDI).....+0.3V to (V_{CC} + 0.3V)
CMOS Outputs to GND (CLKOUT, GPSIF_, SDO).....-0.3V to (V_{CC} + 0.3V)
RFIN to GND.....-0.3V to (V_{CC} + 0.3V)
First IF Filter I/O to GND (IFOUT±, IFIN±).....-0.3V to (V_{CC} + 0.3V)
Crystal Inputs to GND (XTAL, REFCLK).....-0.3V to (V_{CC} + 0.3V)
Maximum RF Input Power.....0dBm
Continuous Power Dissipation (T_A = +85°C)
28-Pin Thin QFN (derate 20.8mW/°C above +70°C) .1000mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

LT3468/LT3468-1

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage 16V
SW Voltage .....–0.4V to 50V
CHARGE Voltage..... 10V
$\overline{DONE}$ Voltage 10V
Current into $\overline{DONE}$ Pin ..... ±1mA
Maximum Junction Temperature ..... 125°C
Operating Temperature Range (Note 2) ...–40°C to 85°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

- Ambient temperature to junction temperature will depends on thermal impedance of packaging.

Analog Design versus Digital Design:

- Digital: Speed ↔ Power ↔ Area

- Analog: Speed ↔ Power ↔ Area ↔ Precision ↔ Gain ↔ Noise ↔ Linearity etc.

- Analog Designer need to grasp multiple concepts simultaneously.

- Must be able to make appropriate simplifications and assumptions.

Analog Design versus Digital Design:

Analog Circuits	Digital Circuits
Signals are continuous in amplitude and can be continuous or discrete in time	Signals are discontinuous in amplitude and time – binary states
Designed at circuit level	Designed at the systems level using HDLs
Customised methodology	Standard methodology
CAD tools are difficult to apply	CAD tools have been extremely successful
Requires precision modelling	Timing models only
Performance optimised	Programmable by software
Irregular blocks	Regular blocks
Difficult to route automatically	Easy to route automatically
Dynamic range is limited by power supplies and noise (and linearity)	Dynamic range unlimited
IP not easily portable	Pervasive with IPs

Analog Design Productivity: [6]

- While digital designers have improved their design methodology and adopted automation, analog and mixed-signal designers by and large have not.

- More re-spins (2, 3 or 4?) for design of complex analog chip as compare to complex digital chip.

- The mismatch in schedule and risk between analog and digital portion of mixed-signal (or SoC) design makes it difficult to justify combining analog and digital on the same chip.

- Due to low-level of productivity, difficult to assembled a team that is large enough to take on a project and complete it in timely manner.

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